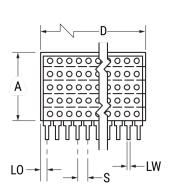
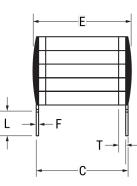


General Information



Side View



End View

Series KPS LDD Comm SMPS Leaded Stacked Chip Style Description Low ESR, High Current Stacked Ceramic Chips Low ESR, High Current, High Performance Features RoHS No 🛕 WARNING: Cancer and reproductive harm -Prop 65 http://www.p65warnings.ca.gov. Termination 60/40 Solder Coated Lead Wire Leads Failure Rate N/A Testing and Commercial Reliability AEC-Q200 No Note: Number of chips in stack depends on design. Notes Number of Chips in this stack = 5. Note: Lead alignment within pin rows shall be within ±.0.13 mm.

Click here for the 3D model.

Dimensions	
D	9.845mm +/-0.955mm
L	6.35mm MIN
Т	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
А	16.51mm MAX
С	10.16mm +/-0.635mm
Е	11.18mm +/-0.25mm
G	1.4mm +/-0.254mm
LO	1.586mm MAX
LW	0.508mm +/-0.051mm

Packaging Specifications			
Packaging	Waffle, Box		
Packaging Quantity	36		

Specifications			
Capacitance	3.9 uF		
Capacitance Tolerance	10%		
Voltage DC	500 VDC		
Dielectric Withstanding Voltage	750 VDC		
Temperature Range	-55/+125°C		
Temperature Coefficient	X7R		
Dissipation Factor	2.5% 1 kHz 25C		
Aging Rate	3% Loss/Decade Hour		
Insulation Resistance	25.6 GOhms		

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.