Please note that effective July 26, 2021, the former Infrastructure and Automotive business of Silicon Labs is now part of Skyworks' Mixed Signal Solutions. All Silicon Labs registered trademarks that may be contained herein remain the sole property of Silicon Laboratories, Inc. and are only for nominative descriptive purposes and do not represent any sponsorship or endorsement of such product(s) by Silicon Labs.



Si5348A Datasheet Addendum Device Configuration Summary for Si5348A-B-GM

Page 1 of 2

7-Output Stratum 3/3E SETS, G.8262 EEC Option 1 and 2, IEEE 1588 Network Synchronizer

Overview

Part: Si5348 Design ID: 5348BP2

Created By: ClockBuilder Pro v1.7 [2015-03-26] Timestamp: 2015-03-26 09:25:11 GMT-05:00

Device Grade

Device Output Clock
Grade Frequency Range Typical Jitter
-----Si5348A* 100 Hz to 710.4 MHz < 150 fs
Si5348B 100 Hz to 350 MHz "

* Device Grade

Design

=====

Host Interface:

I/O Power Supply: VDD (Core)

SPI Mode: 4-Wire

I2C Address Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins)

XA/XB:

48 MHz (XTAL - Crystal)

Inputs:

INO: Unused IN1: Unused IN2: Unused IN3: Unused IN4: Unused

Outputs:

OUTO: Unused OUT1: Unused OUT2: Unused OUT3: Unused OUT4: Unused OUT5: Unused OUT6: Unused

Frequency Plan

No plan

This datasheet addendum is provided as supplemental information to the Si5348A datasheet, located at www.silabs.com/timing. You can search for and download any datasheet addendum for Si534x/8x part numbers. Go to https://www.silabs.com/custom-timing for more information.

Silicon Laboratories 400 West Cesar Chavez Austin, TX 78701 Phone (512) 416-8500



Si5348A Datasheet Addendum Device Configuration Summary for Si5348A-B-GM

Page 2 of 2

www.silabs.com