



# Half-Bridge MOSFET Driver for Switching Power Supplies

## FEATURES

- 4.5- to 5.5-V Operation
- Undervoltage Lockout
- 250-kHz to 1-MHz Switching Frequency
- Shutdown Quiescent Current <math><5 \mu\text{A}</math>
- One Input PWM Signal Generates Both Drive
- Bootstrapped High-Side Drive
- Operates from 4.5- to 30-V Supply
- TTL/CMOS Compatible Input Levels
- 1-A Peak Drive Current
- Break-Before-Make Circuit

## APPLICATIONS

- Multiphase Desktop CPU Supplies
- Single-Supply Synchronous Buck Converters
- Mobile Computing CPU Core Power Converters
- Standard-Synchronous Converters
- High Frequency Switching Converters

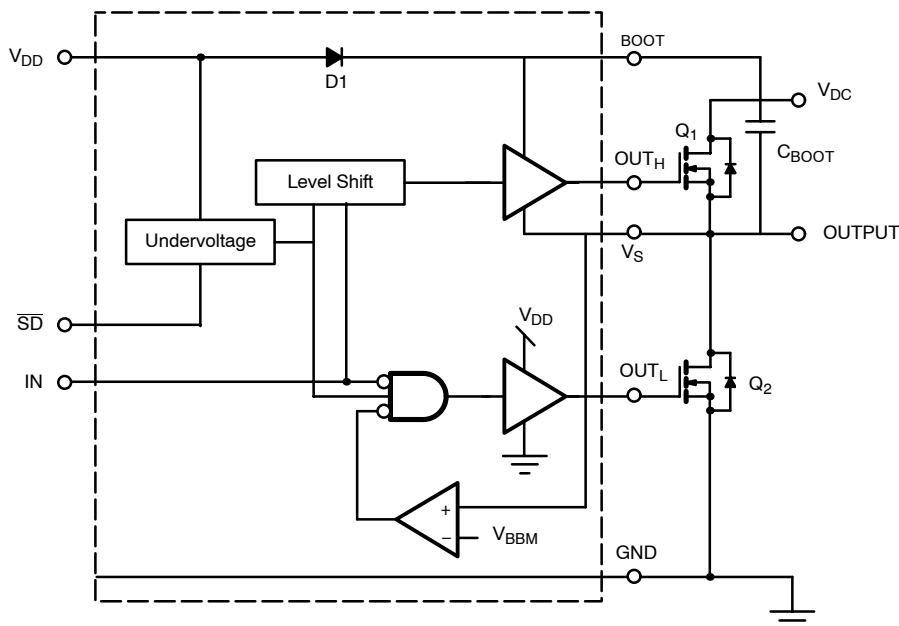
## DESCRIPTION

The Si9912 is a dual MOSFET high-speed driver with break-before-make. It is designed to operate in high frequency dc-dc switchmode power supplies. The high-side driver is bootstrapped to handle the high voltage slew rate associated with “floating” high-side gate drivers. Each driver is capable of switching a 3000-pF load with 60-ns propagation delay and 25-ns transition time. The Si9912 comes with an internal break-before-make feature to prevent shoot-through current in the external MOSFETs. A shutdown pin is used to enable the

driver. When disabled, the quiescent current of the driver is less than 5  $\mu\text{A}$ .

The Si9912 is available in both standard and lead (Pb)-free, 8-pin SOIC packages for operation over the industrial operation range ( $-40^\circ\text{C}$  to  $85^\circ\text{C}$ ).

## FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE



TRUTH TABLE				
$V_S$	$\overline{SD}$	IN	$V_{OUTL}$	$V_{OUTH}$
L	L	L	L	L
L	L	H	L	L
L	H	L	H	L
L	H	H	L	H
H	L	L	L	L
H	L	H	L	L
H	H	L	L	L
H	H	H	L	H


**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Limit	Unit
Low Side Driver Supply Voltage	V <sub>DD</sub>	7.0	V
Input Voltage on IN	V <sub>IN</sub>	-0.3 to V <sub>DD</sub> +0.3	
Shutdown Pin Voltage	V <sub>SD</sub>	-0.3 to V <sub>DD</sub> +0.3	
Bootstrap Voltage	V <sub>BOOT</sub>	35.0	
High Side Driver (Bootstrap) Supply Voltage	V <sub>BOOT</sub> - V <sub>S</sub>	7.0	
Operating Junction Temperature Range	T <sub>J</sub>	-40 to 125	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to 150	
Power Dissipation (Note a and b)	P <sub>D</sub>	830	mW
Thermal Impedance	θ <sub>JA</sub>	125	°C/W
Lead Temperature (soldering 10 Sec)		300	°C

## Notes

- a. Device mounted with all leads soldered to P.C. Board  
 b. Derate 8.3 W/°C above 25 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Limit	Unit
Bootstrap Voltage (High-Side Drain Voltage)	V <sub>BOOT</sub>	4.5 to 30	V
Logic Supply	V <sub>DD</sub>	4.5 to 5.5	
Bootstrap Capacitor	C <sub>BOOT</sub>	100 n to 1 μ	F
Ambient Temperature	T <sub>A</sub>	-40 to 85	°C

**SPECIFICATIONS**

Parameter	Symbol	Test Conditions Unless Specified V <sub>DD</sub> = 4.5 to 5.5 V V <sub>BOOT</sub> = 4.5 to 30 V, T <sub>A</sub> = -40 to 85 °C	Limits			Unit
			Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>	
<b>Power Supplies</b>						
V <sub>DD</sub> Supply	V <sub>DD</sub>		4.5			μA
I <sub>DD</sub> Supply	I <sub>DD1(en)</sub>	SD = H, IN = H, V <sub>S</sub> = 0 V			1000	
I <sub>DD</sub> Supply	I <sub>DD2(en)</sub>	SD = H, IN = L, V <sub>S</sub> = 0 V			500	
I <sub>DD</sub> Supply	I <sub>DD3(dis)</sub>	SD = L, IN = X, V <sub>S</sub> = 0 V			5	
I <sub>DD</sub> Supply	I <sub>DD4(en)</sub>	SD = H, IN = X, V <sub>S</sub> = 25 V, V <sub>BOOT</sub> = 30 V			200	
I <sub>DD</sub> Supply	I <sub>DD5(dis)</sub>	SD = L, IN = X, V <sub>S</sub> = 25 V, V <sub>BOOT</sub> = 30 V			5	
I <sub>DD</sub> Supply	I <sub>DD(en)</sub>	F <sub>IN</sub> = 300 kHz, SD = High, Driving Si4412DY		9		mA
	I <sub>DD(dis)</sub>	F <sub>IN</sub> = 300 kHz, SD = Low, Driving Si4412DY		3		μA
Boot Strap Current	I <sub>BOOT</sub>	V <sub>BOOT</sub> = 30 V, V <sub>S</sub> = 25 V, V <sub>OUTH</sub> = High	0.9		3	mA
<b>Reference Voltage</b>						
Break-Before-Make Reference Voltage	V <sub>BBM</sub>		1.1		3	V
<b>Logic Inputs (SD, IN)</b>						
Input High	V <sub>IH</sub>		0.7 × V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
Input Low	V <sub>IL</sub>		-0.3		0.3 × V <sub>DD</sub>	
<b>Undervoltage Lockout</b>						
V <sub>DD</sub> Undervoltage	V <sub>UVL</sub>	V <sub>DD</sub> Rising	3.7		4.3	V
V <sub>DD</sub> Undervoltage Hysteresis	V <sub>HYST</sub>			0.4		

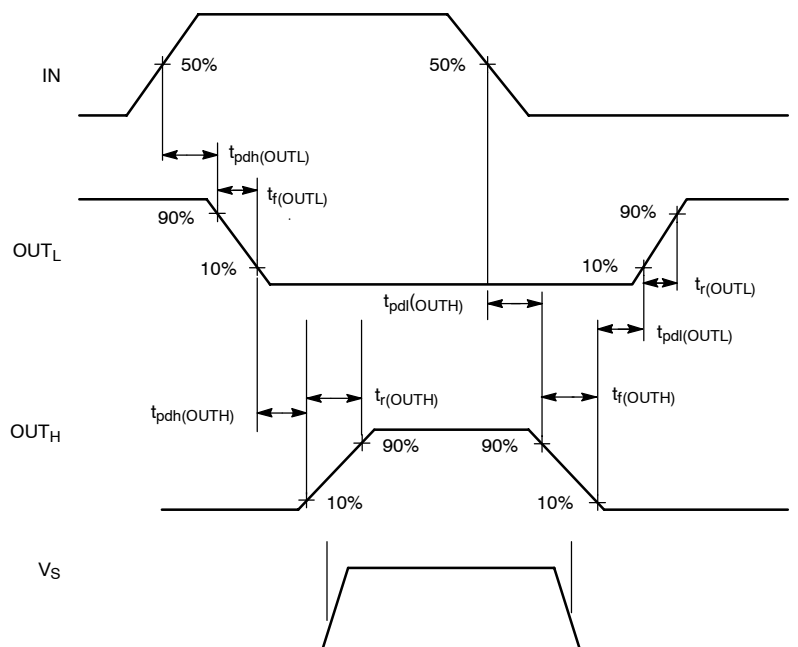


SPECIFICATIONS						
Parameter	Symbol	Test Conditions Unless Specified $V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$ $V_{BOOT} = 4.5 \text{ to } 30 \text{ V}, T_A = -40 \text{ to } 85^\circ\text{C}$	Limits			Unit
			Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>	
<b>Bootstrap Diode</b>						
Diode Forward Voltage	$V_{FD1}$	Forward Current = 100 mA		0.8	1	V
<b>Output Drive Current</b>						
OUT <sub>H</sub> Source Current	$I_{OUT(H+)}$	$V_{BOOT} - V_S = 3.7 \text{ V}, V_{OUTH} - V_S = 2 \text{ V}$			-0.4	A
OUT <sub>H</sub> Sink Current	$I_{OUT(H-)}$	$V_{BOOT} - V_S = 3.7 \text{ V}, V_{OUTH} - V_S = 1 \text{ V}$	0.4			
OUT <sub>L</sub> Source Current	$I_{OUT(L+)}$	$V_{DD} = 4.5 \text{ V}, V_{OUTL} = 2 \text{ V}$			-0.4	
OUT <sub>L</sub> Sink Current	$I_{OUT(L-)}$	$V_{DD} = 4.5 \text{ V}, V_{OUTL} = 1 \text{ V}$	0.6			
<b>Timing (<math>C_{LOAD} = 3 \text{ nF}</math>)</b>						
OUT <sub>L</sub> Off Propagation Delay	$t_{pd(OUTL)}$	$V_{DD} = 4.5 \text{ V}$		30		ns
OUT <sub>L</sub> On Propagation Delay	$t_{pdh(OUTL)}$				20	
OUT <sub>H</sub> Off Propagation Delay	$t_{pd(OUTH)}$	$V_{BOOT} - V_S = 4.5 \text{ V}$		30		
OUT <sub>H</sub> On Propagation Delay	$t_{pdh(OUTH)}$				20	
OUT <sub>L</sub> Turn On Time	$t_r(OUTL)$	OUT <sub>L</sub> = 10 to 90%		25		
OUT <sub>L</sub> Turn Off Time	$t_f(OUTL)$	OUT <sub>L</sub> = 90 to 10%		25		
OUT <sub>H</sub> Turn On Time	$t_r(OUTH)$	OUT <sub>H</sub> - $V_S$ = 10 to 90%		30		
OUT <sub>H</sub> Turn Off Time	$t_f(OUTH)$	OUT <sub>H</sub> - $V_S$ = 90 to 10%		20		

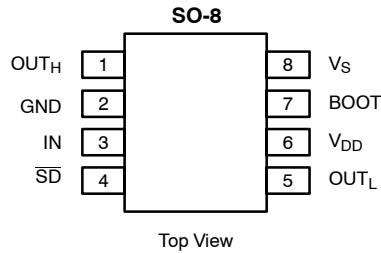
Notes

- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**TIMING WAVEFORMS**



**PIN CONFIGURATION**



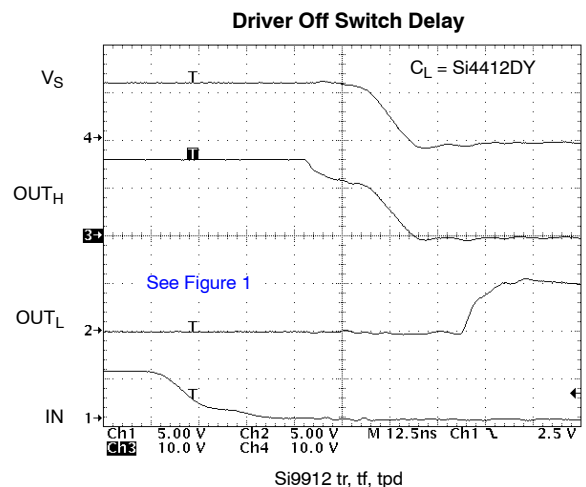
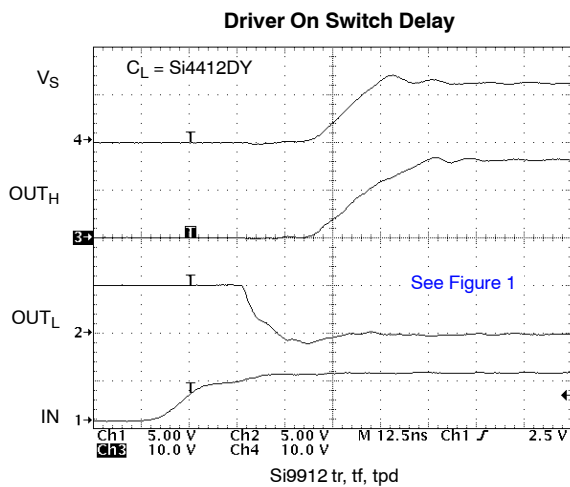
**PIN DESCRIPTION**

Pin Number	Name	Function
1	OUT <sub>H</sub>	Output drive for upper MOSFET.
2	GND	Ground supply
3	IN	CMOS level input signal. Controls both output drives.
4	$\overline{SD}$	Shutdown pin
5	OUT <sub>L</sub>	Output drive for lower MOSFET.
6	V <sub>DD</sub>	Input power supply
7	BOOT	Floating bootstrap supply for the upper MOSFET
8	V <sub>S</sub>	Floating GND for the upper MOSFET. V <sub>S</sub> is connected to the buck switching node and the source side of the upper MOSFET.

ORDERING INFORMATION		
Part Number	Temperature Range	Package
Si9912DY	-40 to 85°C	Bulk
Si9912DY-T1		Tape and Reel
Si9912DY-T1—E3 (Lead (Pb)-Free)		

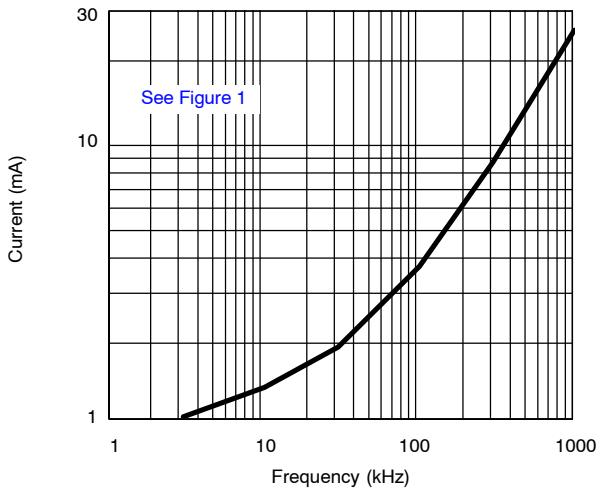
Eval Kit	Temperature Range	Board Type
Si9912DB	-40 to 85°C	Surface Mount

**TYPICAL WAVEFORMS**

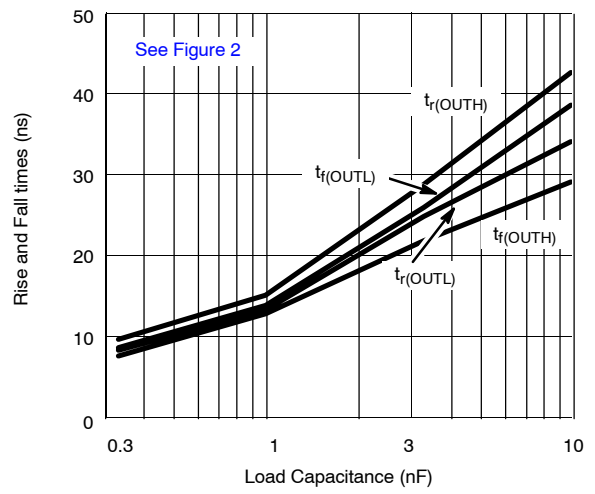


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

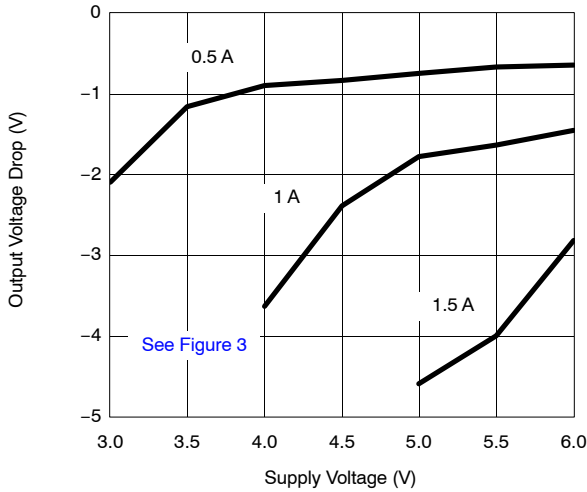
**$I_{DD}$  Supply Current vs. Frequency**



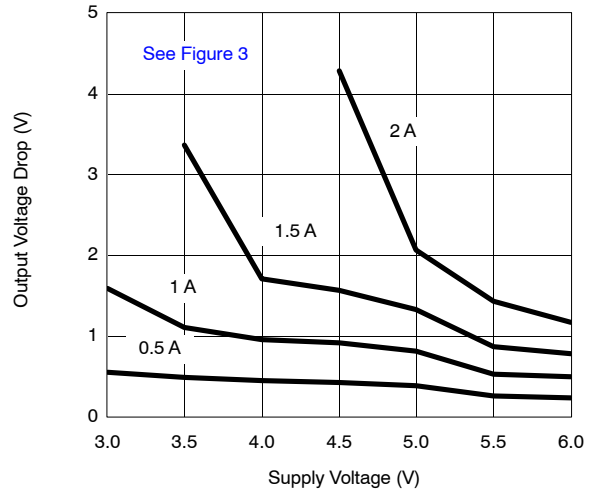
**Rise and Fall Time vs.  $C_{LOAD}$**



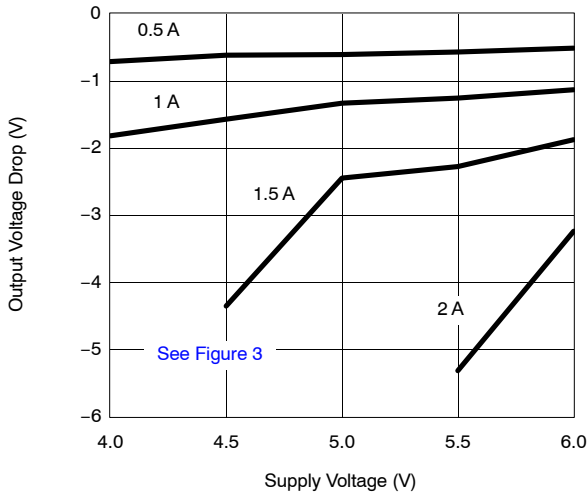
**$V_{OUT(H+)}$  vs. Supply**



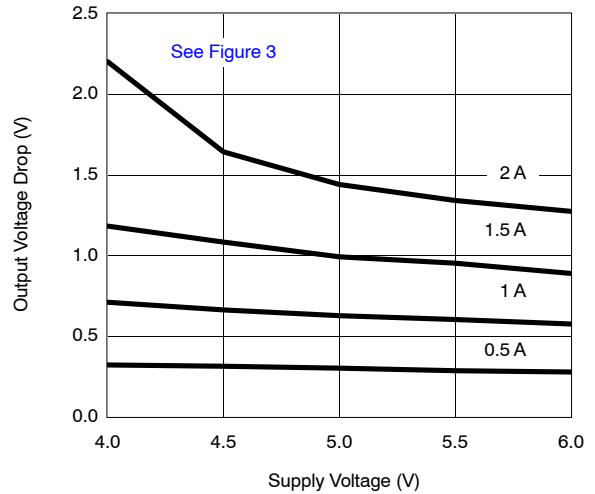
**$V_{OUT(H-)}$  vs. Supply**

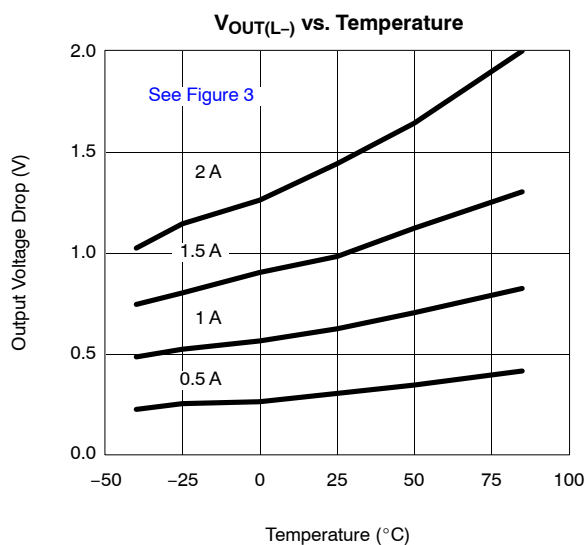
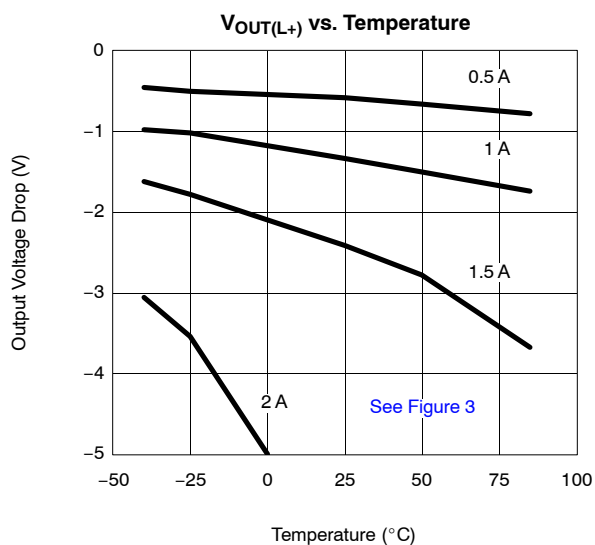
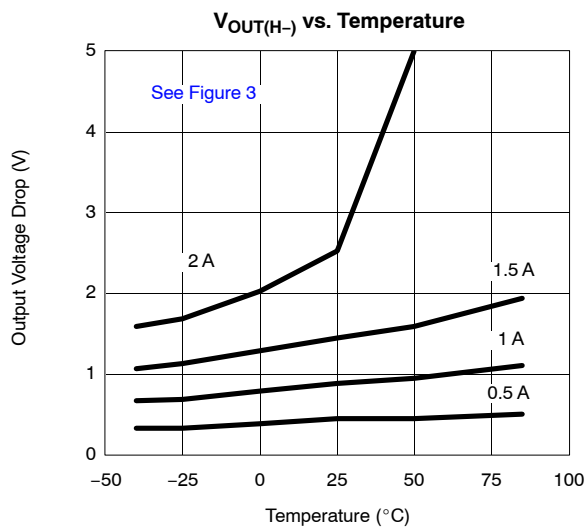
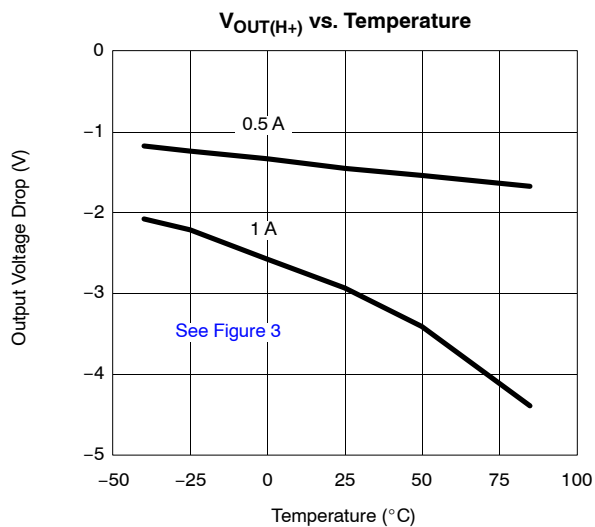


**$V_{OUT(L+)}$  vs. Supply**



**$V_{OUT(L-)}$  vs. Supply**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

**THEORY OF OPERATION**
**Break-Before-Make Function**

The Si9912 has an internal break-before-make function to ensure that both high-side and low-side MOSFETs are not turned on at the same time. The high-side drive (OUT<sub>H</sub>) will not turn on until the low-side gate drive voltage (measured at the OUT<sub>L</sub> pin) is less than V<sub>B<sub>BM</sub></sub>, thus ensuring that the low-side MOSFET is turned off. The low-side drive (OUT<sub>L</sub>) will not turn on until the voltage at the MOSFET half-bridge output (measured at the V<sub>S</sub> pin) is less than V<sub>B<sub>BM</sub></sub>, thus ensuring that the high-side MOSFET is turned off.

**Under Voltage Lockout Function**

The Si9912 has an internal under-voltage lockout feature to prevent driving the MOSFET gates when the supply voltage (at V<sub>DD</sub>) is less than the under-voltage lockout specification (V<sub>UVL</sub>). This prevents the output MOSFETs from being turned on without sufficient gate voltage to ensure they are fully on. There is hysteresis included in this feature to prevent lockout from cycling on and off.

**Bootstrap Supply Operation**  
(see Functional Block Diagram)

The power to drive the high-side MOSFET (Q2) gate comes from the bootstrap capacitor ( $C_{BOOT}$ ). This capacitor charges through D1 during the time when the low-side MOSFET is on ( $V_S$  is at GND potential), and then provides the necessary charge to turn on the high-side MOSFET.  $C_{BOOT}$  should be sized to be greater than ten times the high-side MOSFET gate capacitance, and large enough to supply the bootstrap current ( $I_{BOOT}$ ) during the high-side on time, without significant voltage droop.

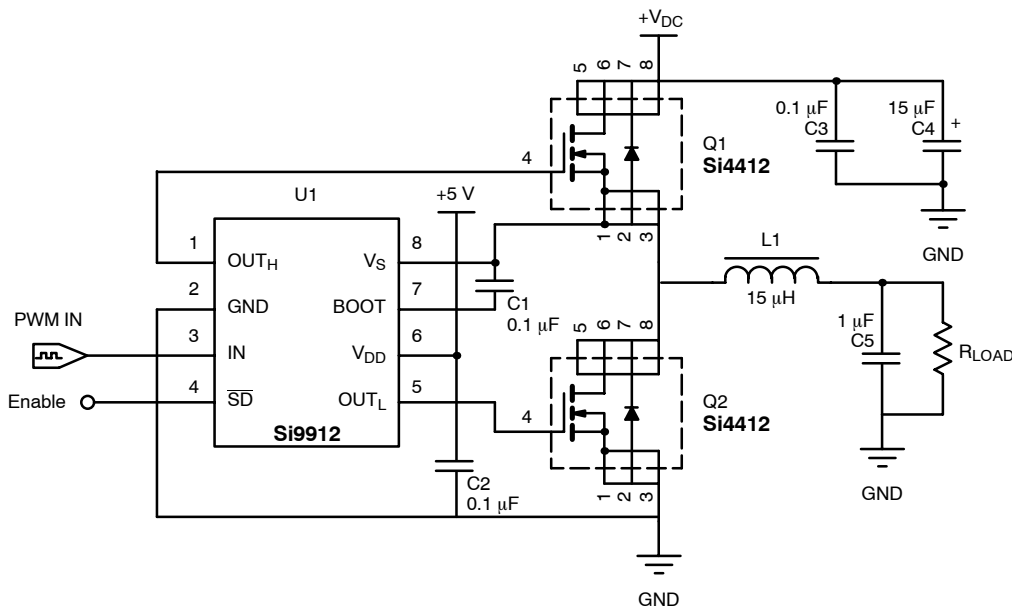
**Shutdown ( $\overline{SD}$ )**  
(shutdown input, active low)

When this pin is high, the IC operates normally. When this pin is low, both high- and low-side MOSFETs are turned off.

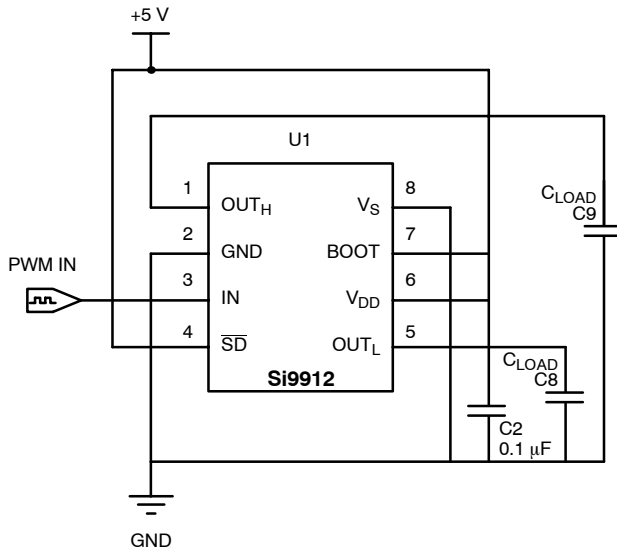
**Layout Considerations**

There are a few critical layout considerations for these parts. Firstly, the IC must be decoupled as closely as possible to the power pins. Secondly the IC should be placed physically close to the high- and low-side MOSFETs it is driving. The major consideration is that the MOSFET gates must be charged or discharged in a few nanoseconds, and the peak current to do this is of the order of 1 A. This current must flow from the decoupling and bootstrap capacitors to the IC, and from the output driver pin to the MOSFET gate, returning from the MOSFET source to the IC. The aim of the layout is to reduce the parasitic inductance of these current paths as much as possible. This is accomplished by making these traces as short as possible, and also running trace and its current return path adjacent to each other.

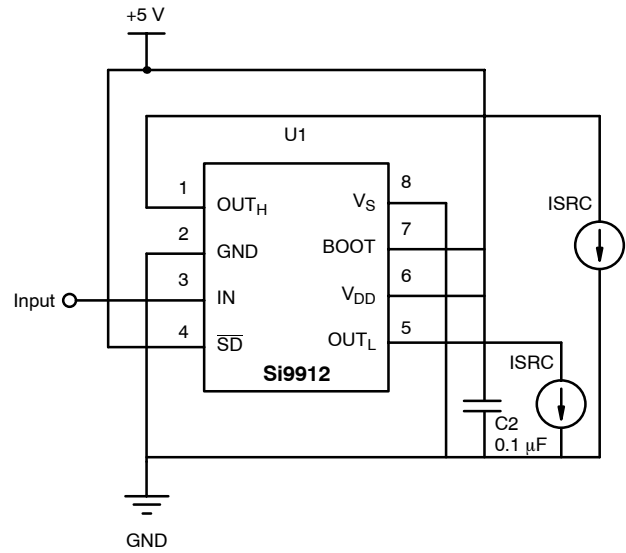
**APPLICATIONS**



**FIGURE 1.** Typical Applications Schematic Circuit Used to Obtain Typical Rising and Falling Switching Waveforms



**FIGURE 2.** Capacitive Load Test Circuit Used to Measure Rise and Fall Times vs. Capacitance

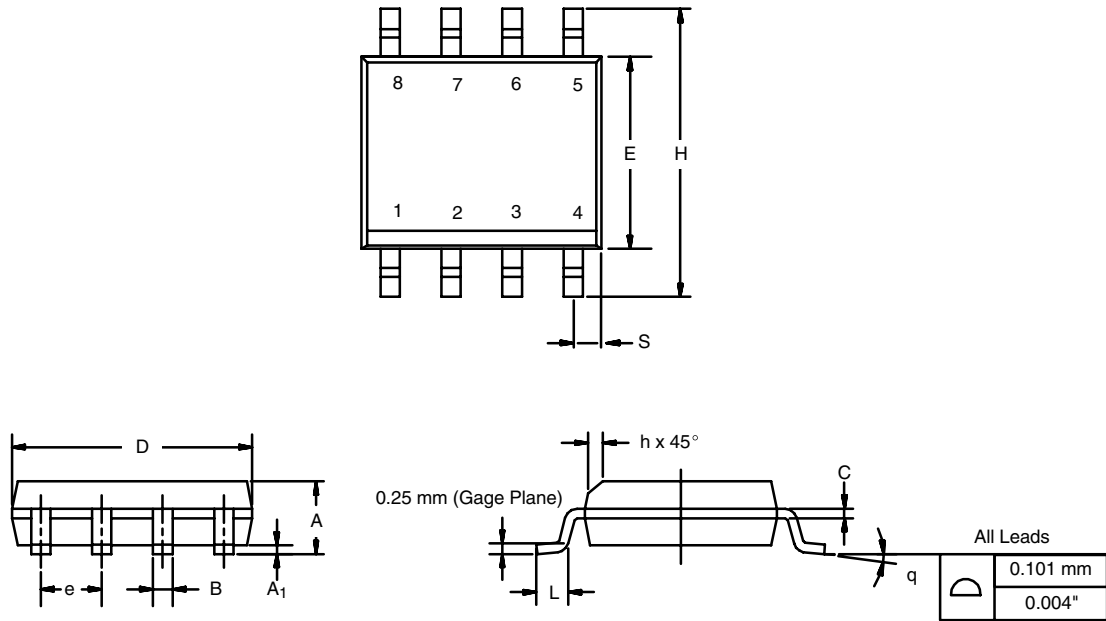


**FIGURE 3.** Load Test Schematic Circuit Used to Measure Driver Output Impedance



## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				



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