EFM32ZG Errata

This document contains information on the EFM32ZG errata. The latest available revision of this device is revision B.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from package marking or electronically.

Errata effective date: March 2021.

1. Errata Summary

The table below lists all known errata for the EFM32ZG and all unresolved errata in revision B of the EFM32ZG.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision:	
			A	B
ADC_E118	Requirements for ADC_CLK > 7 MHz	Yes	X	X
CMU_E115	HFRCO 1 MHz Band Switching	Yes	X	X
DI_E103	Flash Page Size	Yes	X	X
EMU_E107	Interrupts During EM2 Entry	Yes	X	X
EMU_E109	Potential Brown Out in EM2	Yes	X	X
EMU_E110	Potential Hard Fault when Exiting EM2 or EM3	Yes	X	—
IDAC_E101	IDAC Output Current Degradation	Yes	X	X
PCNT_E102	PCNT Pulse Width Filtering Does Not Work	No	X	X
RMU_E101	POR Calibration Initialization Issue	Yes	X	—
RMU_E102	Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers	Yes	X	—
RMU_E103	Reset May Fail to Trigger During Supply Voltage Brownouts	Yes	X	—
TIMER_E103	Capture/Compare Output is Unreliable with RSSCOIST Enabled	No	X	X
USART_E113	IrDA Modulation and Transmission of PRS Input Data	Yes	X	X

2. Current Errata Descriptions

2.1 ADC_E118 — Requirements for ADC_CLK > 7 MHz

Description of Errata
If operating the ADC_CLK at frequencies greater than 7 MHz, the ADC_BIASPROG register default value of 0x747 may not be sufficient to achieve the published missing codes performance specification.
Affected Conditions / Impacts
Devices operating the ADC_CLK at frequencies greater than 7 MHz while using the default ADC_BIASPROG value of 0x747 may experience performance outside data sheet limits.
Workaround
For systems requiring an ADC_CLK rate > 7 MHz, it may be necessary to increase the ADC's bias current components via the COMPBIAS, BIASPROG, and/or HALFBIAS bit fields in the ADC_BIASPROG register depending on a given application's ADC performance requirements.
Resolution
There is currently no resolution for this issue.

2.2 CMU_E115 — HFRCO 1 MHz Band Switching

Description of Errata
Switching to or from the 1 MHz band of the HFRCO or AUXHFRCO may cause a hard fault even at the maximum supported number of wait states.
Affected Conditions / Impacts
When the HFRCO or AUXHFRCO is selected as a clock source (e.g., the HFRCO has been selected as the HFCLK source) and the device is running with the maximum supported number of wait states, switching to or from the 1 MHz band can possibly cause a clock glitch that results in unexpected behavior or a hard fault.
Workaround
Before switching to or from the 1 MHz band when the HFRCO or AUXHFRCO is selected as the clock source, first switch to another stable clock source (such as the LFRCO). For example, when switching from the 21 MHz band to the 1 MHz band, the following procedure needs to be followed: 1. Select another stable clock source by writing to the HFCLKSEL field of the CMU_CMD register. 2. Wait until the clock source shows that it has been selected in the CMU_STATUS register, (e.g., CMU_STATUS_LFRCOSEL = 1). 3. Program the CMU_HFRCOCTRL register to select the 1 MHz band and tuning value. 4. Wait until the HFRCO has stabilized at the new frequency by waiting for the HFRCORDY bit in the CMU_STATUS register to change for 0 to 1. 5. Select the HFRCO as the clock source by writing to the HFCLKSEL field of the CMU_CMD register.
Resolution
There is currently no resolution for this issue.

2.3 DI_E103 — Flash Page Size

Description of Errata
The MEM_INFO_PAGE_SIZE value stored in the Device Information (DI) Page is incorrect.
Affected Conditions / Impacts
For devices with PROD_REV values of 23 or lower, the MEM_INFO_PAGE_SIZE register value in the Device Information Page is incorrect.
Workaround
Use fixed flash page size of 1024 bytes.
Resolution
There is currently no resolution for this issue.

2.4 EMU_E107 — Interrupts During EM2 Entry

Description of Errata
An interrupt from a peripheral running from the high frequency clock that is received during EM2 entry will cause the EMU to ignore the SLEEPDEEP flag.
Affected Conditions / Impacts
During EM2 entry, the high frequency clocks that are disabled during EM2 will run for some clock cycles after WFI is issued to allow safe shutdown of the peripherals. If an enabled interrupt is requested from one of these non-EM2 peripherals during this shutdown period, the attempt to enter EM2 will fail, and the device will enter EM1 instead. As a result, the pending interrupt will immediately wake the device to EM0.
Workaround
Before entering EM2, disable all high frequency peripheral interrupts in the core.
Resolution
There is currently no resolution for this issue.

2.5 EMU_E109 — Potential Brown Out in EM2

Description of Errata
There is an error with the calibration algorithm for a voltage regulator that is active during EM2 mode.
Affected Conditions / Impacts
There is an error with the calibration algorithm for a voltage regulator that is active during EM2 mode. This error can, in rare instances, cause the device to brown out and reset while operating in EM2 mode.
Workaround
The issue has been corrected with an updated and validated test program. Devices with a date code greater than or equal to 1626 have been tested with the corrected test program. Firmware can also work around this issue by writing the calibration value for the low current regulator active in EM2 to 0x6 after any reset or wakeup from EM4. More information on this firmware workaround including example code can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2016/11/04/emu_e109_-_potential-gBa3
Resolution
The issue has been corrected with an updated and validated test program. Devices with a date code and PROD_REV greater than or equal to 1626 and 0x8B respectively have been tested with the corrected test program.

2.6 IDAC_E101 — IDAC Output Current Degradation

Description of Errata
The current output of the IDAC might degrade over time.
Affected Conditions / Impacts
Due to an undefined shut-down state of the IDAC, powered devices that do not use the IDAC continuously might experience some degradation in the current output over the lifetime of the device. The degradation is very small when the device is used at room temperature, but the output current will fall well outside specs if the device is exposed to higher temperatures for longer periods of time.
Workaround
If the IDAC output current stability is crucial to the application, the IDAC should never be completely disabled while the device is powered. Leaving the IDAC enabled in the lowest output code setting with duty-cycling enabled consumes ~50 nA extra current and eliminates the problem.
Resolution
There is currently no resolution for this issue.

2.7 PCNT_E102 — PCNT Pulse Width Filtering Does Not Work

Description of Errata
PCNT pulse width filtering does not work.
Affected Conditions / Impacts
The PCNT pulse width filter does not work as intended.
Workaround
Do not use the pulse width filter, i.e., ensure FILT = 0 in PCNTn_CTRL.
Resolution
There is currently no resolution for this issue.

2.8 TIMER_E103 — Capture/Compare Output is Unreliable with RSSCOIST Enabled

Description of Errata
The TIMER capture/compare output is unreliable when RSSCOIST is enabled and the clock is prescaled.
Affected Conditions / Impacts
When RSSCOIST is set and PRESC > 0 in TIMERn_CTRL, the capture/compare output value is not reliable.
Workaround
Do not use a prescaled clock, i.e., ensure PRESC = 0 in TIMERn_CTRL when RSSCOIST is enabled.
Resolution
There is currently no resolution for this issue.

2.9 USART_E113 — IrDA Modulation and Transmission of PRS Input Data

Description of Errata
If the USART IrDA modulator is configured to accept input from a PRS channel, the incoming data stream will not be transmitted because the required clock from the baud rate generator is never enabled.
Affected Conditions / Impacts
It is not possible for the USART IrDA modulator to directly transmit data from a source other than the USART's own transmitter. The USART_IRCTRL_IRPRSEN bit should remain at its reset state of 0.
Workaround
Assuming the data to be sent via the PRS is also data that could be received by the EFM32/EFR32 USART, then the data can be received using the USART's PRS RX feature (USART_INPUT_RXPRS = 1), stored in RAM (e.g., using DMA), and then transmitted with IrDA mode enabled. In cases where IrDA operation is transmit-only, the PRS RX data can be received on the same USART doing the transmission. If IrDA operation is bidirectional, then another USART must be used to receive the PRS data. If the data to be sent is in some other format (e.g., pulses from a timer output), then there is no direct way to transmit it using the IrDA modulator. It would be necessary to capture the data in some other way and reformat it as serial data timed according to the clock generated by the USART.
Resolution
There is currently no resolution for this issue.

3. Resolved Errata Descriptions

This section contains previous errata for EFM32ZG devices.

For errata on the latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 EMU_E110 — Potential Hard Fault when Exiting EM2 or EM3

Description of Errata
The flash is powered down in EM2 and EM3 to save power. Some control registers in the flash can rarely enter an invalid state upon power-on, causing the first read of flash to be incorrect. If this occurs after exiting EM2 or EM3, the core attempts to fetch the interrupt address, but the value will be incorrect and may be invalid. In the case of an invalid value, the core will then jump to the hard fault handler for attempting to execute code from an invalid address. All subsequent reads from the flash are unaffected, and it is only the first flash read after exit from EM2 or EM3 that is potentially erroneous.
Affected Conditions / Impacts
When exiting EM2 or EM3, some devices may intermittently execute code incorrectly or enter the hard fault handler instead of entering the expected ISR associated with the wake source.
Workaround
To workaround this issue, move the interrupt vector table and interrupt service routines for EM2 or EM3 wake sources to RAM and perform a dummy read of the flash in the ISR. Additional information on the workaround and examples provided is available from the following Knowledge Base article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2017/05/09/emu_e110_-_potential-i2Pn
Resolution
This issue has been resolved. Devices with a date code greater than or equal to 1742 will not have this issue.

3.2 RMU_E101 — POR Calibration Initialization Issue

Description of Errata
Upon initial power-on, some devices may not be able to access flash memory above the 4 kB boundary, or some calibration registers on some devices may not be set to their factory calibration values.
Affected Conditions / Impacts
The list of affected devices can be found in the Knowledge Base (KB) article listed under Fix/Workaround. Some devices are sensitive to the power supply ramp during initial power-on. Specific ramp profiles on these devices can cause an intermittent issue resulting in one of two failure modes (A) or (B): A. Flash memory above the 4 kB boundary is inaccessible. Reads of the flash will return zeros. Write attempts will return an invalid address error code in the MSC_STATUS register. Code execution will behave as though the memory above 4 kB was filled with zeros until the device resets itself. B. Some parts of the calibration initialization process do not complete successfully. On USB devices, the USB voltage regulator does not get calibrated. Specific peripheral registers that may not be calibrated are as follows (not all registers apply to all devices): ADC0_CAL, IDAC_CAL, DAC0_CAL, DAC0_BIASPROG, DAC0_OPACTRL, and DAC0_OPAOFFSET. A SYSRESETREQ reset will clear either failure mode, and the device will behave normally until the next power-on event.
Workaround
Additional information including a software workaround is available from the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2015/10/09/rmu_e101_-_por_calib-cEpZ
Resolution
Devices with a date code and PROD_REV greater than or equal to 1537 and 0x89 respectively will not have this issue.

3.3 RMU_E102 — Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers

Description of Errata
Output of the on-chip regulator (DECOUPLE pin) may be approximately 0 V, and the device will not respond to a pin reset.
Affected Conditions / Impacts
The device supply voltage is specified as 1.98 V minimum. For certain supply waveforms, similar to disconnecting a battery, allowing the supply to decay to approximately 0.9 V (and stopping the decay at approximately 0.9 V), then reconnecting the battery, the output of the regulator (DECOUPLE pin) may be approximately 0 V. In this state, code will not execute, and the device will not respond to a pin reset. More information on this issue can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e102_por_bodres-AQh7
Workaround
Hold the RESETn pin logic low, starting before the supply is disconnected, and keep RESETn pin logic low until the supply reaches a valid voltage. If the DECOUPLE pin measures approximately 0 V, power cycle the supplies by pulling them all the way to 0 V before connecting supplies again.
Resolution
This issue is resolved in revision B devices.

3.4 RMU_E103 — Reset May Fail to Trigger During Supply Voltage Brownouts

Description of Errata
Reset may fail to trigger when the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range.
Affected Conditions / Impacts
If the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range, the device may fail to reset, allowing code execution while the supply voltage remains in the 1.25 - 1.45 V range. More information on this issue can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e103_por_bodres-N3MD
Workaround
Hold the RESETn pin in logic low, starting before the device supplies fall below 1.6 V, and keep the RESETn pin logic low until the device supplies reach a valid voltage again.
Resolution
This issue is resolved in revision B devices.

4. Revision History

Revision 0.80

March, 2021
- Added ADC_E118.
- Added CMU_E115

Revision 0.70

September, 2019
- Updated to product revision B.
- Resolved DI_E103, EMU_E109, RMU_E101, RMU_E102, and RMU_E103.
- Migrated to new errata document format.

Revision 0.60

January, 2019
- Added EMU_E107, RMU_E102, RMU_E103, and USART_E113.
- Resolved EMU_E110.
- EMU_E109 and RMU_E101 workaround URLs updated.

Revision 0.50

July, 2017
- Updated EMU_E110 to refer to both EM2 and EM3.

Revision 0.40

April, 2017
- Added EMU_E110.
- Updated errata formatting.
- Merged all errata documents for EFM32ZG devices into one document.
- Merged errata history and errata into one document.

Revision 0.30

August, 2016
- Added EMU_E109.

Revision 0.20

October, 2015
- Added DI_E103, PCNT_E102, RMU_E101, and TIMER_E103.

Revision 0.10

November, 2013
- Initial preliminary release.

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