

Buck DC/DC Converter for Energy Harvester with Adjustable Maximum Power Point Control, Adjustable Output Voltage and PG Function Evaluation Board

No. EEV-422-K001A-201014

R1801K001A-EV is the evaluation board for R1801 which has the below features, benefits and specification.

OVERVIEW

R1801K is a power-storing buck DC/DC converter for a photovoltaic and vibration energy harvester. The Power Good (PG) function can output PG signal according to the output voltage facilitating to build a system. A low operating quiescent current allows a harvester to be used under a low-illumination environment, and it is suitable for an equipment with low power supplied from a harvester.

KEY BENEFITS

- Providing a low power supply (I_Q 200 nA) and a high efficiency (approximately 80% @ 10 μ A).
- Monitoring the output voltage to output Power Good (PG) signal.
- Adjustable output voltage and maximum power point control voltage by pin setting.

KEY SPECIFICATIONS

- Input Voltage Range: 2.3 V to 5.5 V
- Output Voltage Range: 2.8 V
- Maximum Power Point Control Voltage Range: 3.7 V
- Output Voltage Accuracy: $\pm 3.0\%$
- Operating Quiescent Current: Typ. 200 nA ($T_a = 25^\circ\text{C}$, at no load)
under condition of $V_{IN} = 4\text{ V}$, $V_{OUT} = 3.0\text{ V}$
- Starting Power: 1 μ W ($V_{IN} = 4\text{ V}$, $V_{OUT} = 3.0\text{ V}$)
- Reverse Current Protection ($V_{IN} \geq 2.0\text{ V}$)
- Adjustable Maximum Power Point Control, Adjustable Output Voltage
- PG Function
- For more details on R1801 IC, please refer to
<https://www.n-redc.co.jp/en/pdf/datasheet/r1801-ea.pdf>

PART NUMBER INFORMATION

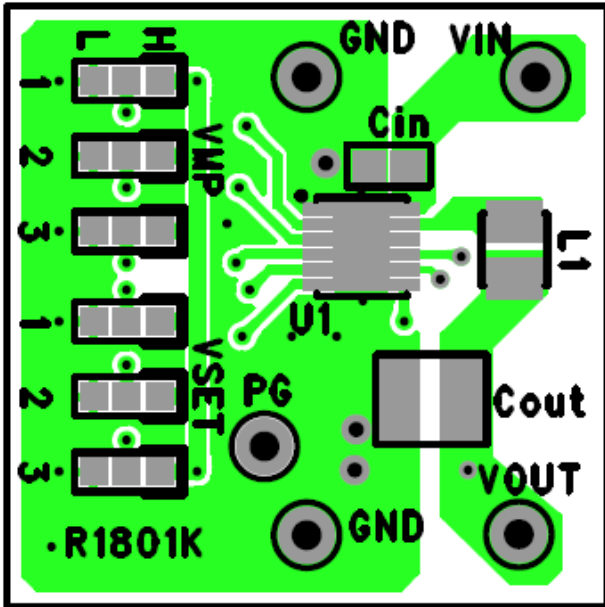
Product Name	Package
R1801K001A-EV	DFN(PLP)2730-12

001: The set output voltage (V_{SET}) = 2.8 V,
The set maximum power point control voltage (V_{MPSET}) = 3.7 V

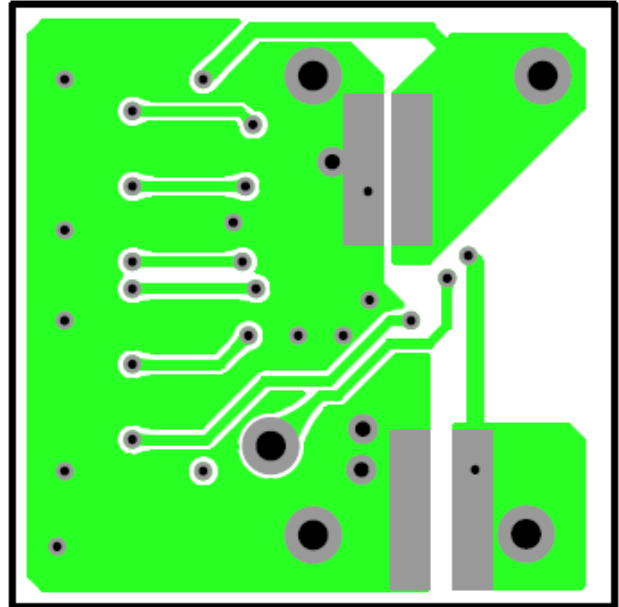
A: Fixed

PCB LAYOUT

R1801KxxxA-TR (PKG: DFN(PLP)2730-12)



Top Layer



Bottom Layer

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Pin Voltage	-0.3 to 6.5	V
V_{LX}	LX Pin Voltage	-0.3 to $V_{IN} + 0.3$	V
V_{VFB}	VFB Pin Voltage	-0.3 to 6.5	V
V_{VMP1}	VMP1 Pin Voltage	-0.3 to 6.5	V
V_{VMP2}	VMP2 Pin Voltage	-0.3 to 6.5	V
V_{VMP3}	VMP3 Pin Voltage	-0.3 to 6.5	V
V_{VSET1}	VSET1 Pin Voltage	-0.3 to 6.5	V
V_{VSET2}	VSET2 Pin Voltage	-0.3 to 6.5	V
V_{VSET3}	VSET3 Pin Voltage	-0.3 to 6.5	V
V_{PG}	Power Good Pin	-0.3 to 6.5	V
P_D	Power Dissipation	Refer to Appendix "POWER DISSIPATION"	
T_j	Junction Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	2.3 to 5.5	V
T_a	Operating Temperature Range	-40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

The specifications surrounded by are guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$.

R1801K Electrical Characteristics

($T_a = 25^{\circ}\text{C}$)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	$V_{\text{IN}} \geq V_{\text{SET}} + 0.5 \text{ V}$, $V_{\text{SET1-3}} = \text{"L"}$, at no load	$\frac{V_{\text{SET}}}{\times 0.97}$		$\frac{V_{\text{SET}}}{\times 1.03}$	V
I_{Q}	Operating Quiescent Current	$V_{\text{IN}} = 5.0 \text{ V}$, $V_{\text{VFB}} = 3.0 \text{ V}$, device not switching VFB pin current is converted by V_{IN} current		200	420	nA
V_{MP}	Accuracy of Maximum Power Point Control Voltage	$V_{\text{VFB}} = 0 \text{ V}$	-200		200	mV
$I_{\text{VMP1 to 3}}$	VMP1 to 3 Pin H/L Leakage Current	$V_{\text{IN}} = 5.5 \text{ V}$, $V_{\text{VMP1 to 3}} = 5.5 \text{ V} / 0 \text{ V}$			0.1	uA
$I_{\text{VSET1 to 3}}$	VSET1 to 3 Pin H/L Leakage Current	$V_{\text{IN}} = 5.5 \text{ V}$, $V_{\text{VSET1 to 3}} = 5.5 \text{ V} / 0 \text{ V}$			0.1	uA
I_{LEAK}	Output Driver H/L Leakage Current	$V_{\text{IN}} = 5.5 \text{ V}$, $V_{\text{LX}} = 5.5 \text{ V} / 0 \text{ V}$			0.1	uA
ΔV_{MP}	VMP Adjustment Resolution			100		mV
ΔV_{SET}	VSET Adjustment Resolution			100		mV

All test items listed under Electrical Characteristics are done under the pulse load condition ($T_j \approx T_a = 25^{\circ}\text{C}$).
Test circuit is operated with "Open Loop Control" (GND = 0 V), unless otherwise specified.

PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS

The specifications surrounded by are guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$.

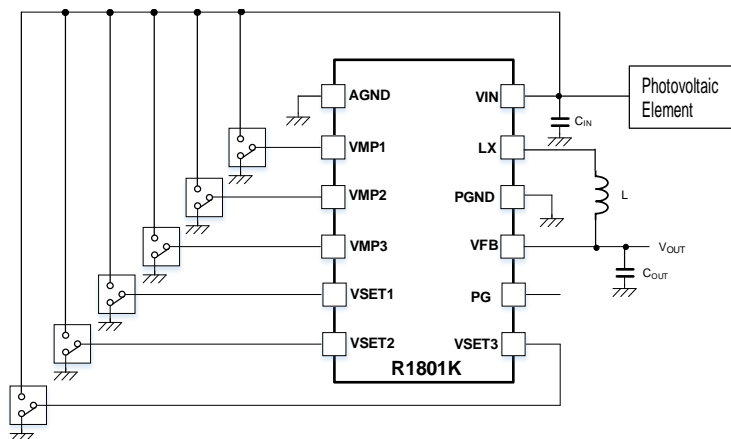
Product Name	V_{SET} ($V_{\text{SET1-3}} = \text{"L"}$) [V]			V_{MP} ($V_{\text{MP1-3}} = \text{"L"}$) [V]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
R1801K001A	2.716	2.8	2.884	3.500	3.7	3.900

* Please contact us for setting voltages other than those listed above.

* When use the PG function, put the V_{SET} voltage 2.5 V or higher.

* It is recommended to set as $V_{\text{MP}} > V_{\text{SET}} + 0.5\text{V}$ or higher.

TYPICAL APPLICATION CIRCUIT



Recommended External Components⁽¹⁾

Symbol	Value
C _{IN}	10 μF
C _{OUT}	47 μF
L	22 μH

VMP1~3 = L VMP = 3.7 V

VSET1~3 = L VSET = 2.8 V

R1801K Typical Application Circuit

ADJUSTABLE MAXIMUM POWER POINT CONTROL / OUTPUT VOLTAGE

When the pin voltage of VMP1 to 3 and VSET1 to 3 is H, the maximum power voltage and VSET voltage are adjustable externally. 1 corresponds to +100 mV, 2 corresponds to +200 mV and 3 corresponds to -300 mV, and TYP. ± 300 mV is adjustable. However, setting all bits to H is a prohibited.

Due to the circuit configuration, the H / L level threshold voltage of each pin depends on the input voltage.

When using H voltage, it is recommended to pull up both of VMPPC / VSET to the input voltage.

Use the L voltage shorted to GND.

All adjustment pins should not be OPEN, use them as H / L levels.

Regulated Voltage Logic Table of Maximum Power Point Control Voltage

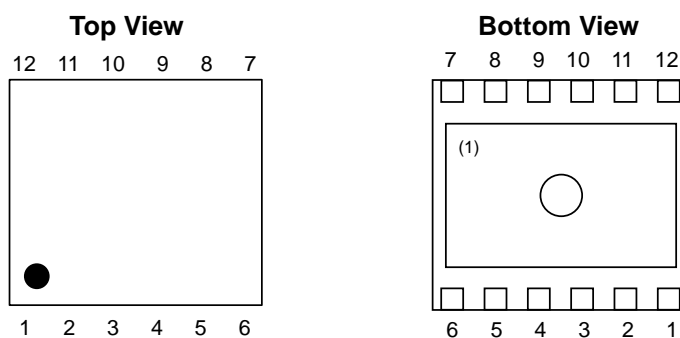
Regulated Voltage	VMP1	VMP2	VMP3
- 300 mV	H	H	L
- 200 mV	L	H	L
- 100 mV	H	L	L
0 mV	L	L	L
100 mV	L	H	H
200 mV	H	L	H
300 mV	L	L	H
Prohibited	H	H	H

Regulated Voltage Logic Table of Output Voltage

Regulated Voltage	VSET1	VSET2	VSET3
- 300 mV	H	H	L
- 200 mV	L	H	L
- 100 mV	H	L	L
0 mV	L	L	L
100 mV	L	H	H
200 mV	H	L	H
300 mV	L	L	H
Prohibited	H	H	H

⁽¹⁾The bill of materials will be attached on the shipment of each purchased evaluation board.

PIN DESCRIPTION



DFN (PLP) 2730-12 Pin Configuration

DFN(PLP)2730-12 Pin Description

Pin No.	Symbol	Description
1	AGND	Analog Ground Pin
2	VMP1	Maximum Power Point Control Voltage Adjustment Pin 1
3	VMP2	Maximum Power Point Control Voltage Adjustment Pin 2
4	VMP3	Maximum Power Point Control Voltage Adjustment Pin 3
5	VSET1	Output Voltage Adjustment Pin 1
6	VSET2	Output Voltage Adjustment Pin 2
7	VSET3	Output Voltage Adjustment Pin 3
8	PG	Power Good Pin
9	VFB	Output Voltage Pin
10	PGND	Power Ground Pin
11	LX	DC/DC Switching Pin
12	VIN	Pin for Connecting Photovoltaic Element

⁽¹⁾The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

- Using a ceramic capacitor with a lower equivalent series resistance (ESR) is recommended; a capacitor of 10 μF or higher for C_{IN} between VIN and GND pins, a capacitor of 47 μF or higher for C_{OUT} . Using a mass-storage device for C_{OUT} also is recommended. Please choose capacitors depending on the bias characteristics, V_{IN} and V_{OUT} . (Refer to *Recommended External Components*)
- Please choose inductors which have low direct-current resistance, enough allowable current and low magnetic saturation.
- When an intermediate voltage other than VIN or GND is input to the VMP1 to 3 and VSET1 to 3 pins, the supply current may increase due to the cross-conduction current of the IC internal logic circuit. When the VMP1 to 3 and VSET1 to 3 pins are open, the maximum power point control voltage and VSET voltage may vary. When using the IC, connect the VMP1 to 3 and VSET1 to 3 pins to "VIN" or "GND".



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