AK4380

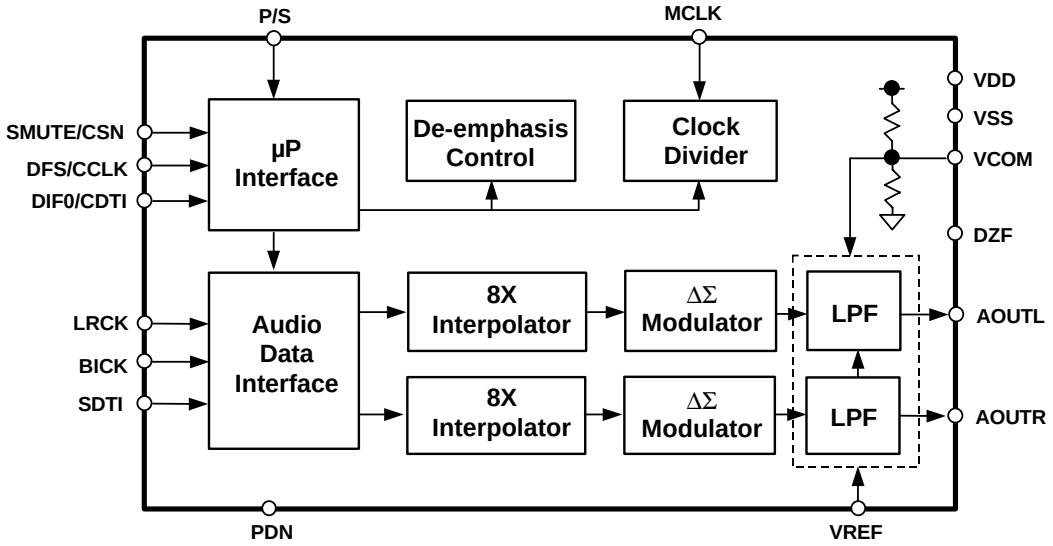
100dB 24Bit 96kHz 2ch DAC

GENERAL DESCRIPTION

The AK4380 offers the perfect mix for cost and performance based audio systems. Using AKM's multi bit architecture for its modulator the AK4380 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4380 integrates a combination of SCF and CTF filters, removing the need for high cost external filters and increasing performance for systems with excessive clock jitter. The 24 Bit word length and 96kHz sampling rate make this part ideal for a wide range of applications including DVD and AC-3 systems. The AK4380 is offered in a space saving 16pin TSSOP package.

FEATURES

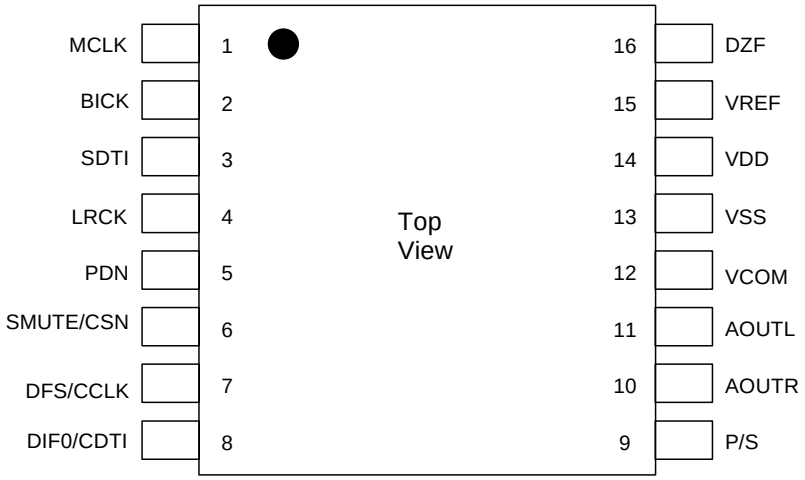
- **Sampling Rates Ranging from 8kHz to 96kHz**
- **128x Oversampling (Normal speed mode)**
- **64x Oversampling (Double speed mode)**
- **24Bit 8x FIR Digital Filter**
- **2nd order Analog LPF**
- **On chip Buffer with Single End Output**
- **Digital de-emphasis for 32k, 44.1k and 48kHz sampling**
- **Soft mute**
- **I/F format: 24bit MSB justified, 24/20/16bit LSB justified, I^2S**
- **Master clock: 256fs, 384fs, 512fs or 768fs (Normal speed mode)**
  128fs, 192fs, 256fs or 384fs (Double speed mode)
- **THD+N: -88dB**
- **Dynamic Range: 100dB**
- **High Tolerance to Clock Jitter**
- **Power supply: 4.5 to 5.5V**
- **Space Saving 16 Pin TSSOP (6.4mm x 5.0mm) Package**



■ Ordering Guide

AK4380VT	-40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4380	Evaluation Board for AK4380	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin
5	PDN	I	Power-Down Mode Pin When at "L", the AK4380 is in the power-down mode and is held in reset. The AK4380 should always be reset upon power-up.
6	SMUTE	I	Soft Mute Pin in parallel mode "H": Enable, "L": Disable
	CSN	I	Chip Select Pin in serial mode
7	DFS	I	Double Speed Sampling Mode Pin in parallel mode "L": Normal Speed, "H": Double Speed
	CCLK	I	Control Data Input Pin in serial mode
8	DIF0	I	Audio Data Interface Format Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial mode
9	P/S	I	Parallel/Serial Select Pin (Internal pull-up pin) "L": Serial control mode, "H": Parallel control mode
10	AOUTR	O	Rch Analog Output Pin
11	AOUTL	O	Lch Analog Output Pin
12	VCOM	O	Common Voltage Pin, VDD/2 Normally connected to VSS with a 0.1µF ceramic capacitor in parallel with a 10µF electrolytic cap.
13	VSS	-	Ground Pin
14	VDD	-	Power Supply Pin
15	VREF	I	Voltage Reference Input Pin
16	DZF	O	Data Zero Input Detect Pin When SDTI of both channels follow a total 8192 LRCK cycles with "0" input data, this spin goes to "H".

Note: All input pins except pull-up pin should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VDD	-0.3	6.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage	VIND	-0.3	VDD+0.3	V
Ambient Operating Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	4.5	5.0	5.5	V
Voltage Reference (Note 2)	VREF	3.0	-	VDD	V

Note: 2. Analog output voltage scales with the voltage of VREF.
AOUT (typ@0dB) = 3.4Vpp×VREF/5.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta = 25°C; VDD = 5.0V; fs = 44.1kHz at DFS = "0"; BICK = 64fs; Signal Frequency = 1kHz; 24bit Input Data; Measurement frequency = 20Hz ~ 20kHz at fs = 44.1kHz, 20Hz ~ 40kHz at fs = 96kHz; $R_L \geq 10k\Omega$; unless otherwise specified)

Parameter		min	typ	max	Units
Resolution				24	Bits
Dynamic Characteristics (Note 3)					
THD+N (0dB Output)	fs = 44.1kHz		-88	-82	dB
	fs = 96kHz		-86	-	dB
Dynamic Range (-60dB Output, A-weight)	fs = 44.1kHz	92	100		dB
	fs = 96kHz	-	93		dB
S/N (A-weight)	fs = 44.1kHz	92	100		dB
	fs = 96kHz	-	93		dB
Interchannel Isolation (1kHz)		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
DC Accuracy					
Gain Drift			100	-	ppm/°C
Output Voltage	(Note 4)	3.15	3.40	3.65	Vpp
Load Resistance		10			kΩ
Output Current				200	µA
Power Supplies					
Power Supply Current (VDD)					
Normal Operation (PDN = "H")			14	22	mA
Power-Down Mode (PDN = "L")	(Note 5)		10	100	µA
Power Supply Rejection	(Note 6)		40		dB

Notes: 3. Measured by Audio Precision (System Two). Refer to the evaluation board manual.
4. Full-scale voltage (0dB). Output voltage scales with the voltage of VREF,
AOUT (typ@0dB) = 3.4Vpp×VREF/5.
5. All digital inputs including clock pins (MCLK, BICK and LRCK) are held VDD or VSS.
6. PSR is applied to VDD with 1kHz, 100mV. VREF pin is held +5V.

FILTER CHARACTERISTICS

(Ta = 25°C; VDD = 4.5 ~ 5.5V; fs = 44.1kHz; DEM0 = "1", DEM1 = "0")

Parameter		Symbol	min	typ	max	Units
Digital filter						
Passband	±0.05dB (Note 7)	PB	0		20.0	kHz
	-6.0dB		-	22.05	-	kHz
Stopband	(Note 7)	SB	24.25			kHz
Passband Ripple		PR			± 0.02	dB
Stopband Attenuation		SA	54			dB
Group Delay	(Note 8)	GD	-	19.1	-	1/fs
Digital Filter + LPF						
Frequency Response	0 ~ 20.0kHz	FR	-	± 0.2	-	dB
	40.0kHz		-	± 0.3	-	dB

Notes: 7. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.
8. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta = 25°C; VDD = 4.5 ~ 5.5V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	2.2	-	-	V
Low-Level Input Voltage		VIL	-	-	0.8	V
High-Level Output Voltage	(Iout = -80μA)	VOH	VDD-0.4	-	-	V
Low-Level Output Voltage	(Iout = 80μA)	VOL	-		0.4	V
Input Leakage Current	(Note 9)	Iin	-	-	± 10	μA

Note: 9. P/S pin has internal pull-up device, normally 100kΩ.

SWITCHING CHARACTERISTICS

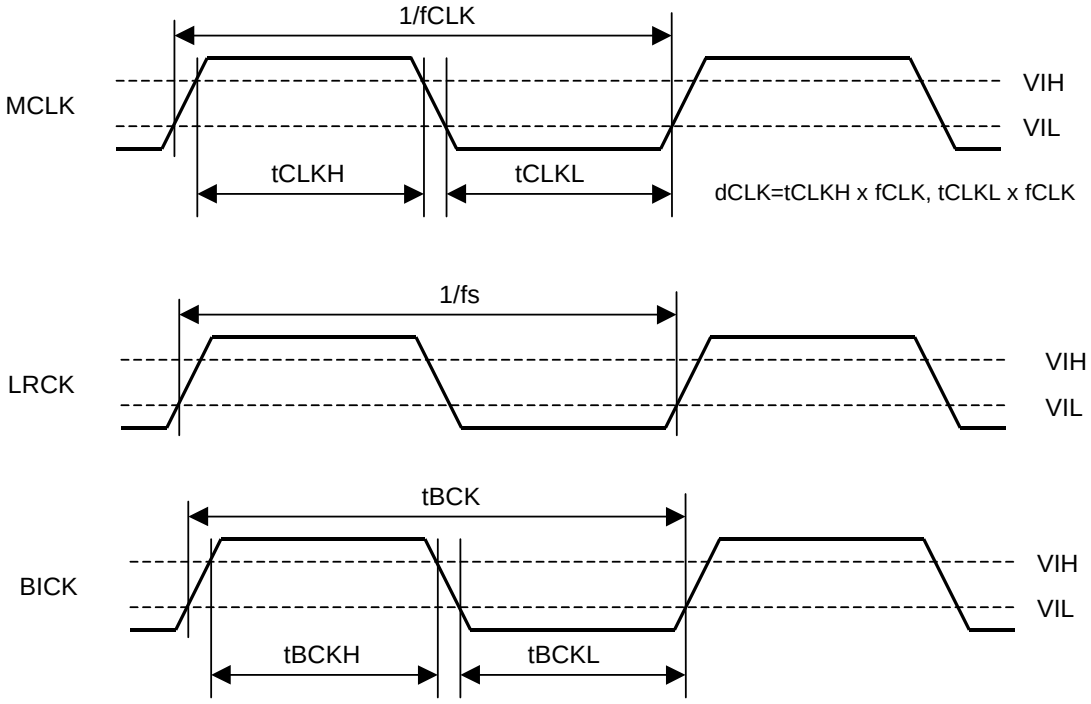
(Ta = 25°C; VDD = 4.5 ~ 5.5V; C_L = 20pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Frequency		fCLK	2.048	11.2896	36.864	MHz
Duty Cycle		dCLK	40		60	%
LRCK Frequency		fs	8	44.1	96	kHz
Duty Cycle		Duty	45		55	%
Audio Interface Timing						
BICK Period						
Normal Speed Mode		tBCK	1/128fs			ns
Double Speed Mode		tBCK	1/64fs			ns
BICK Pulse Width Low		tBCKL	70			ns
Pulse Width High		tBCKH	70			ns
BICK "↑" to LRCK Edge	(Note 10)	tBLR	40			ns
LRCK Edge to BICK "↑"	(Note 10)	tLRB	40			ns
SDTI Hold Time		tSDH	40			ns
SDTI Setup Time		tSDS	40			ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	40			ns
CDTI Hold Time		tCDH	40			ns
CSN High Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Reset Timing						
PDN Pulse Width	(Note 11)	tPD	150			ns

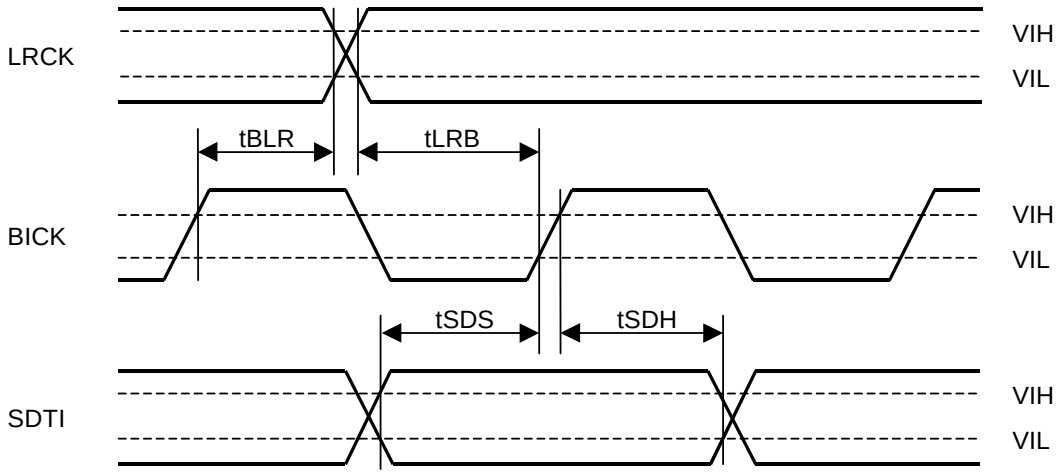
Notes: 10. BICK rising edge must not occur at the same time as LRCK edge.

11. The AK4380 can be reset by PDN= "L" upon power up.
If MCLK frequency or DFS changes, the AK4380 should be reset by PDN pin or RSTN bit.

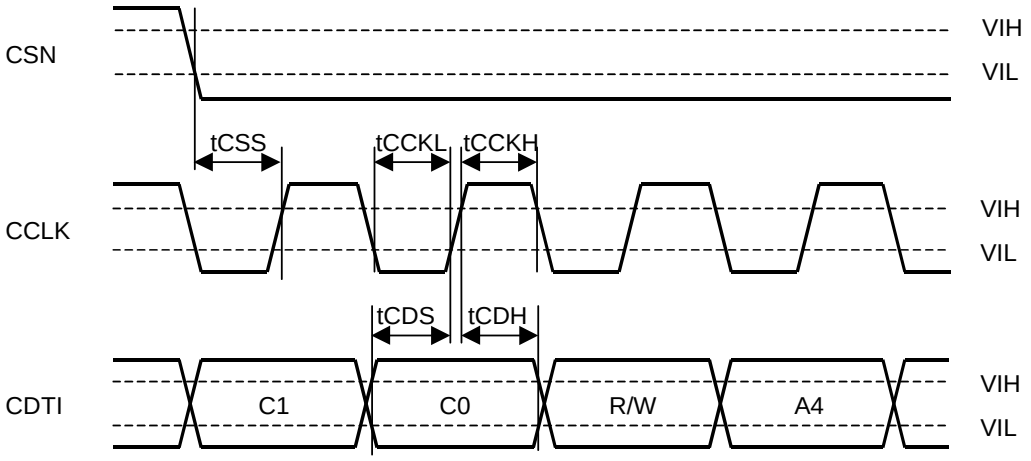
■ **Timing Diagram**



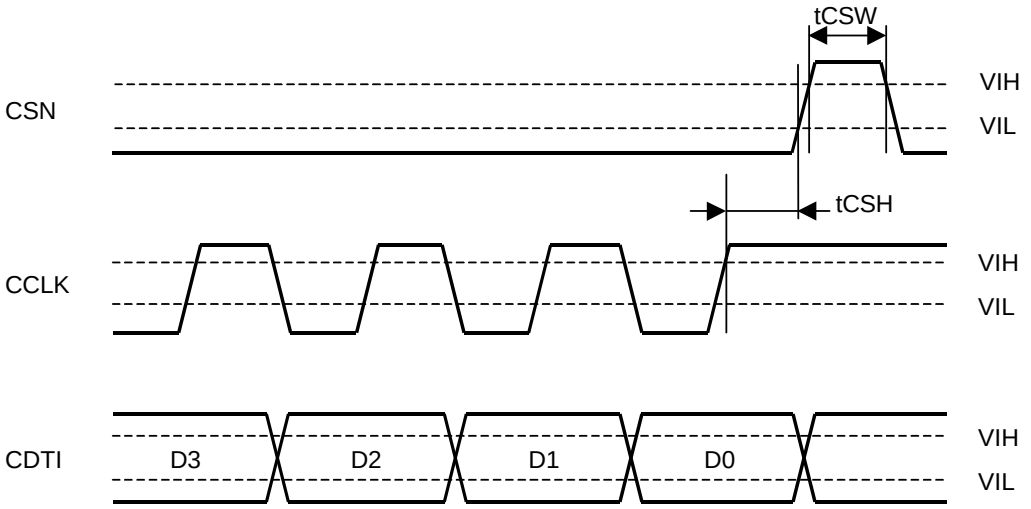
Clock Timing



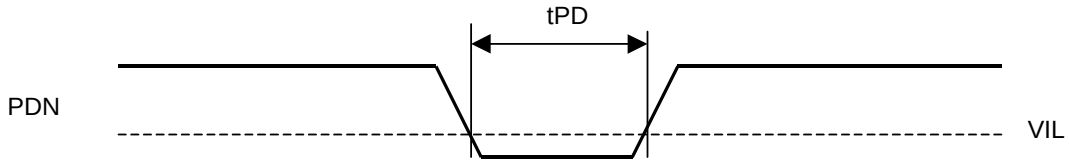
Serial Interface Timing



WRITE Command Input Timing



WRITE Data Input Timing



Power-down Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4380, are MCLK, LRCK and BICK. The master clock (MCLK) corresponds to 256fs, 384fs, 512fs or 768fs (for normal speed mode; 128fs, 192fs, 256fs or 384fs for double speed mode). MCLK frequency is automatically detected, and the internal master clock becomes 256fs (for normal speed mode; 128fs for double speed mode). The MCLK should be synchronized with LRCK but the phase is not critical. Table 1~3 illustrate corresponding clock frequencies.

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4380 is in the normal operation mode (PDN= "H"). If these clocks are not provided, the AK4380 may draw excess current because the device utilizes dynamic refreshed logic internally. The AK4380 should be reset by PDN= "L" after threse clocks are provided. If the external clocks are not present, the AK4380 should be in the power-down mode (PDN= "L"). After exiting reset at power-up etc., the AK4380 is in the power-down mode until MCLK and LRCK are input.

	Normal Speed Mode	Double Speed Mode
DFS pin / DFS bit	"L" / "0"	"H" / "1"
LRCK Frequency (fs)	8kHz~48kHz	8kHz~96kHz
MCLK Frequency	256fs,384fs,512fs,768fs	128fs,192fs,256fs,384fs

Table 1. System clock

LRCK	MCLK				BICK
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	3.0720MHz

Table 2. System clock example (Normal Speed Mode)

LRCK	MCLK				BICK
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 3. System clock example (Double Speed Mode)

■ Audio Serial Interface Format

Data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF0-2 bits as shown in Table 4 can select five formats in serial mode. In parallel mode, the DIF0 pin as shown Table 5 can select two formats. In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 16 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	SDTI Format	BICK	Figure	
0	0	0	0	16bit LSB Justified	≥32fs	Figure 1	
1	0	0	1	20bit LSB Justified	≥40fs	Figure 2	
2	0	1	0	24bit MSB Justified	≥48fs	Figure 3	
3	0	1	1	24bit I^2S Compatible	≥48fs	Figure 4	Default
4	1	0	0	24bit LSB Justified	≥48fs	Figure 2	

Table 4. Audio Data Formats (Serial mode)

Mode	DIF0	SDTI Format	BICK	Figure
2	0	24bit MSB Justified	≥48fs	Figure 3
3	1	24bit I^2S Compatible	≥48fs	Figure 4

Table 5. Audio Data Formats (Parallel mode)

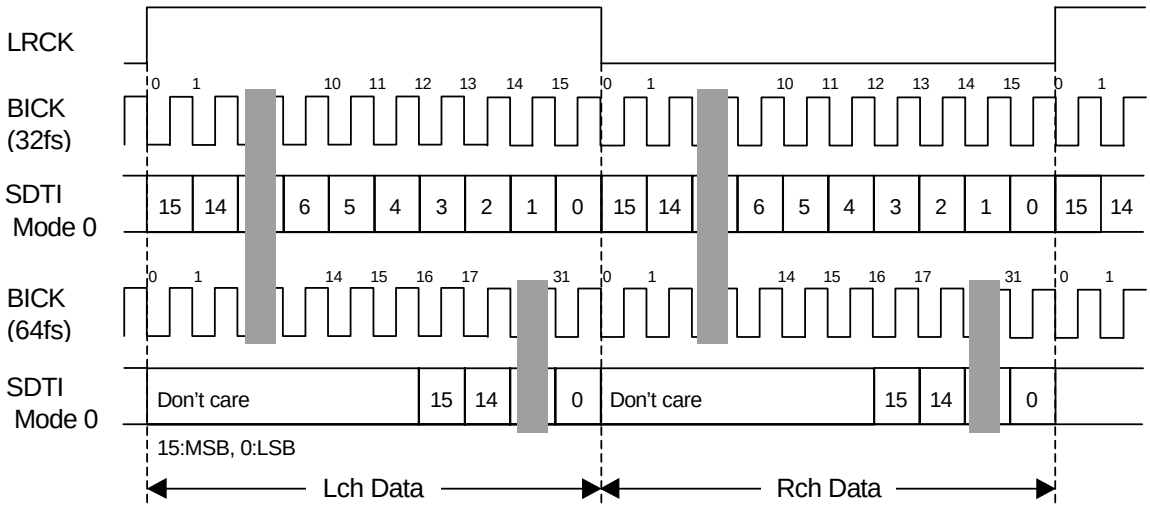


Figure 1. Mode 0 Timing

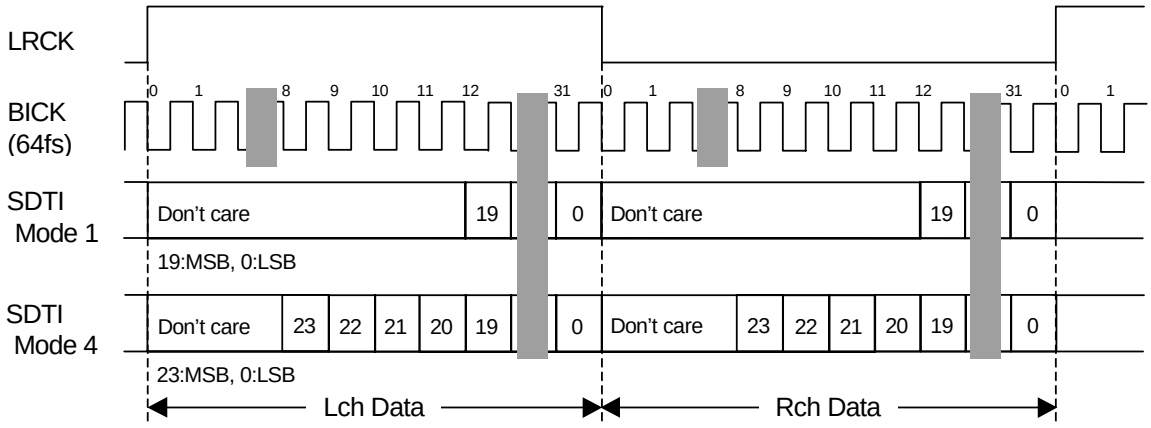


Figure 2. Mode 1,4 Timing

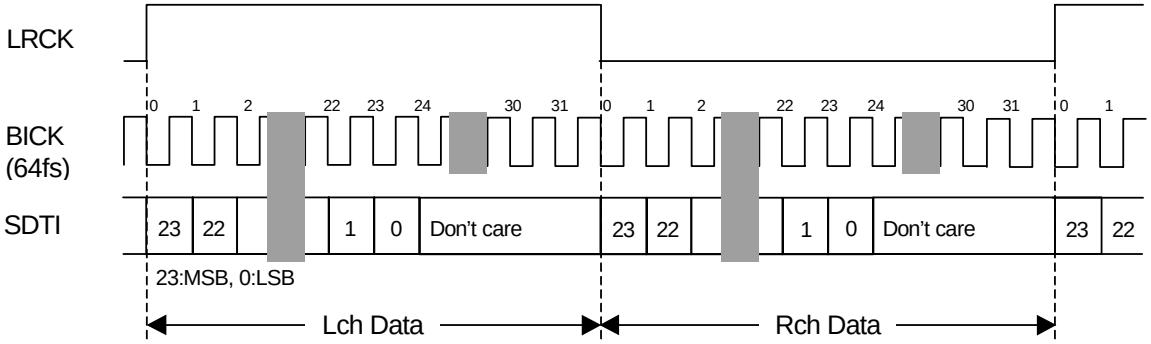


Figure 3. Mode 2 Timing

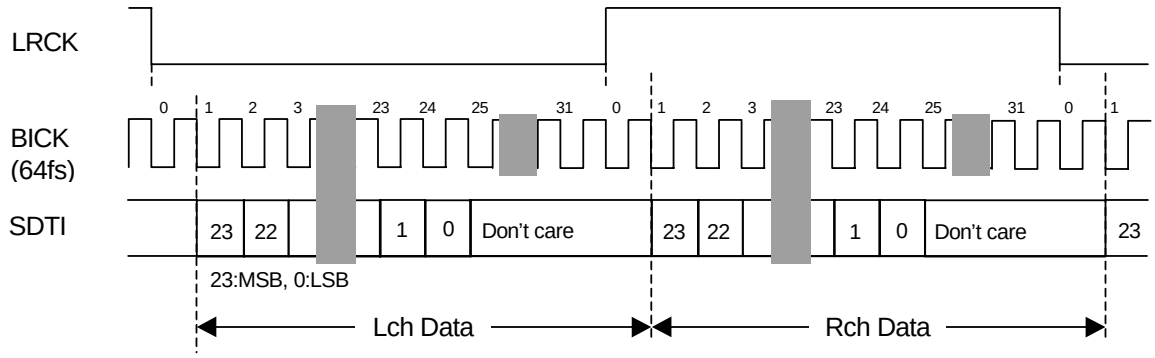


Figure 4. Mode 3 Timing

■ De-emphasis filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc = 50/15μs) and is controlled by the DEM0 and DEM1 bits regardless of the status of DFS.

DFS	DEM1	DEM0	Mode	
0	0	0	44.1kHz	
0	0	1	OFF	Default
0	1	0	48kHz	
0	1	1	32kHz	
1	0	0	44.1kHz	
1	0	1	OFF	
1	1	0	48kHz	
1	1	1	32kHz	

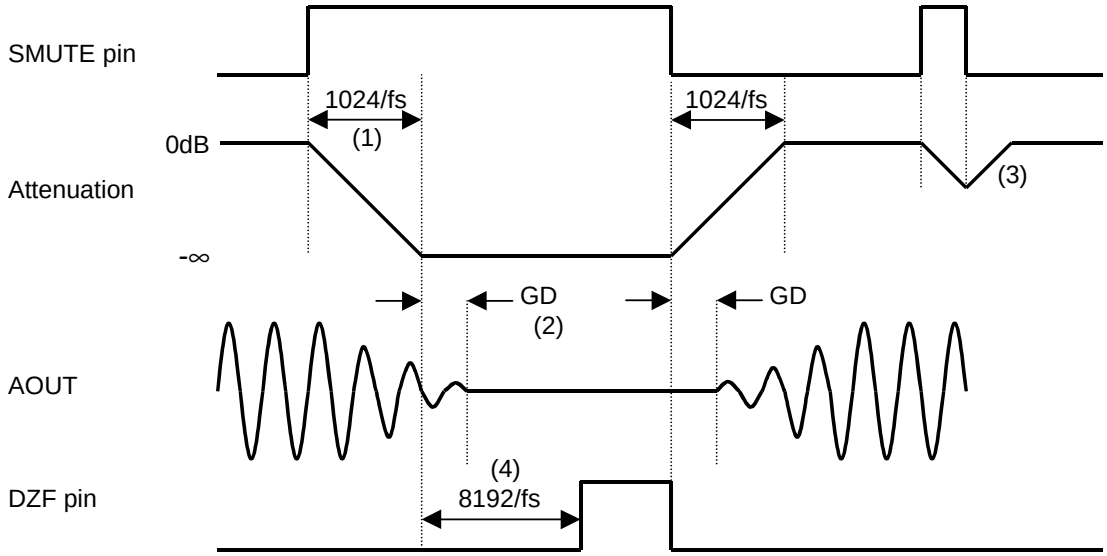
Table 6. De-emphasis filter control

■ Zero detection

When the input data at both channels is continuously zeros for 8192 LRCK cycles, DZF pin goes to “H”. DZF pin channel immediately goes to “L” if the input data is not zero after going DZF “H”. If RSTN bit is “0”, DZF pin goes to “H”. DZF pin goes to “L” at 4~5/fs after RSTN bit returns to “1”.

■ Soft mute operation

Soft mute operation is performed at digital domain. When the SMUTE pin goes to “H”, the output signal is attenuated by -∞ during 1024 LRCK cycles. When the SMUTE pin is returned to “L”, the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) The output signal is attenuated by -∞ during 1024 LRCK cycles (1024/fs).
(2) The analog output corresponding to the digital input has a group delay, GD.
(3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.
(4) When the input data at both channels is continuously zeros for 8192 LRCK cycles, DZF pin goes to “H”. DZF pin immediately goes to “L” if the input data is not zero after going DZF “H”.

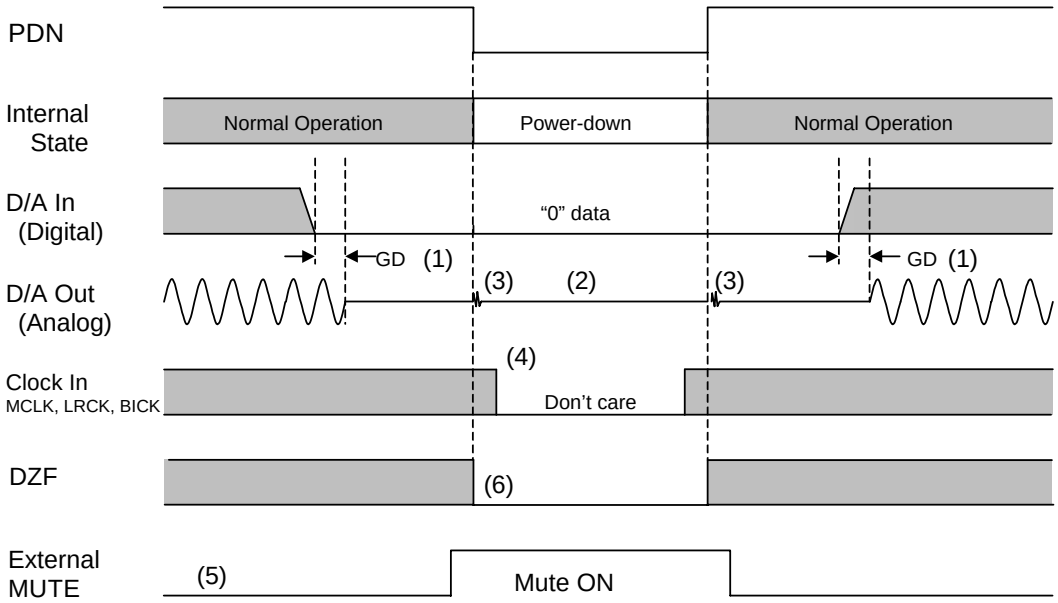
Figure 5. Soft mute and zero detection

■ System Reset

The AK4380 should be reset once by bringing PDN = "L" upon power-up. The AK4380 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4380 is in the power-down mode until MCLK and LRCK are input.

■ Power-down

The AK4380 is placed in the power-down mode by bringing PDN pin "L" and the anlog outputs are floating (Hi-Z). Figure 6 shows an example of the system timing at the power-down and power-up.



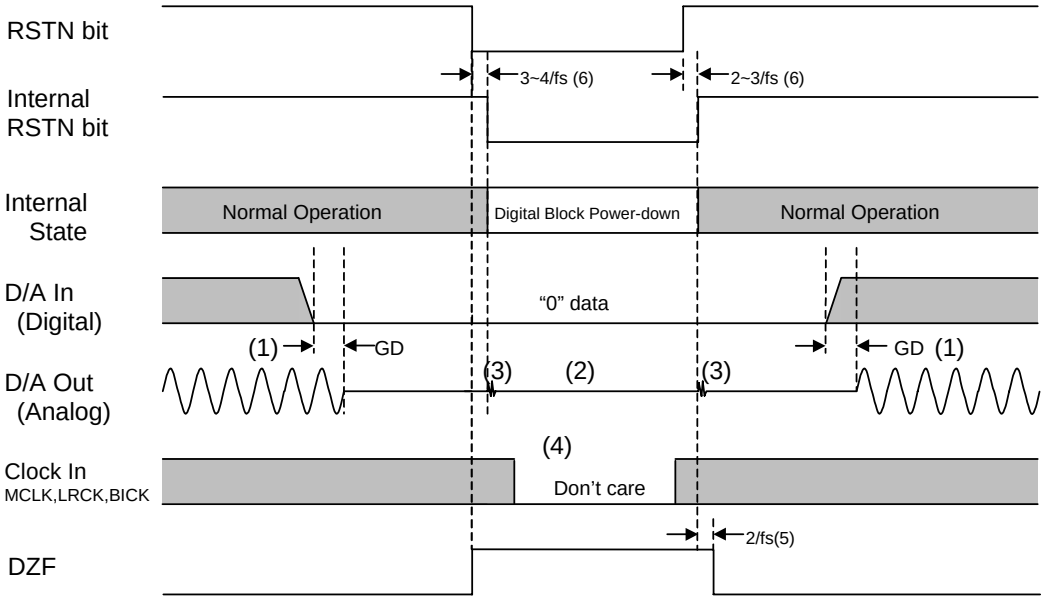
Notes:

(1) The analog output corresponding to the digital input has a group delay, GD.
(2) Analog outputs are floating (Hi-Z) at the power-down mode.
(3) Click noise occures at the edges("↑ ↓") of PDN signal. This noise is output even if input data is "0".
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = "L").
(5) Please mute the analog output externally if the click noise(3) influences system application. The timing example is shown in this figure.
(6) DZF pin is "L" in the power-down mode (PDN = "L").

Figure 6. Power-down/up sequence example

■ Reset Function

When RSTN = “0”, the AK4380’s digital section is powered down but the internal register values are not initialized. The analog outputs go to VCOM voltage and DZF pin goes to “H”. Figure 7 shows the example of reset by RSTN bit.



Notes:

(1) The analog output corresponding to the digital input has a group delay, GD.

(2) Analog outputs go to VCOM voltage.

(3) Click noise occurs at the edges(“↑ ↓”) of the internal timing of RSTN bit. This noise is output even if “0” data is input.

(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the reset mode (RSTN = “L”).

(5) DZF pin goes to “H” when the RSTN bit becomes to “0”, and goes to “L” at 2/fs after RSTN bit becomes to “1”.

(6) There is a delay, 3~4/fs from RSTN bit "0" to the internal RSTN bit “0”, and 2~3/fs from RSTN bit “1” to the internal RSTN “1”.

Figure 7. Reset sequence example

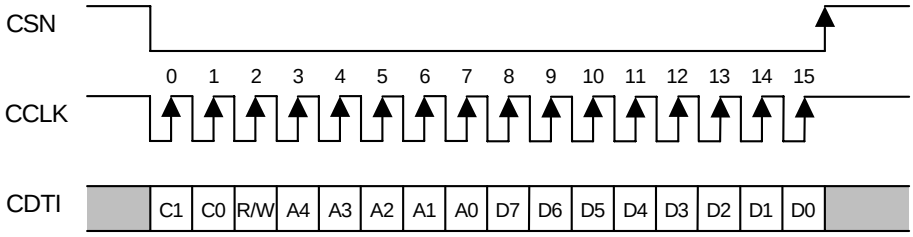
■ Mode Control Interface

Some function of AK4380 can be controlled by pins (parallel control mode) shown in Table 6. The serial control interface is enabled by the P/S pin = "L". Internal registers may be written by 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip Address (2bits, CAD1/0; fixed to "01"), Read/Write (1bit; fixed to "1", Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). AK4380 latches the data on the rising edge of CCLK, so data should clocked in on the falling edge. The writing of data becomes valid by CSN "↑". The clock speed of CCLK is 5MHz (max). The CSN and CCLK must be fixed to "H" when the register does not be accessed.

Function	Parallel mode	Serial mode
Double speed	O	O
De-emphasis	X	O
SMUTE	O	O
Zero Detection	O	O
16/20/24bit LSB justified format	X	O

Table 7. Function list (O: available, X: not available)

PDN = "L" resets the registers to their default values. When the state of P/S pin is changed, AK4380 should be reset by PDN= "L". In the serial mode, the internal timing circuit is reset by RSTN bit, but the registers are not initialized.



C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 8. Control I/F Timing

* The AK4380 does not support the read command and chip address. C1, C0 and R/W are fixed to "011"
* When the AK4380 is in the power down mode (PDN = "L") or the MCLK is not provided, writing into the control register is inhibited.

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	0	0	DIF2	DIF1	DIF0	PW	RSTN
01H	Control 2	0	0	0	0	DFS	DEM1	DEM0	SMUTE

Notes: For addresses from 02H to 1FH, data must not be written.
When PDN pin goes "L", the registers are initialized to their default values.
When RSTN bit goes "0", the only internal timing is reset and the registers are not initialized to their default values.
All data can be written to the register even if PW or RSTN bit is "0".

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	0	0	DIF2	DIF1	DIF0	PW	RSTN
default		0	0	0	0	1	1	1	1

RSTN: Internal timing reset control
0: Reset. All registers are not initialized.
1: Normal Operation
When MCLK frequency or DFS changes, the AK4380 should be reset by PDN pin or RSTN bit.

PW: Power down control
0: Power down. All registers are not initialized.
1: Normal Operation

DIF2-0: Audio data interface formats (see Table 4)
Initial: "011", Mode 3

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	0	0	DFS	DEM1	DEM0	SMUTE
default		0	0	0	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal operation
1: DAC outputs soft-muted

DEM1-0: De-emphasis Response Control (see Table 6)
Initial: "01", OFF

DFS: Sampling Speed Control (see Table 1)
0: Normal speed, 8kHz~48kHz
1: Double speed, 8kHz~96kHz

SYSTEM DESIGN

Figure 9 and 10 show the system connection diagram. An evaluation board (AKD4380) is available in order to allow an easy study on the layout of a surrounding circuit.

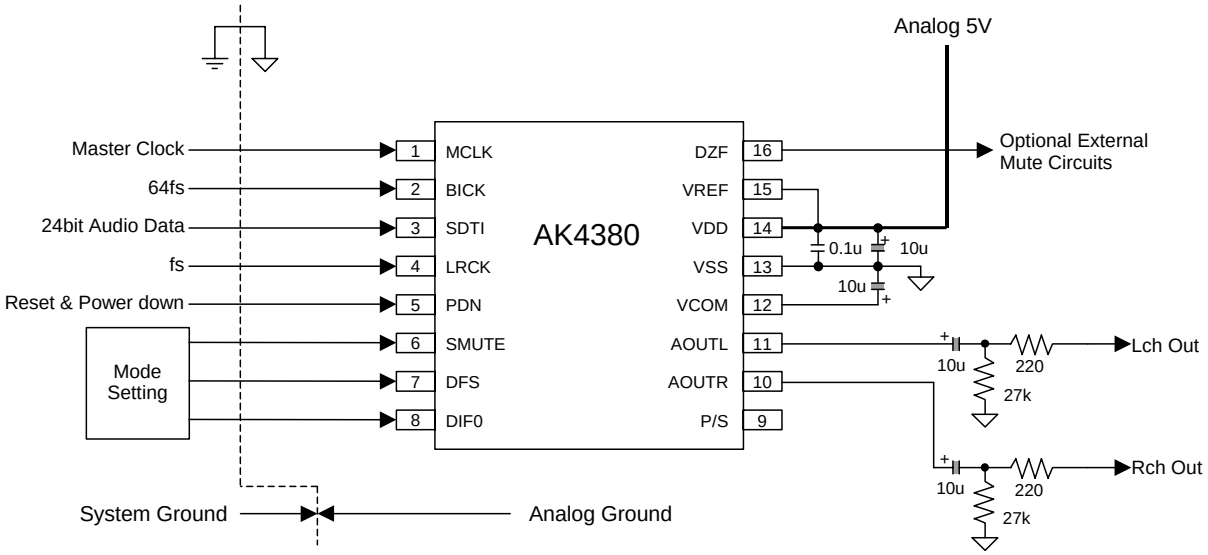


Figure 9. Typical Connection Diagram (Parallel mode)

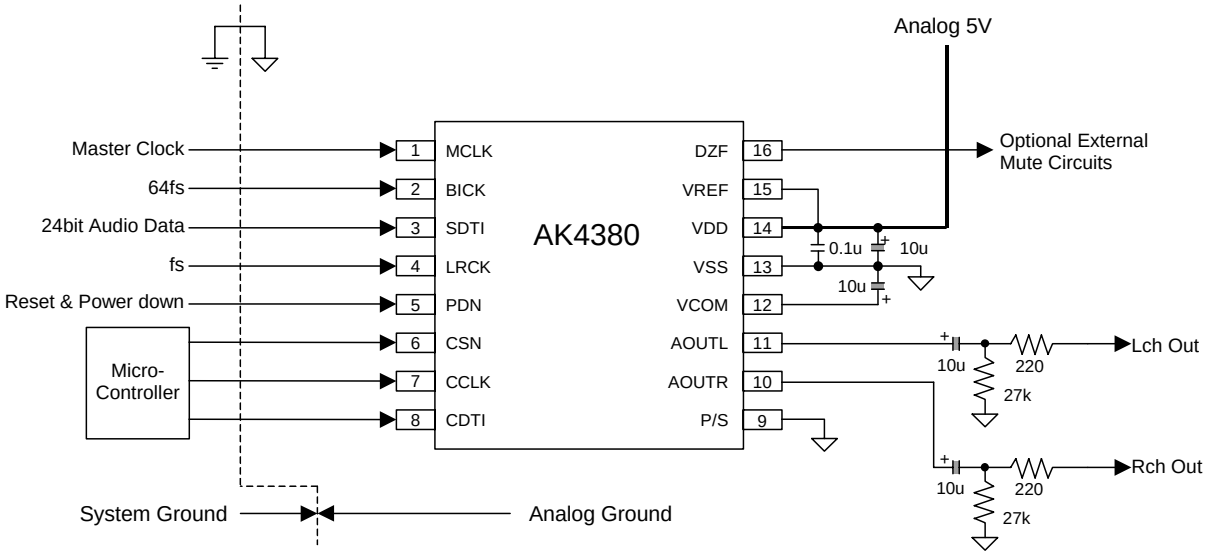


Figure 10. Typical Connection Diagram (Serial mode)

Notes:

- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and the load.
- ALL input pins except internal pull-up pin should not be left floating.
- Decoupling capacitor, especially 0.1µF ceramic capacitor for high frequency should be placed as near to VDD and VREF pins as possible.
- System ground including DSP/µP should be separated from AK4380's VSS. Both grounds should be connected by one point at power supply or regulator on system board.

1. Grounding and Power Supply Decoupling

VDD and VSS are supplied from analog supply and should be separated from system digital supply. Decoupling capacitor, especially 0.1μF ceramic capacitor for high frequency should be placed as near to VDD as possible.

2. Voltage Reference

The differential Voltage between VREF and VSS pins set the analog output range. VCOM is a signal ground of this chip. An electrolytic capacitor 10μF parallel with a 0.1μF ceramic capacitor attached to VREF and VCOM pins eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from VREF and VCOM pins in order to avoid unwanted coupling into the AK4380.

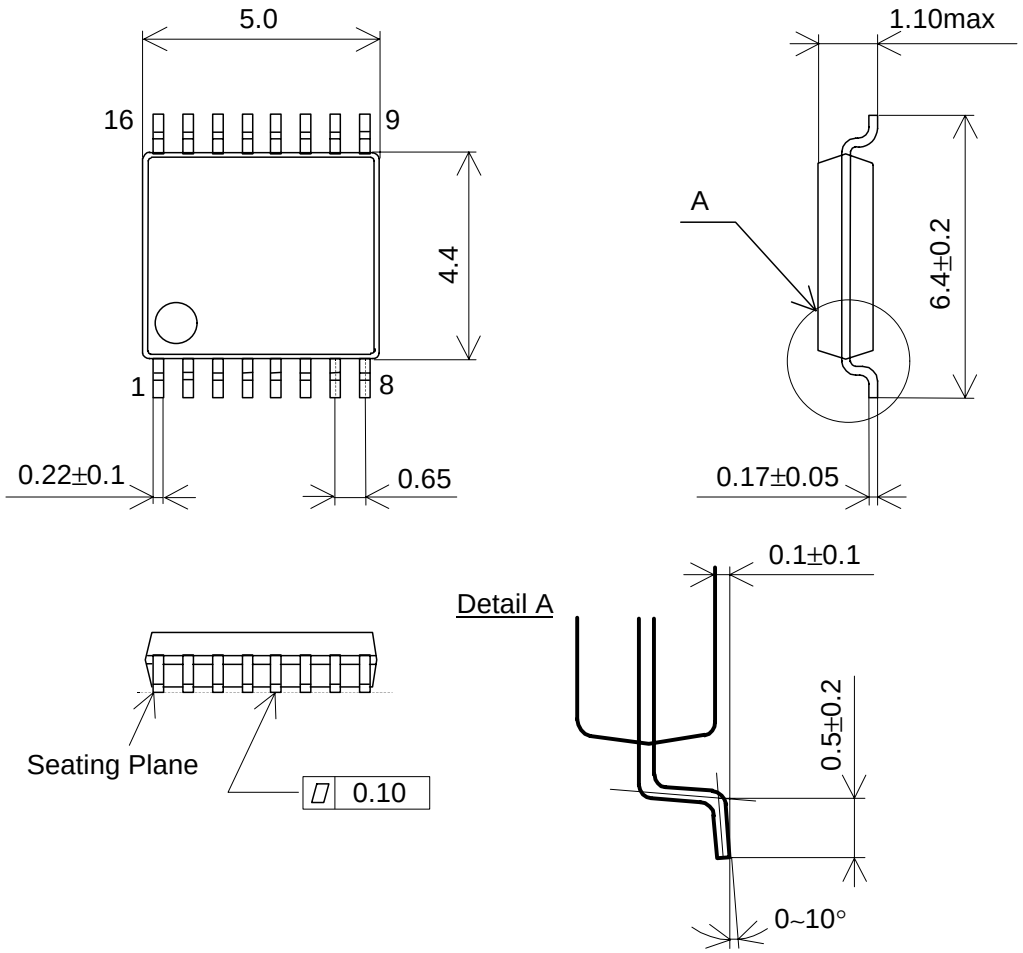
3. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 3.40Vpp (typ@VREF=5V). The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Therefore, any external filters are not required for typical application. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage for 000000H (@24bit).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of VCOM + a few mV.

PACKAGE

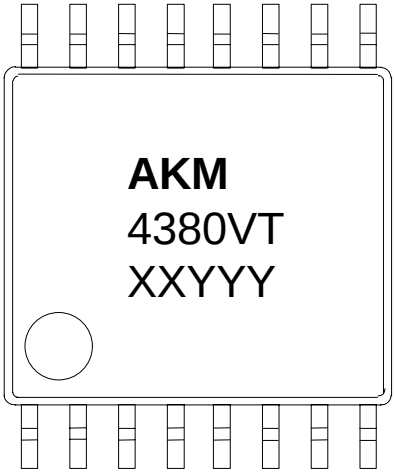
16pin TSSOP (Unit: mm)



■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: lot#
   YYY: Date Code
3) Marketing Code : 4380VT
4) Asahi Kasei Logo