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BOOTSTRAP SUPPLY CIRCUIT AND GUIDELINES

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INTRODUCTION

This application note describes the operation of the bootstrap circuit and guidelines in selecting a bootstrap capacitance value to ensure normal operation of the gate drives. Some common circuit issues are highlighted, and methods of mitigation are presented. The Allegro products related to this application note include the A491x family, the AMT491xx family, the AMT49502, and the A89503.

PRINCIPLE OF OPERATION

The bootstrap circuit is designed to provide a positive voltage bias for the high-side gate driver. When the high-side drivers are active, the reference voltage for the driver will rise close to the bridge supply voltage, V_{BRG}. The supply to the driver then must exceed the bridge supply voltage to ensure that the driver remains active. This temporary high-side supply is provided by a bootstrap capacitor connected between the bootstrap supply terminal, C, and the high-side reference terminal, S. The circuit diagram in Figure 1 describes the bootstrap operation.

When the low-side bridge MOSFET is turned on, the associated reference S terminal is close to ground, allowing the bootstrap capacitor to be independently charged to approximately V_{REG}.

When the low-side bridge MOSFET is turned off and the high-side bridge MOSFET is turned on, the voltage at the S terminal goes close to V_{BRG}. The voltage on the bootstrap supply terminal rises with the S terminal to provide the boosted gate voltage needed for the high-side N-channel bridge MOSFET. A bootstrap diode is placed in the device to provide junction isolation to permit the C node to rise above V_{REG} (Figure 1B).

BOOTSTRAP CAPACITOR SELECTION

Assume a device requires a bootstrap capacitor C, where C_{BOOT}, Q_{BOOT}, and V_{BOOT} refer to the bootstrap capacitor and Q_{GATE} refers to the high-side MOSFET. C_{BOOT} must be correctly selected to ensure proper operation of the device. Too small and there can be a large voltage drop at the time the charge is transferred from C_{BOOT} to the MOSFET gate.

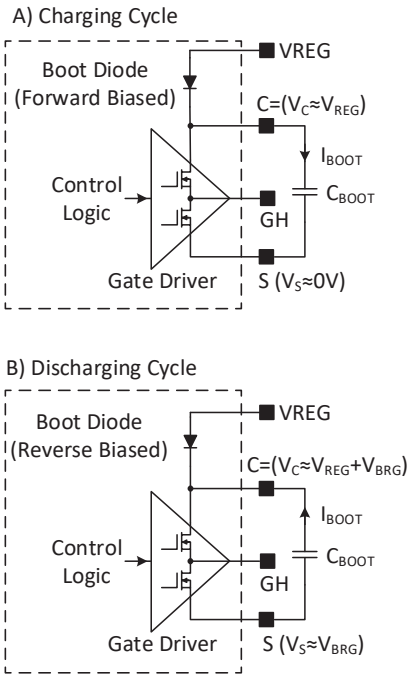

Figure 1: Diagram showing Charging Cycle (A) and Discharging Cycle (B) of bootstrap capacitor

To keep the voltage drop due to charge sharing small, the charge in the bootstrap capacitor, Q_{BOOT}, should be much larger than Q_{GATE}, the charge required by the gate:

$$Q_{BOOT} \gg Q_{GATE}$$

A factor of 20 is a reasonable value because it allows satisfactory discharge of the bootstrap capacitor during each switching cycle as demonstrated by the equations below.

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

$$C_{BOOT} = \frac{Q_{GATE} \times 20}{V_{BOOT}}$$

where V_{BOOT} is the voltage across the bootstrap capacitor,

Q_{BOOT} is the charge on the bootstrap capacitor, and Q_{GATE} is the total gate charge of the MOSFET (often labelled $Q_{G(TOT)}$).

The voltage drop, ΔV, across the bootstrap capacitor as the MOSFET is being turned on can be approximated by:

$$\Delta V = \frac{Q_{GATE}}{C_{BOOT}}$$

So, for a factor of 20, ΔV will be 5% of V_{BOOT}. The factor selected is dependent on what is the acceptable voltage drop for a specific system.

The maximum voltage across the bootstrap capacitor under normal operating conditions is V_{REG} max. However, in some circumstances, the voltage may transiently reach a maximum of 18 V, which is the clamp voltage of the Zener diode between the C terminal and the S terminal. In most applications, with a good ceramic capacitor, the working voltage can be limited to 16 V.

BOOTSTRAP CHARGING

It is necessary to ensure the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested. The time required to charge the capacitor, t_{CHARGE}, in µs, is approximated by:

$$t_{CHARGE} = \frac{C_{BOOT} \times \Delta V}{100}$$

where C_{BOOT} is the value of the bootstrap capacitor in nF and ΔV is the required voltage of the bootstrap capacitor. For further product-specific information, refer to the relevant product datasheet. At power-up and when the drivers have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case, ΔV can be considered to be the full high-side drive voltage. Otherwise, ΔV is the amount of voltage dropped during the charge transfer. The capacitor is charged whenever the S terminal is pulled low and current flows from the capacitor connected to the V_{REG} terminal through the internal bootstrap diode circuit to C_{BOOT}.

OPERATION AT 100% DUTY (TOCP)

When the high-side gate is set to operate at 100% duty cycle, the bootstrap capacitor will be unable to maintain the gate source voltage as it discharges. Bootstrap capacitor discharge occurs as a result of bias current drawn by the high-side gate driver plus any current drawn by gate-source resistors connected across the bridge MOSFET. This problem is solved by the inclusion of a top-off charge pump (TOCP) found internal to the device as seen in Figure 2. The TOCP continuously recharges the bootstrap capacitor to ensure that the voltage does not drop to an undervoltage threshold.

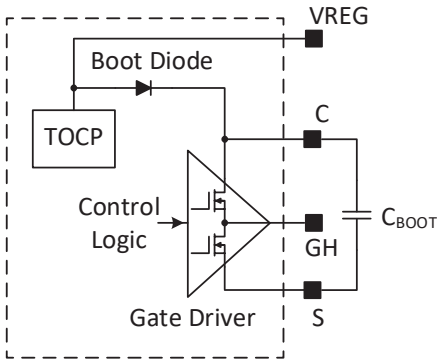

Figure 2: Diagram showing bootstrap circuit with addition of TOCP.

OPERATION AT HIGH DUTY CYCLE

If operation is such that the low-side bridge MOSFET on-time is small (typically less than one or two microseconds), it is possible that the charge required to turn on the high-side bridge MOSFET is not fully replenished on the bootstrap capacitor during each low-side bridge MOSFET on-time. Consequently, switching under these conditions cannot be sustained for many cycles because the boot capacitor charge state quickly drops to too low a level. One example of such a situation is in sinusoidal drive systems when a phase passes through periods of high duty operation (i.e. high-side bridge MOSFET on for most of the switching cycle) to drive current into the load.

It is possible to mitigate this issue to a limited extent by oversizing the bootstrap capacitor. A larger capacitor will take a longer time to discharge as it stores a larger amount of charge, allowing it to ride through the high duty cycle for a longer period of time. The following simplified justification illustrates the effect of bootstrap capacitor size.

Assuming a bootstrap capacitance (C_b) of 220 nF and MOSFET gate charge (Q_g) of 150 µC, the charge required for high-side bridge MOSFET turn-on during every PWM cycle can be represented by the following equation:

$$Q_g = C_b \, \Delta v$$

where Δ_v is the change in bootstrap capacitor voltage during each PWM cycle.

After a certain number of PWM cycles, n, the capacitor voltage will drop to the bootstrap undervoltage threshold limit (V_{BCUV}). The change in bootstrap capacitor voltage from its peak value, V_{bo} to V_{BCUV} can be represented by the following equation:

$$(V_{bo} - V_{BCUV}) = n\Delta v = \frac{nQ_g}{C_b}$$

Rearranging:

$$n = \frac{(V_{bo} - V_{BCUV})C_b}{Q_g}$$

Assuming the following illustrative datasheet values:

$$V_{BO} \approx V_{reg} \approx 10\,V \; and \; V_{BCUV} = 0.71\,V_{reg}$$

$$n = \frac{(10\,V - 0.71 \times 10\,V)220\,nF}{150\,nC} = 4$$

To increase n to 10 for example, the capacitance C_b can be recalculated as follows:

$$C_b = \frac{nQ_g}{V_{bo} - V_{BCUV}} = \frac{10 \times 150\,nC}{10\,V - 0.71 \times 10\,V} \approx 500\,nF$$

The above method assumes that the high PWM cycle will only be run for a limited period of time; hence, it provides a solution to extend the time before a bootstrap undervoltage fault occurs.

LONGTERM OPERATION AT HIGH DUTY CYCLE

Allegro offers a number of products that can operate without duty cycle restriction. These include the AMT49100, AMT49106, and AMT49107. In these products, there is a second charge pump (VCP charge pump) that generates a positive voltage, V_{CP}, with respect to V_{BB}. Under most conditions, most of the bootstrap capacitor charge is delivered directly from VREG as in a conventional bootstrap arrangement. If operating at high duty, the bootstrap capacitor charge is partly replenished from VREG on each switching cycle in the conventional way, with any shortfall being made up from VCP during periods when Sx is at supply.

During periods when the Sx node remains permanently high (100% duty), the bootstrap capacitor charge is maintained from the VCP supply. In this case, the VCP supply operates like a high power TOCP with 10 to 100 times the current capability. It provides an average current during the high-side on-time to replenish the charge before the next turn off-on event occurs. This arrangement provides the most efficient gate drive system capable of operating from 0% to 100% duty without restriction. The diagram below depicts the operation of the bootstrap circuit.

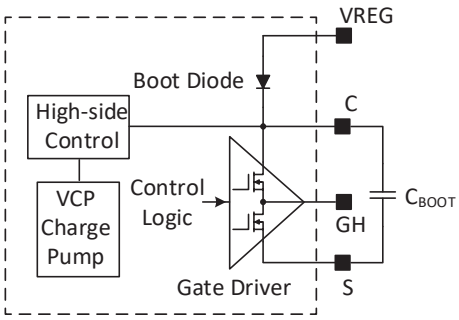

Figure 3: Diagram showing bootstrap circuit with additional VCP charge pump.

Revision History

Number	Date	Description	Responsibility
–	January 25, 2021	Initial release	I. Baptiste, A. Wood

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