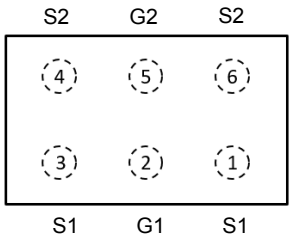
GOOD-ARK SEMICONDUCTOR

GSFCP0212

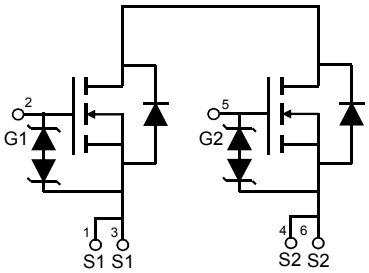
20V Dual N-Channel MOSFET

Main Product Characteristics

V_{SSS}	20V
$R_{SS(ON)}$ TYP	4.9mΩ @4.5V
	5.1mΩ @4.0V
	5.2mΩ @3.8V
	5.7mΩ @3.1V
	6.6mΩ @2.5V
I_S	12A



CSP



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Ideal for high efficiency switched mode power supplies
- Low on-resistance with low gate charge
- Fast switching and reverse body recovery

Description

The GSFCP0212 utilizes the latest techniques to achieve high cell density, low on-resistance and low gate charge. Embedded with ESD diodes, this device is extremely efficient and reliable for use as a load switch and battery protection application.

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Max.	Unit
Source-Source Voltage	V_{SSS}	20	V
Gate-Source Voltage	V_{GSS}	±12	V
Source Current (DC)[1]	I_S	12	A
Source Current (Pulsed)[1,2]	I_{SP}	120	A
Total Power Dissipation[1]	P_T	2.0	W
Channel Temperature Range	T_{ch}	+150	°C
Storage Temperature Range	T_{STG}	-55 To +150	°C

Electrical Characteristics (T_A=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static Parameters						
Source-Source Breakdown Voltage	BV_{SSS}	V_{GS}=0V, I_S=1mA	20	-	-	V
Zero Gate Voltage Source Current	I_{SSS}	V_{SS}=16V, V_{GS}=0V	-	-	100	nA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10V, V_{SS}=0V	-	-	±10	μA
		V_{GS}=±5V, V_{SS}=0V	-	-	±1.0	
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{SS}=V_{GS}, I_S=250μA	0.4	0.85	1.2	V
Static Source to Source On- Resistance	$R_{SS(ON)}$	V_{GS}=4.5V, I_S=3A	2.9	4.9	6.8	mΩ
		V_{GS}=4.0V, I_S=3A	3.0	5.1	7.1	
		V_{GS}=3.8V, I_S=3A	3.1	5.2	7.3	
		V_{GS}=3.1V, I_S=3A	3.4	5.7	8.0	
		V_{GS}=2.5V, I_S=3A	4.0	6.6	9.2	
Turn-On Delay Time[3]	$t_{d(on)}$	V_{DD}=10V, I_S=5A V_{GS}=4.0V	-	0.9	-	μS
Turn-On Rise Time[3]	t_r		-	2.6	-	
Turn-Off Delay Time[3]	$t_{d(off)}$		-	5.7	-	
Turn-Off Fall Time[3]	t_f		-	3.9	-	
Input Capacitance	C_{iss}	V_{SS}=10V, V_{GS}=0V f=1KHz	-	2609	-	pF
Output Capacitance	C_{oss}		-	362	-	
Reverse Transfer Capacitance	C_{rss}		-	295	-	
Total Gate Charge[3]	Q_g	V_{SS}=10V, V_{GS}=6V I_S=8A	-	34.7	-	nC
Gate 1 - Source 1 Charge[3]	Q_{g1s1}		-	5.9	-	
Gate 1 - Source 2 Charge[3]	Q_{g1s2}		-	11.8	-	
Diode Forward Voltage	$V_{F(S-S)}$	V_{GS}=0V, I_S=1A	-	-	1	V

Notes:

1. Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm) using the minimum recommended pad size (36μm Copper).
2. t=10ms, Duty Cycle ≤ 1%.
3. When FET1 is measured, G2 and S2 are short-circuited.

Typical Electrical and Thermal Characteristic Curves

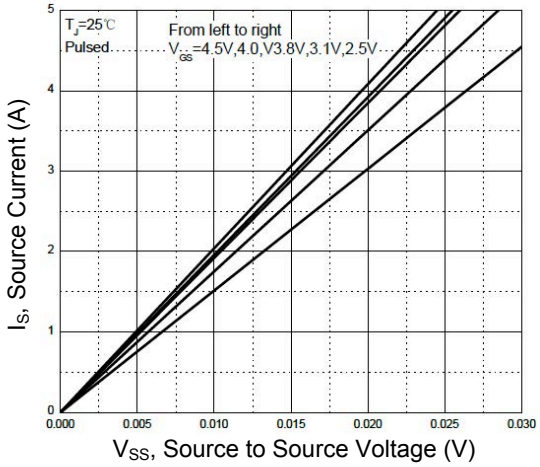


Figure 1. Output Characteristics

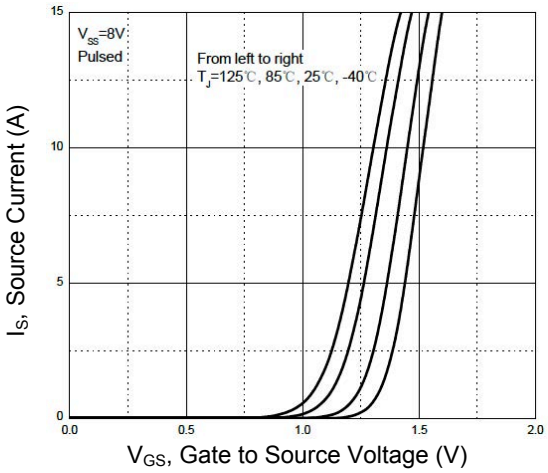


Figure 2. Transfer Characteristics

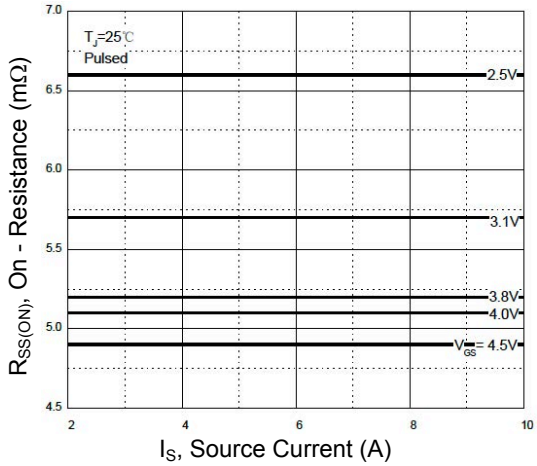


Figure 3. $R_{SS(ON)}$ - Source Current

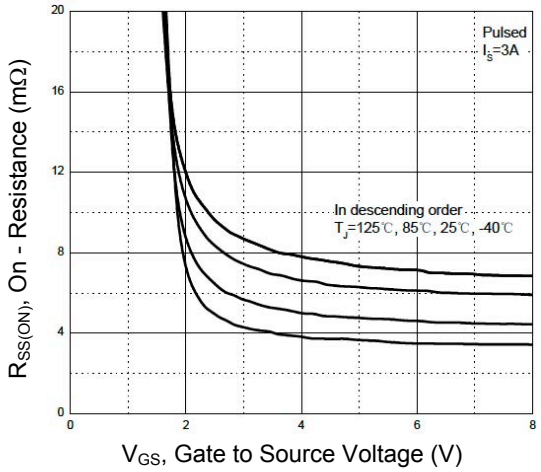


Figure 4. $R_{SS(ON)}$ - Gate to Source Voltage

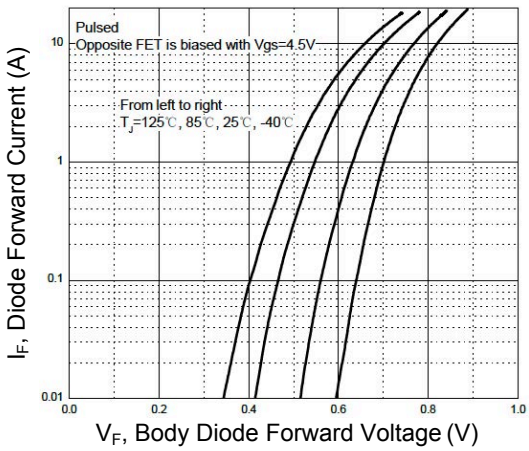


Figure 5. I_F - V_F

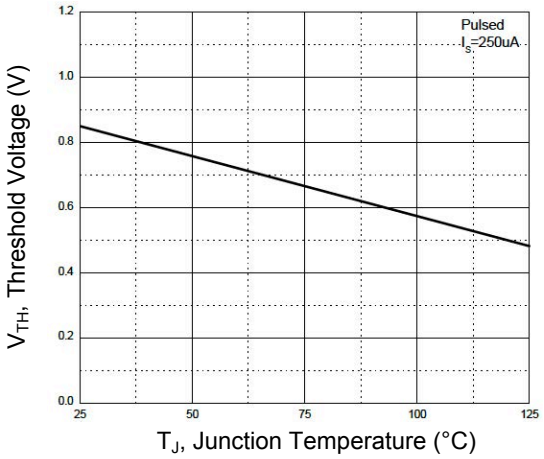


Figure 6. V_{TH} vs. T_J

Typical Electrical and Thermal Characteristic Curves

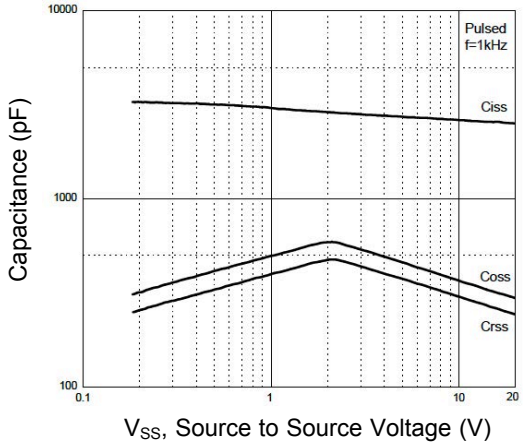


Figure 7. Capacitance Characteristics

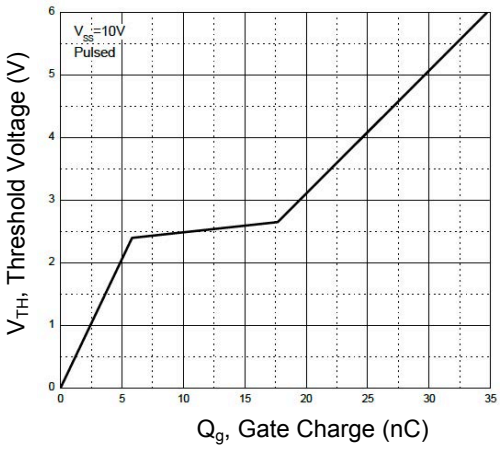


Figure 8. Gate Charge Characteristics

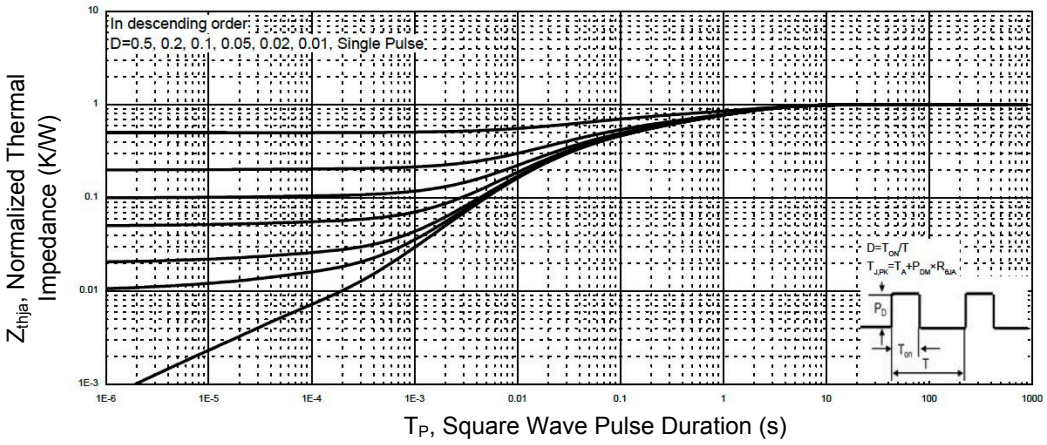


Figure 9. Normalized Maximium Transient Thermal Impedance

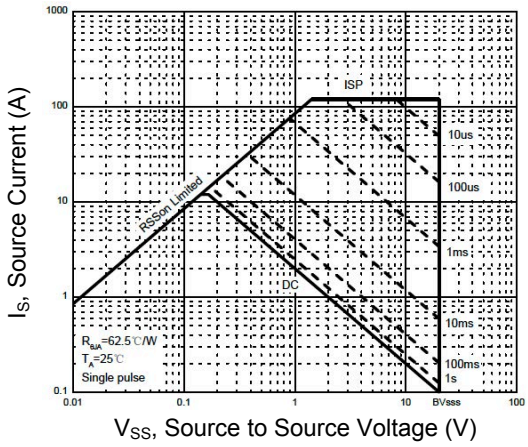
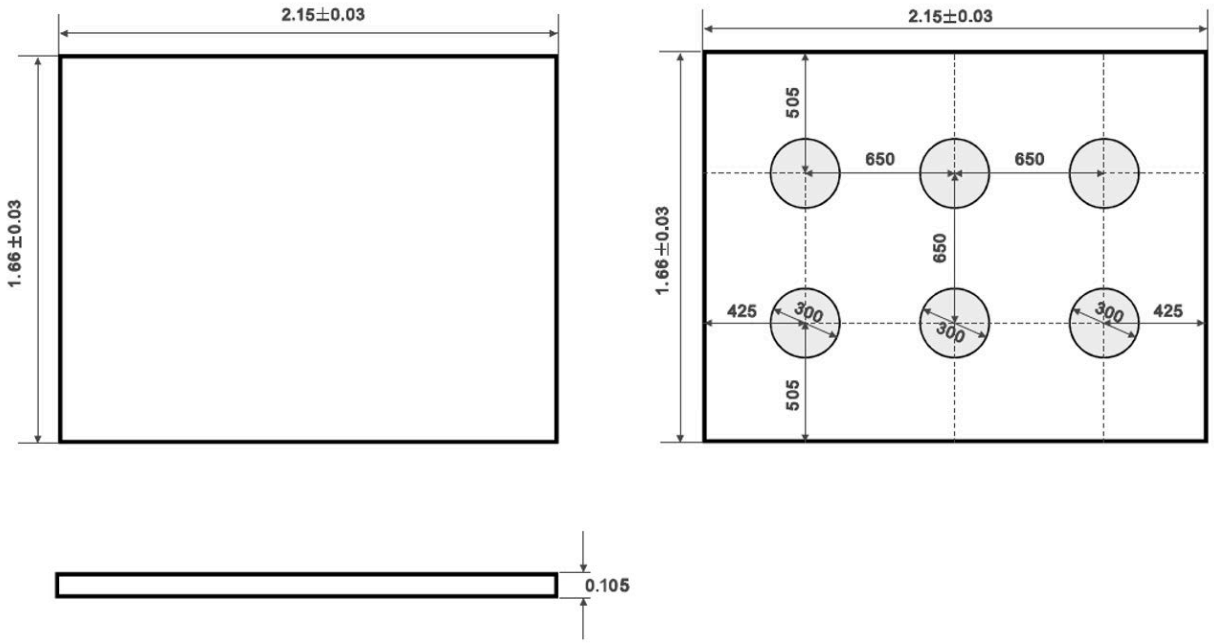


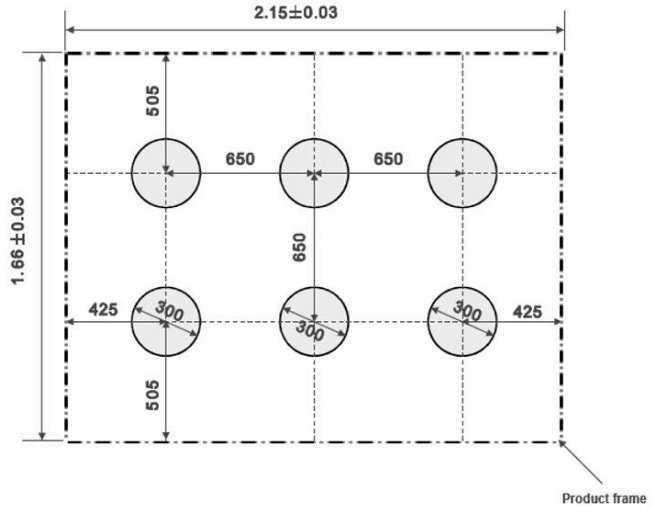
Figure 10. Maximum Forward Biased Safe Operating Area

Package Outline Dimensions (CSP)

Unit: mm



Recommended Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ±0.050mm.
3. The pad layout is for reference purposes only.