


NOTES:

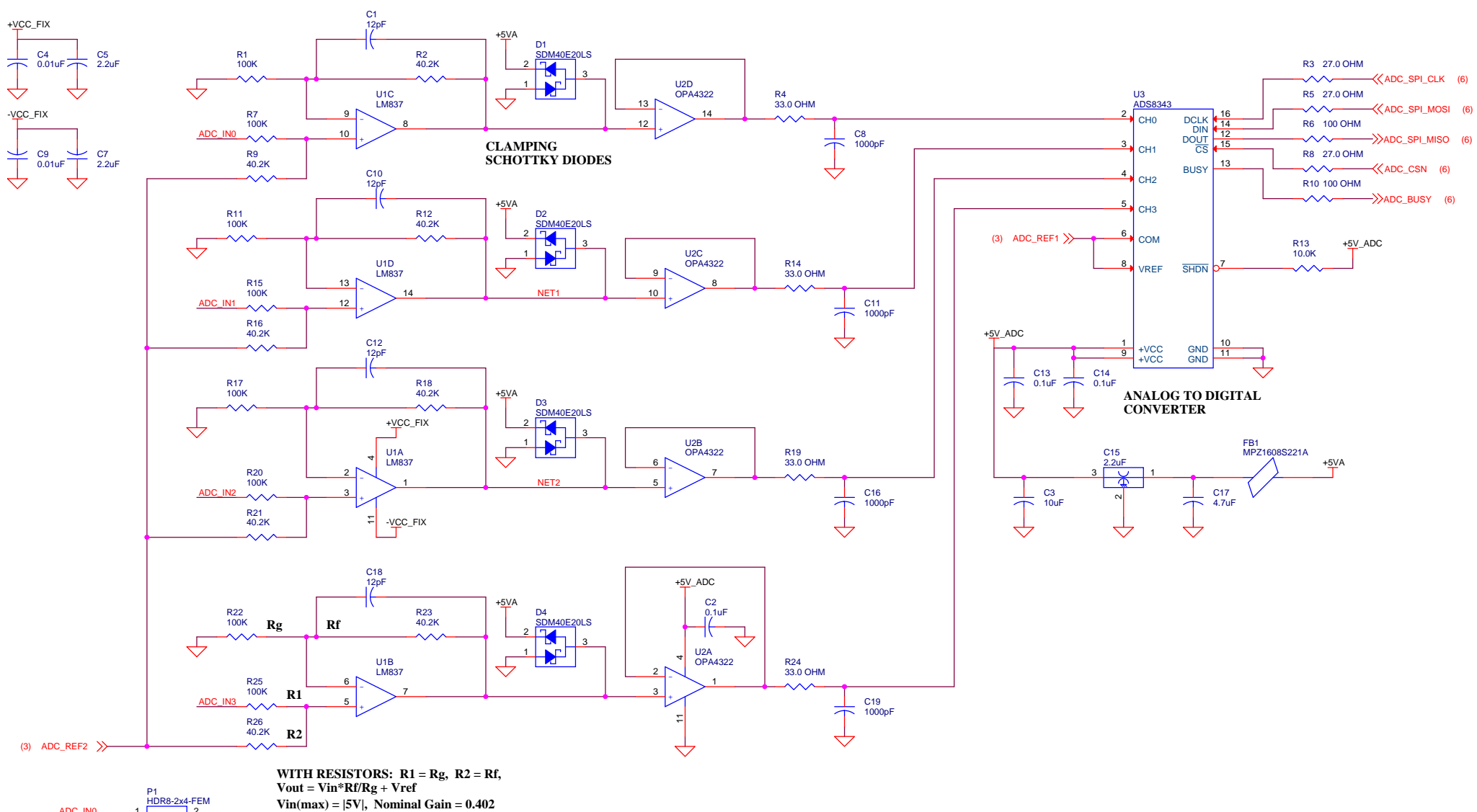
1. FULL ADC INPUT OP-AMP EQUATION

$$V_{out} = V_{in} \left[\frac{R_2}{R_1 + R_2} \right] \left[\frac{R_f + R_g}{R_g} \right] + V_{ref} \left[\frac{R_1}{R_1 + R_2} \right] \left[\frac{R_f + R_g}{R_g} \right]$$

SHEET DESCRIPTIONS:

- 01: ESD TITLE PAGE
- 02: QUAD INPUT ADC
- 03: ADC VOLTAGE REFERENCE
- 04: QUAD DAC
- 05: VOLTAGE REGULATORS
- 06: ARDUINO & EXP POWER HEADER

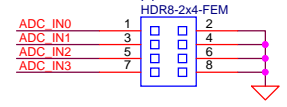
 <small>Technology by</small> TEXAS INSTRUMENTS http://www.ti.com	TEXAS INSTRUMENTS 12500 TI BOULEVARD DALLAS, TX 75243		
	IN COLLABORATION WITH STANFORD UNIVERSITY		
ELECTRONIC SCHEMATIC DIAGRAM			
ENGR D. GARCIA	Size B	CAGE Code	Rev D
RoHS COMPLIANT YES	Scale	DWG NO ANALOG SHIELD	Sheet 1 of 6
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CLAMPING SCHOTTKY DIODES

ANALOG TO DIGITAL CONVERTER

WITH RESISTORS: R1 = Rg, R2 = Rf,
 $V_{out} = V_{in} * Rf / Rg + V_{ref}$
 $V_{in(max)} = |5V|$, Nominal Gain = 0.402

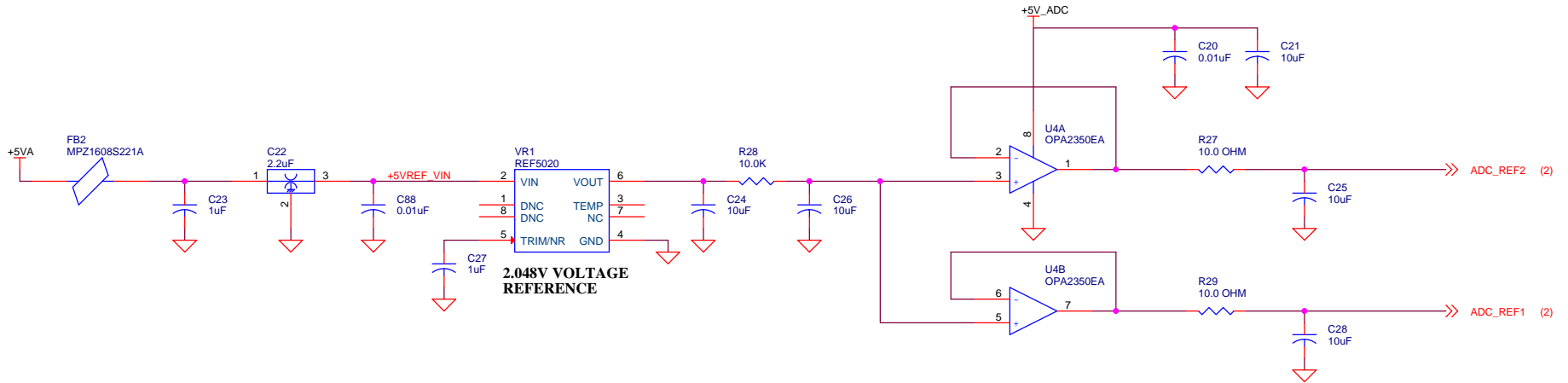



 Technology by TEXAS INSTRUMENTS http://www.ti.com		Title QUAD INPUT ADC	
		Size B	Rev D
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Scale		Friday, March 28, 2014	Sheet 2 of 6

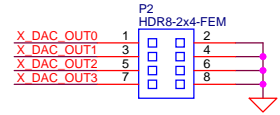
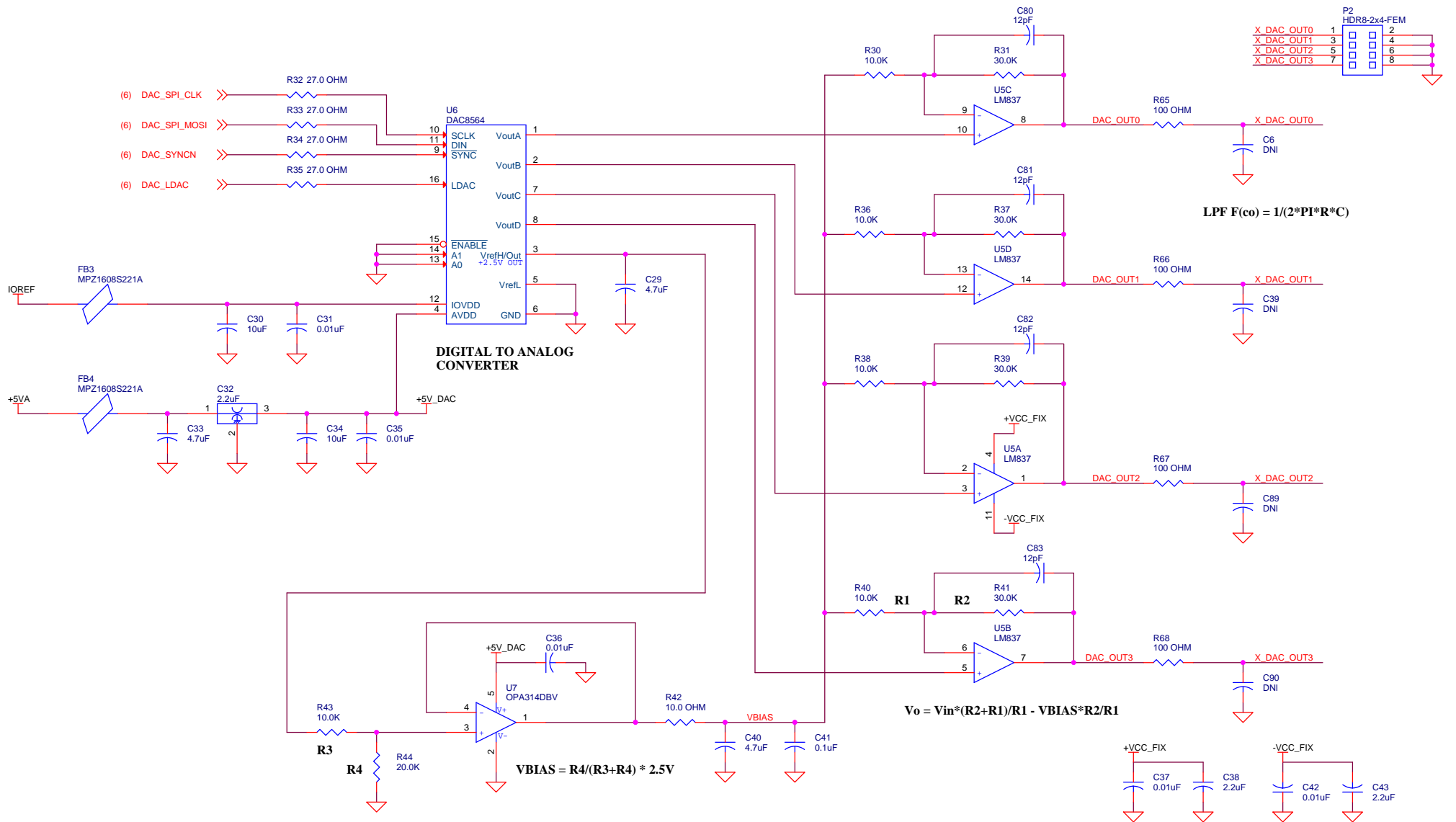
NOTE:

THIS CIRCUIT IS TAKEN FROM TI APPLICATION NOTE:
<http://www.ti.com/lit/an/slyt355/slyt355.pdf>

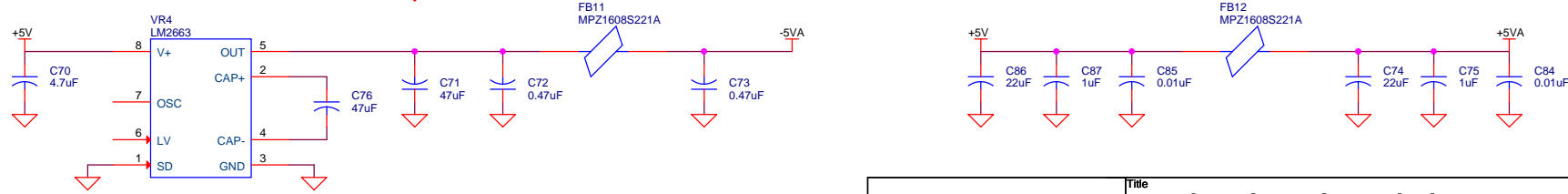
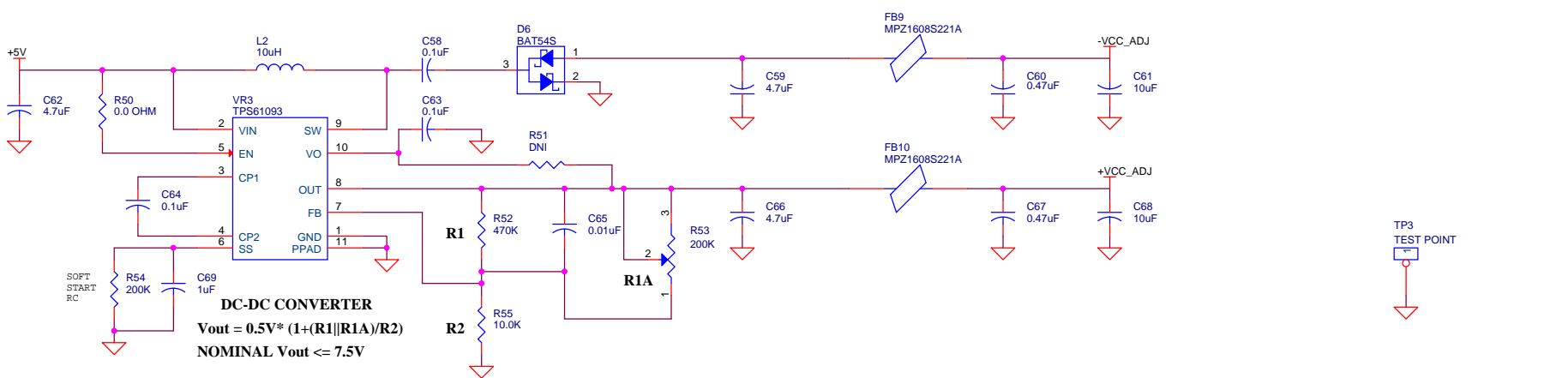
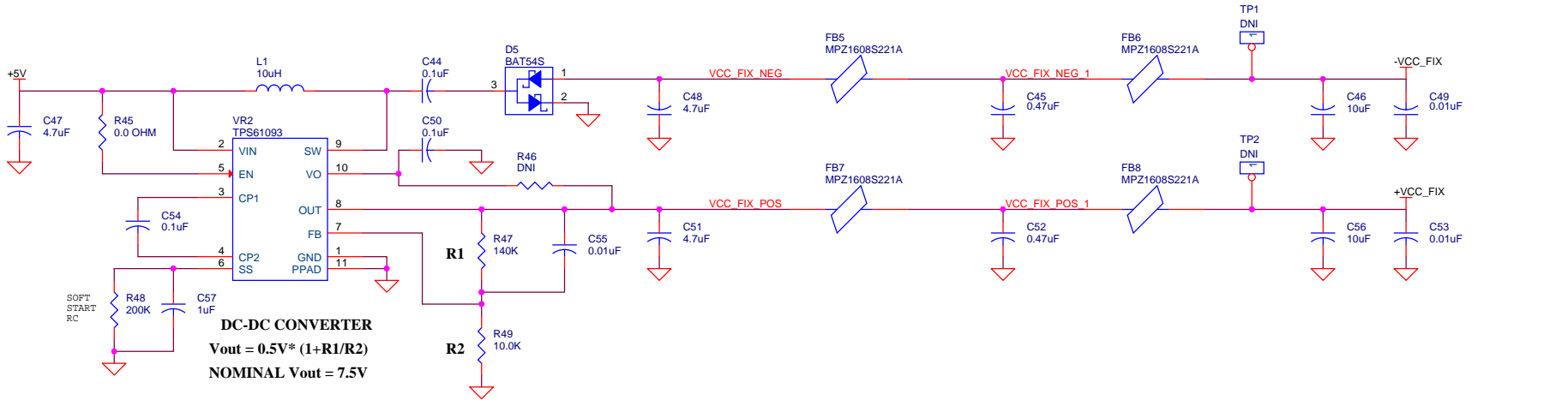
Miro Oljaca and Bonnie Baker, "How the Voltage Reference Affects ADC Performance, Part 3," Analog Applications Journal (4Q 2009)..... slyt355



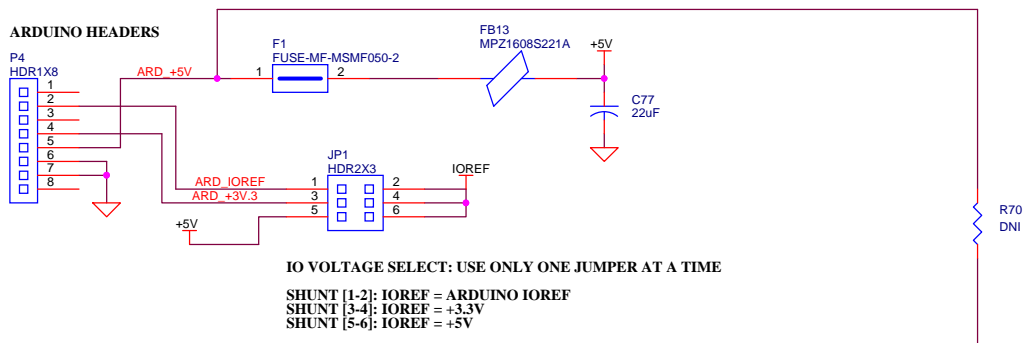
 Technology by TEXAS INSTRUMENTS http://www.ti.com	Title ADC VOLTAGE REFERENCE		
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	DWG NO ANALOG SHIELD		Sheet 3 of 6
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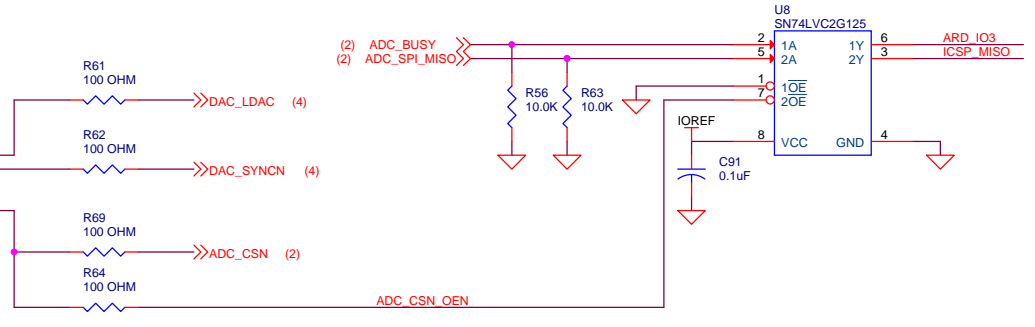
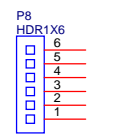
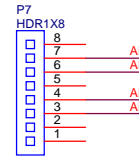
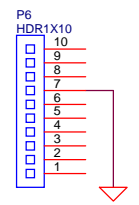
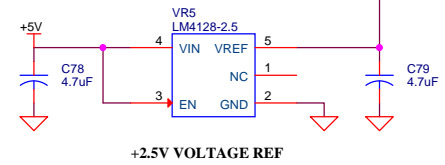
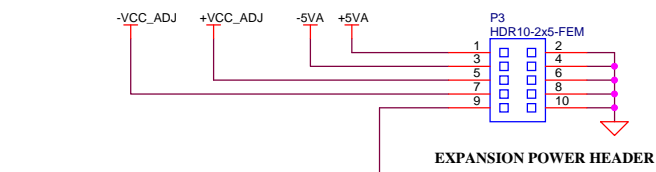
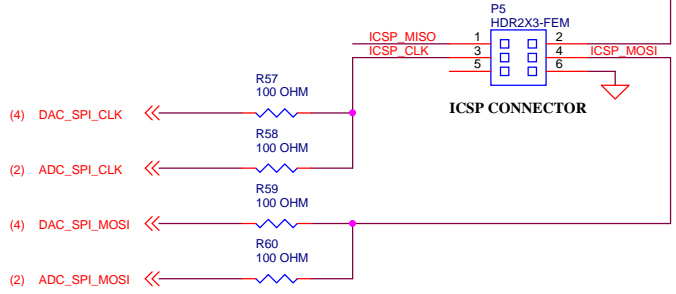
		Title		Rev
		QUAD DAC		
Size	CAGE Code	DWG NO		D
B		ANALOG SHIELD		
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IO VOLTAGE SELECT: USE ONLY ONE JUMPER AT A TIME
SHUNT [1-2]: IOREF = ARDUINO IOREF
SHUNT [3-4]: IOREF = +3.3V
SHUNT [5-6]: IOREF = +5V



		Title		
		ARDUINO & EXP POWER HEADER		
Size	CAGE Code	DWG NO	Rev	
B		ANALOG SHIELD	D	
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