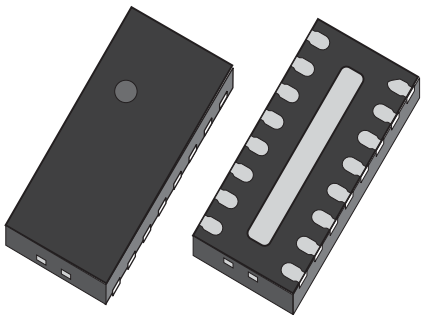
HSP061-8M16

8-line ESD protection for high speed lines

Datasheet - production data



µQFN-16L

Features

- Ultralarge bandwidth: 6.3 GHz
- Ultralow capacitance: 0.6 pF
- Low time domain reflection
- Low leakage current: 100 nA at 25 °C
- Extended operating junction temperature range: -40 °C to 150 °C
- Package size in mm: 3.3 x 1.5 x 0.55
- RoHS compliant

Benefits

- High ESD robustness of the equipment
- Suitable for high density boards

Complies with following standards

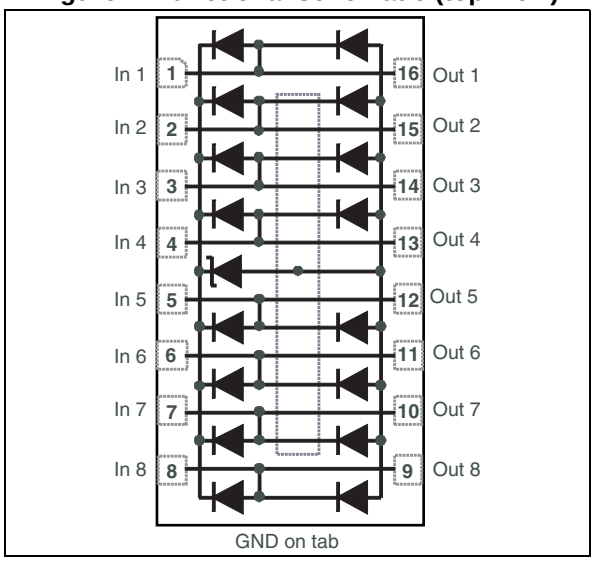
- MIL-STD 883G Method 3015-7 Class 3B:
  - 8 kV
- IEC 61000-4-2 level 4:
  - 8 kV (contact discharge)
  - 15 kV (air discharge)

Applications

The HSP061-8M16 is designed to protect against electrostatic discharge on sub micron technology circuits driving:

- HDMI 1.3 and 1.4
- Digital Video Interface
- Display Port
- Serial ATA

Figure 1. Functional schematic (top view)



Description

The HSP061-8M16 is an 8-channel ESD array with a rail to rail architecture designed specifically for the protection of high speed differential lines.

The ultra-low variation of the capacitance ensures very low influence on signal-skew. The large bandwidth and the low reflection make it compatible with 3.4 Gbps.

The device is packaged in µQFN-16L with a 400 µm pitch, which minimizes the PCB area.

1 Characteristics

Table 1. Absolute maximum ratings T_{amb} = 25 °C

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage(1)	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	8 20	kV
I_{pp}	Repetitive peak pulse current (8/20 µs)		3	A
T_j	Operating junction temperature range		-40 to +150	°C
T_{stg}	Storage temperature range		-65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

1. Measurements done on IEC 61000-4-2 test bench. For further details see Application note AN3353.

Table 2. Electrical characteristics T_{amb} = 25 °C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	Breakdown voltage	I_R = 1 mA	6			V
I_{RM}	Leakage current	V_{RM} = 3 V			100	nA
V_{CL}	Clamping voltage	IEC 61000-4-2, +8 kV contact (I_{PP} = 30 A), measured at 30 ns		14		V
$C_{I/O - GND}$	Capacitance (input/output to ground)	$V_{I/O}$ = 0 V F = 200 to 3000 MHz, V_{OSC} = 30 mV		0.6	0.8	pF
$\Delta C_{I/O - GND}$	Capacitance variation (input/output to ground)	$V_{I/O}$ = 0 V F = 200 to 3000 MHz, V_{OSC} = 30 mV		0.03	0.05	pF
f_C	Cut-off frequency	-3dB		6.3		GHz
Z_{Diff}	Differential impedance	t_r = 200 ps (10 - 90%)(1) $Z_{0\ Diff}$ = 100 Ω	90		105	Ω

1. HDMI specification conditions. This information can be provided for other applications. Please contact your local ST office.

Figure 2. Leakage current versus junction temperature (typical values)

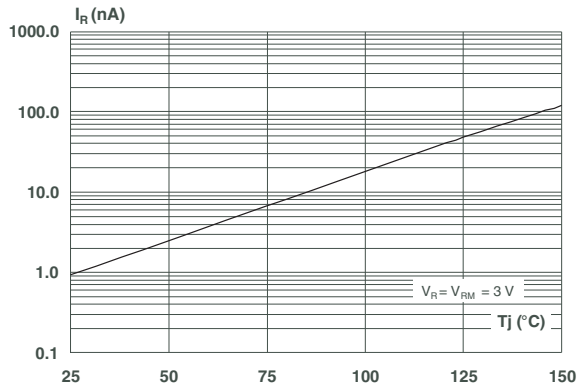


Figure 3. S21 attenuation measurement

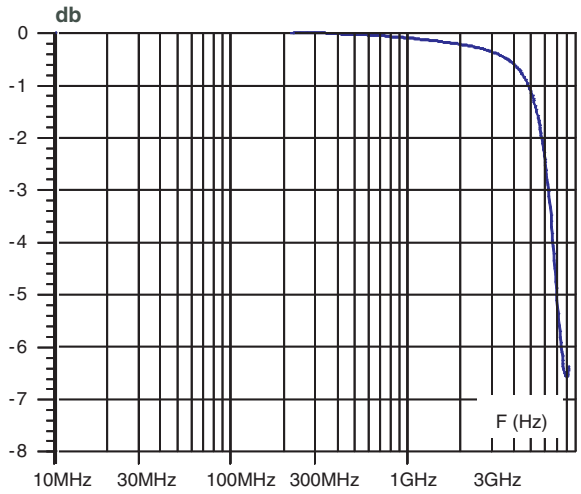


Figure 4. Differential impedance (Z_{diff})(1)

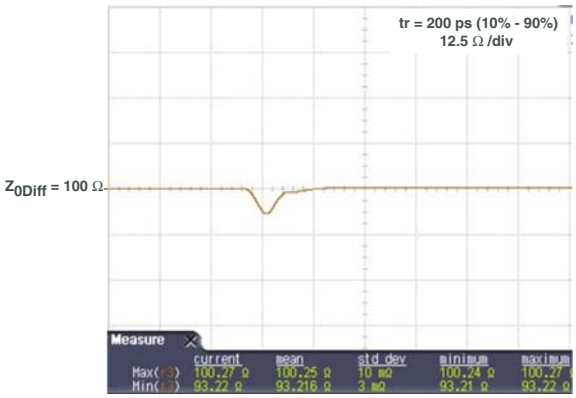
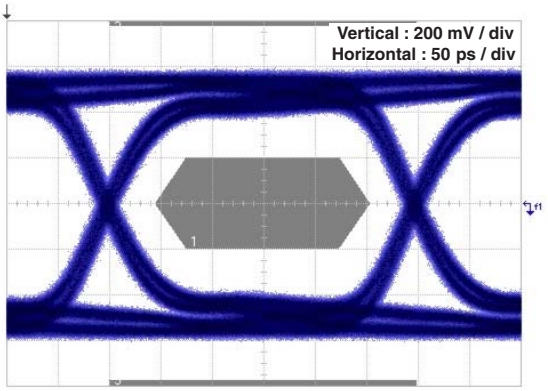


Figure 5. Eye diagram, HDMI mask, at 3.4 Gbps per channel(1)



1. HDMI specification conditions. This information can be provided for other applications. Please contact your local ST office.

Figure 6. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

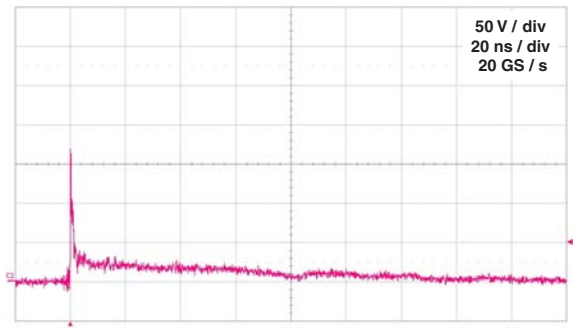
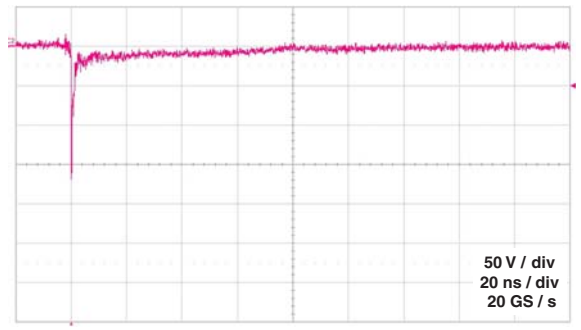


Figure 7. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

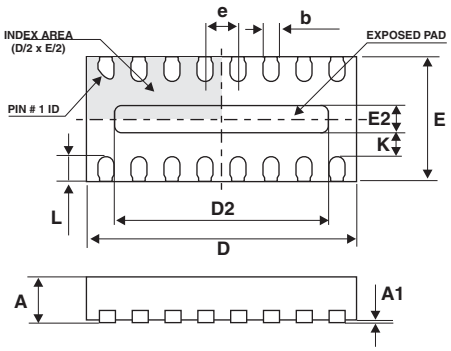


2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 8. µQFN-16L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.20	3.30	3.40	0.126	0.130	0.134
D2	2.45	2.60	2.70	0.096	0.102	0.106
E	1.40	1.50	1.60	0.055	0.059	0.063
E2	0.20	0.35	0.45	0.008	0.014	0.018
e		0.40			0.016	
K	0.20			0.008		
L	0.20	0.30	0.40	0.008	0.012	0.016

Figure 9. Footprint recommendations (dimensions in mm)

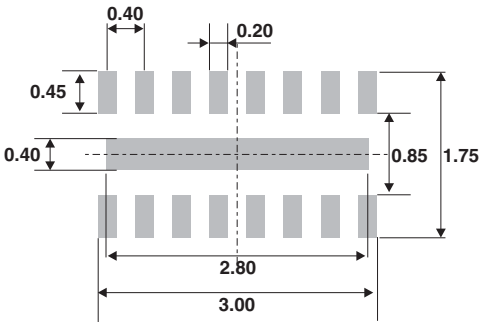
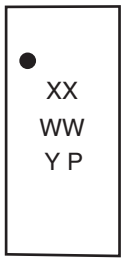
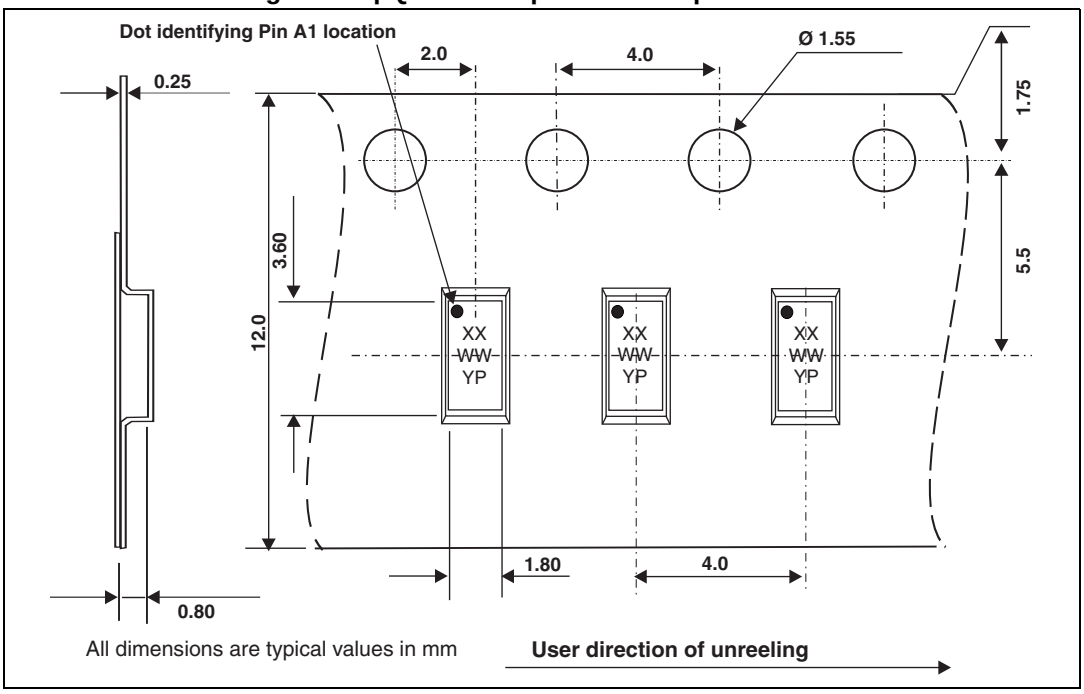


Figure 10. Marking



Dot: Pin 1
XX: Marking
WW: Assembly week
Y: Assembly year
P: Assembly plant

Figure 11. µQFN-16L tape and reel specification

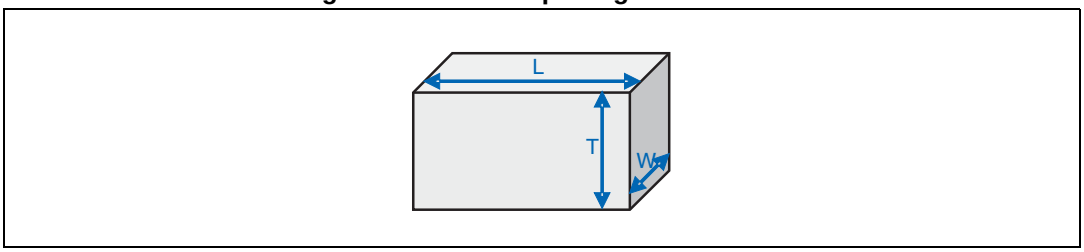


3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 12. Stencil opening dimensions



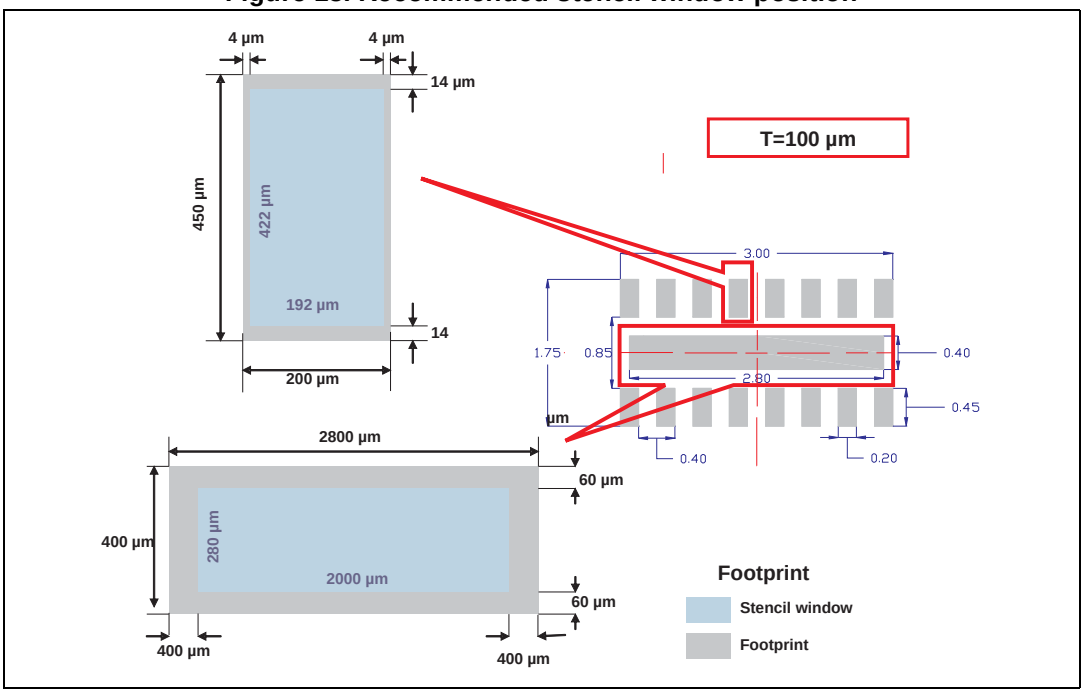
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1{,}5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0{,}66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 13. Recommended stencil window position



3.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

3.3 Placement

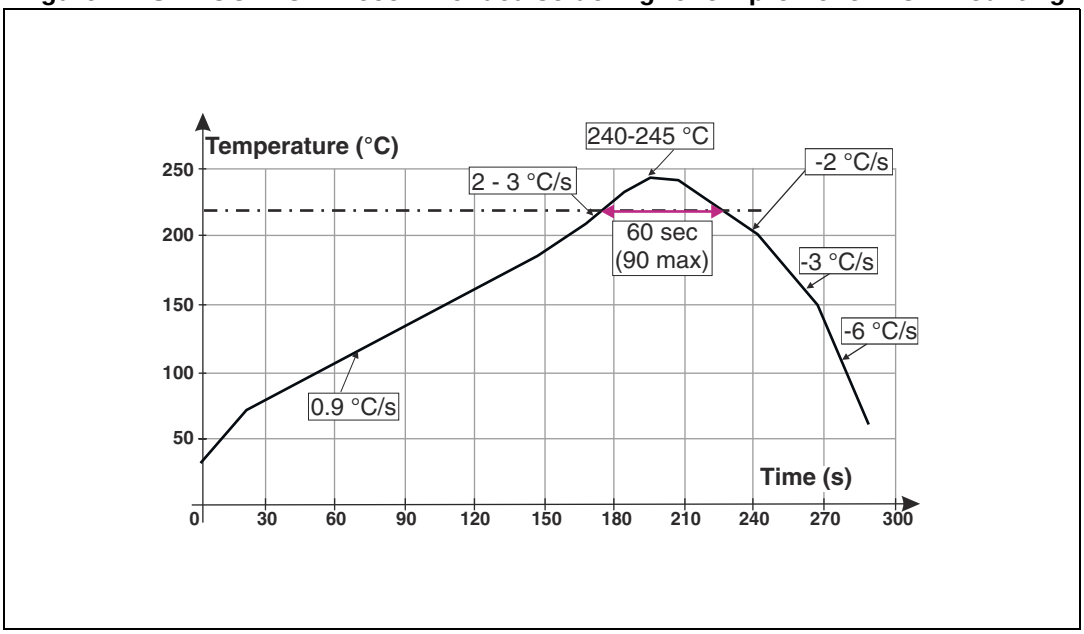
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

3.5 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Ordering information

Figure 15. Ordering information scheme

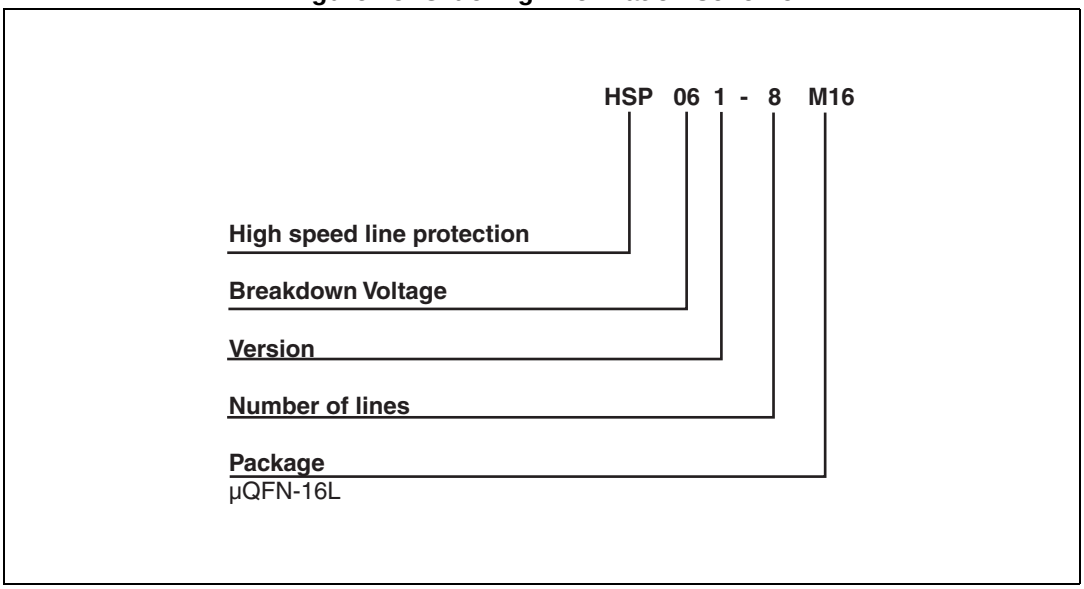


Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
HSP061-8M16	HD	µQFN-16L	12 mg	3000	Tape and reel (7”)

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
19-Nov-2010	1	Initial release.
05-May-2011	2	Updated air discharge value and added footnote in *Table 1*.
03-Apr-2014	3	Reformatted to current standard.

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