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# 1.8V, Low-Power, 12-Bit, 210MSPS ADC for Broadband Applications

MAX1214N

## General Description

The MAX1214N is a monolithic, 12-bit, 210MSPS analog-to-digital converter (ADC) optimized for outstanding dynamic performance at high-IF frequencies beyond 300MHz. The product operates with conversion rates up to 210MSPS while consuming only 799mW.

At 210MSPS and an input frequency up to 100MHz, the MAX1214N achieves an 81.3dBc spurious-free dynamic range (SFDR) with excellent 67dB signal-to-noise ratio (SNR) that remains flat (within 2dB) for input tones up to 250MHz. This makes it ideal for wideband applications such as communications receivers, cable-head end receivers, and power-amplifier predistortion in cellular base-station transceivers.

The MAX1214N operates from a single 1.8V power supply. The analog input is designed for AC-coupled differential or single-ended operation. The ADC also features a selectable on-chip divide-by-2 clock circuit that accepts clock frequencies as high as 420MHz. A low-voltage differential signal (LVDS) sampling clock is recommended for best performance. The converter provides LVDS-compatible digital outputs with data format selectable to be either two's complement or offset binary.

The MAX1214N is available in a 68-pin QFN package with exposed paddle (EP) and is specified over the industrial (-40°C to +85°C) temperature range.

See the *Pin-Compatible Versions* table for a complete selection of 8-bit, 10-bit, and 12-bit high-speed ADCs in this family.

## Applications

Base-Station Power-Amplifier Linearization  
Cable-Head End Receivers  
Wireless and Wired Broadband Communications  
Communications Test Equipment  
Radar and Satellite Subsystems

Pin Configuration appears at end of data sheet.



## Features

- ◆ 210MSPS Conversion Rate
- ◆ Excellent Low-Noise Characteristics
  - SNR = 67dB at  $f_{IN} = 100\text{MHz}$
  - SNR = 65dB at  $f_{IN} = 250\text{MHz}$
- ◆ Excellent Dynamic Range
  - SFDR = 81.3dBc at  $f_{IN} = 100\text{MHz}$
  - SFDR = 84.9dBc at  $f_{IN} = 250\text{MHz}$
- ◆ Single 1.8V Supply
- ◆ 799mW Power Dissipation at  $f_{SAMPLE} = 210\text{MSPS}$  and  $f_{IN} = 100\text{MHz}$
- ◆ On-Chip Track-and-Hold Amplifier
- ◆ Internal 1.24V-Bandgap Reference
- ◆ On-Chip Selectable Divide-by-2 Clock Input
- ◆ LVDS Digital Outputs with Data Clock Output
- ◆ MAX1214NEVKIT Available

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX1214NEGK-D	-40°C to +85°C	68 QFN-EP*	G6800-4
MAX1214NEGK+D	-40°C to +85°C	68 QFN-EP*	G6800-4

\*EP = Exposed paddle.

+Denotes lead-free package.

D = Dry pack.

## Pin-Compatible Versions

PART	RESOLUTION (BITS)	SPEED GRADE (MSPS)	ON-CHIP BUFFER
MAX1121	8	250	Yes
MAX1122	10	170	Yes
MAX1123	10	210	Yes
MAX1124	10	250	Yes
MAX1213	12	170	Yes
MAX1214	12	210	Yes
MAX1215	12	250	Yes
MAX1213N	12	170	No
MAX1214N	12	210	No
MAX1215N	12	250	No

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## ABSOLUTE MAXIMUM RATINGS

AV <sub>CC</sub> to AGND	-0.3V to +2.1V
OV <sub>CC</sub> to OGND	-0.3V to +2.1V
AV <sub>CC</sub> to OV <sub>CC</sub>	-0.3V to +2.1V
AGND to OGND	-0.3V to +0.3V
INP, INN to AGND	-0.3V to (AV <sub>CC</sub> + 0.3V)
All Digital Inputs to AGND	-0.3V to (AV <sub>CC</sub> + 0.3V)
REFIO, REFADJ to AGND	-0.3V to (AV <sub>CC</sub> + 0.3V)
All Digital Outputs to OGND	-0.3V to (OV <sub>CC</sub> + 0.3V)

Current into Any Pin	±50mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C, multilayer board)	
68-Pin QFN-EP (derate 41.7mW/°C above +70°C)	3333mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(AV<sub>CC</sub> = OV<sub>CC</sub> = 1.8V, AGND = OGND = 0, f<sub>SAMPLE</sub> = 210MHz, differential clock input drive, 0.1μF capacitor on REFIO, internal reference, digital output pins differential R<sub>L</sub> = 100Ω. Limits are for T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ACCURACY</b>						
Resolution			12			Bits
Integral Nonlinearity	INL	f <sub>IN</sub> = 10MHz (Note 2)	-2.1	±0.75	+2.1	LSB
Differential Nonlinearity	DNL	No missing codes (Note 2)	-1.0	±0.3	+1.3	LSB
Transfer Curve Offset	V <sub>OS</sub>	(Note 2)	-3		+3	mV
Offset Temperature Drift				±15		μV/°C
<b>ANALOG INPUTS (INP, INN)</b>						
Full-Scale Input Voltage Range	V <sub>FS</sub>		1150	1390		mV <sub>P-P</sub>
Full-Scale Range Temperature Drift				±60		ppm/°C
Common-Mode Input Voltage	V <sub>CM</sub>	Internally self-biased		0.7		V
Differential Input Capacitance	C <sub>IN</sub>			2.5		pF
Differential Input Resistance	R <sub>IN</sub>			1.8		kΩ
Full-Power Analog Bandwidth	FPBW			700		MHz
<b>REFERENCE (REFIO, REFADJ)</b>						
Reference Output Voltage	V <sub>REFIO</sub>	REFADJ = AGND	1.18	1.24	1.30	V
Reference Temperature Drift				90		ppm/°C
REFADJ Input High Voltage	V <sub>REFADJ</sub>	Used to disable the internal reference	AV <sub>CC</sub> - 0.3			V
<b>SAMPLING CHARACTERISTICS</b>						
Maximum Sampling Rate	f <sub>SAMPLE</sub>		210			MHz
Minimum Sampling Rate	f <sub>SAMPLE</sub>			20		MHz
Clock Duty Cycle		Set by clock-management circuit		40 to 60		%
Aperture Delay	t <sub>AD</sub>	Figures 5, 11		620		ps
Aperture Jitter	t <sub>AJ</sub>	Figure 11		0.15		psRMS

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## ELECTRICAL CHARACTERISTICS (continued)

(AVCC = OVCC = 1.8V, AGND = OGND = 0, fSAMPLE = 210MHz, differential clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential RL = 100Ω. Limits are for TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CLOCK INPUTS (CLKP, CLKN)</b>						
Differential Clock Input Amplitude		(Note 3)	200	500		mVp-p
Clock Input Common-Mode Voltage Range		Internally self-biased		1.15 ±0.25		V
Clock Differential Input	RCLK			11 ±25%		kΩ
Clock Differential Input Capacitance	CCLK			5		pF
<b>DYNAMIC CHARACTERISTICS (at AIN = -1dBFS)</b>						
Signal-to-Noise Ratio	SNR	fIN = 10MHz	65.5	67.3		dB
		fIN = 100MHz	65.2	67		
		fIN = 200MHz		65.3		
		fIN = 250MHz		65.0		
Signal-to-Noise and Distortion	SINAD	fIN = 10MHz	65.3	67.2		dB
		fIN = 100MHz	64.9	66.6		
		fIN = 200MHz		65.2		
		fIN = 250MHz		64.9		
Spurious-Free Dynamic Range	SFDR	fIN = 10MHz	77.0	88.5		dBc
		fIN = 100MHz	76.0	81.3		
		fIN = 200MHz		82.8		
		fIN = 250MHz		84.9		
Worst Harmonics (HD2 or HD3)		fIN = 10MHz		-88.5	-77.0	dBc
		fIN = 100MHz		-81.3	-76.0	
		fIN = 200MHz		-82.8		
		fIN = 250MHz		-84.9		
Two-Tone Intermodulation Distortion	TTIMD	fIN1 = 97MHz at -7dBFS, fIN2 = 100MHz at -7dBFS		-79		dBc
<b>LVDS DIGITAL OUTPUTS (D0P/N-D11P/N, ORP/N)</b>						
Differential Output Voltage	VOD	RL = 100Ω	280		440	mV
Output Offset Voltage	OVOS	RL = 100Ω	1.110		1.370	V

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = OV_{CC} = 1.8V$ ,  $AGND = OGND = 0$ ,  $f_{SAMPLE} = 210MHz$ , differential clock input drive,  $0.1\mu F$  capacitor on REFIO, internal reference, digital output pins differential  $R_L = 100\Omega$ . Limits are for  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LVCMOS DIGITAL INPUTS (CLKDIV, <math>\bar{T}/B</math>)</b>						
Digital Input-Voltage Low	$V_{IL}$			$0.2 \times AV_{CC}$		V
Digital Input-Voltage High	$V_{IH}$		$0.8 \times AV_{CC}$			V
<b>TIMING CHARACTERISTICS</b>						
CLK-to-Data Propagation Delay	$t_{PDL}$	Figure 5		2.05		ns
CLK-to-DCLK Propagation Delay	$t_{CPDL}$	Figure 5		3.95		ns
DCLK-to-Data Propagation Delay	$t_{CPDL} - t_{PDL}$	Figure 5 (Note 3)	1.8	1.9	2.0	ns
LVDS Output Rise Time	$t_{RISE}$	20% to 80%, $C_L = 5pF$		450		ps
LVDS Output Fall Time	$t_{FALL}$	20% to 80%, $C_L = 5pF$		450		ps
Output Data Pipeline Delay	$t_{LATENCY}$	Figure 5		11		Clock cycles
<b>POWER REQUIREMENTS</b>						
Analog Supply Voltage Range	$AV_{CC}$		1.70	1.80	1.90	V
Digital Supply Voltage Range	$OV_{CC}$		1.70	1.80	1.90	V
Analog Supply Current	$I_{AVCC}$	$f_{IN} = 100MHz$		379	410	mA
Digital Supply Current	$I_{OVCC}$	$f_{IN} = 100MHz$		65	71	mA
Analog Power Dissipation	$P_{DISS}$	$f_{IN} = 100MHz$		799	866	mW
Power-Supply Rejection Ratio (Note 4)	PSRR	Offset		1.8		mV/V
		Gain		1.5		%FS/V

**Note 1:** Values at  $T_A \geq +25^\circ C$  guaranteed by production test, values at  $T_A < +25^\circ C$  guaranteed by design and characterization.

**Note 2:** Static linearity and offset parameters are computed from an end-point curve fit.

**Note 3:** Parameter guaranteed by design and characterization:  $T_A = -40^\circ C$  to  $+85^\circ C$ .

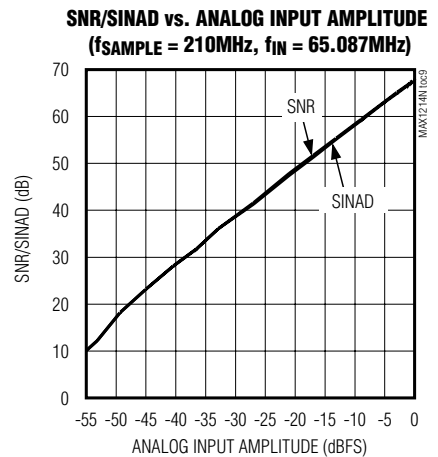
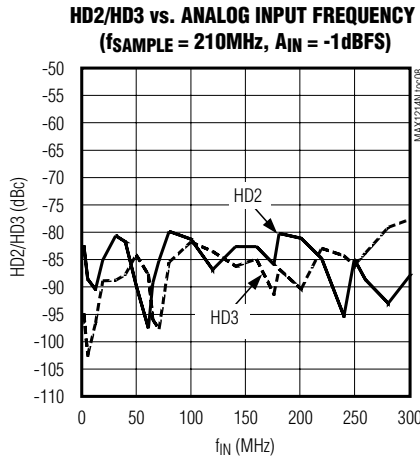
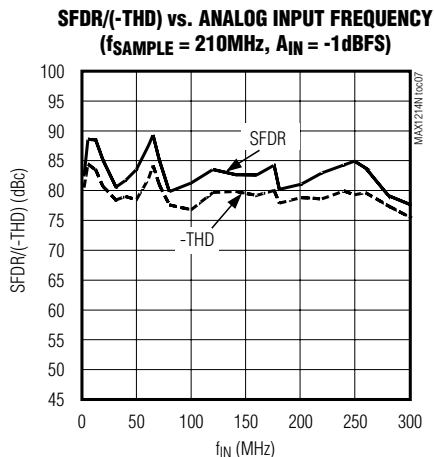
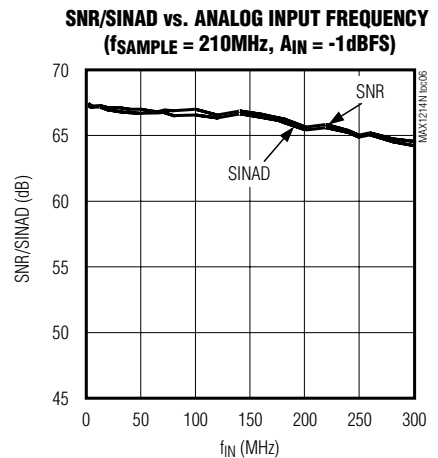
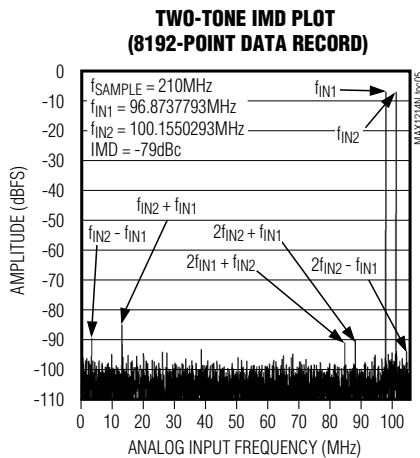
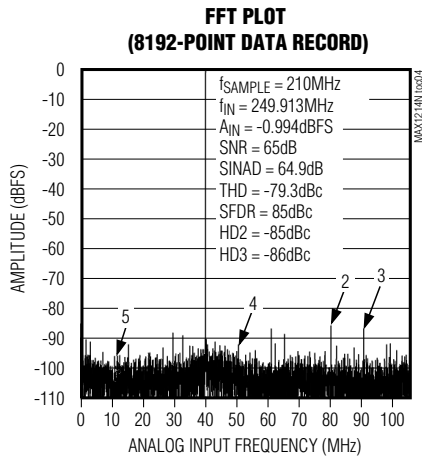
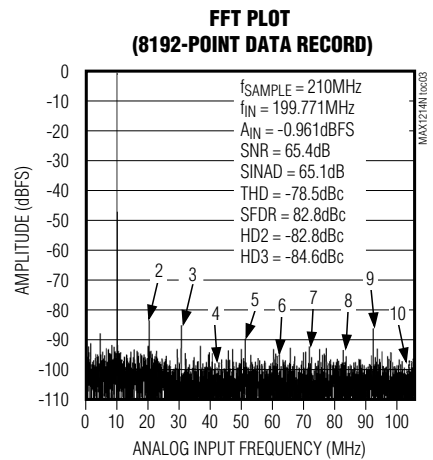
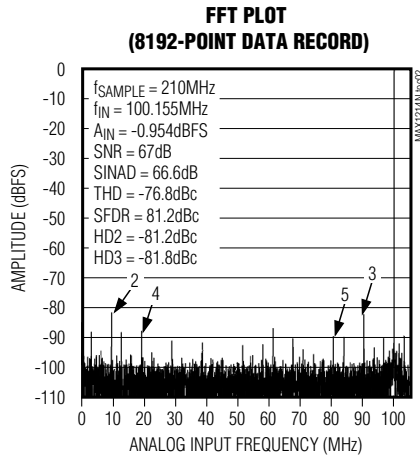
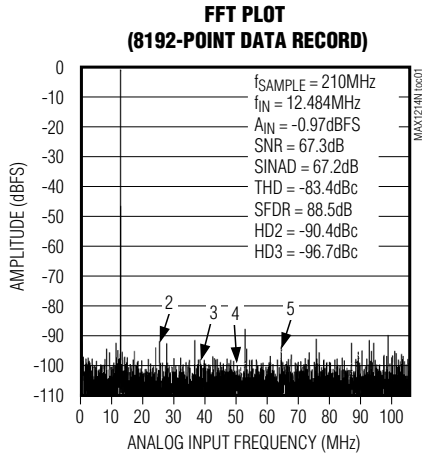
**Note 4:** PSRR is measured with both analog and digital supplies connected to the same potential.

# 1.8V, Low-Power, 12-Bit, 210Mps ADC for Broadband Applications

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## Typical Operating Characteristics

( $V_{CC} = OV_{CC} = 1.8V$ ,  $AGND = O_{GND} = 0$ ,  $f_{SAMPLE} = 210MHz$ ,  $A_{IN} = -1dBFS$ ; see each TOC for detailed information on test conditions, differential input drive, differential sine-wave clock input drive,  $0.1\mu F$  capacitor on REFIO, internal reference, digital output pins differential  $R_L = 100\Omega$ ,  $T_A = +25^\circ C$ .)

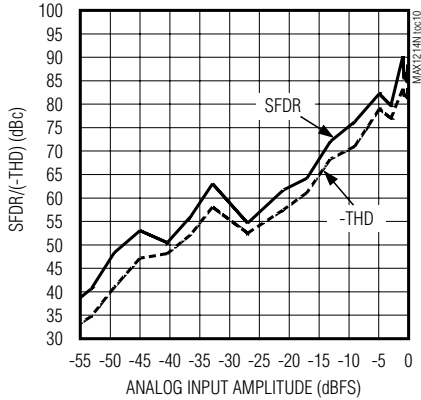


# 1.8V, Low-Power, 12-Bit, 210Mps ADC for Broadband Applications

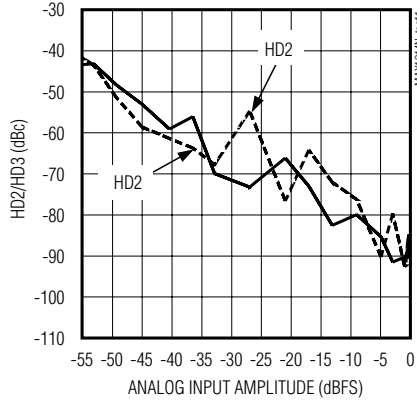
## Typical Operating Characteristics (continued)

( $V_{CC} = OV_{CC} = 1.8V$ ,  $AGND = OGND = 0$ ,  $f_{SAMPLE} = 210MHz$ ,  $A_{IN} = -1dBFS$ ; see each TOC for detailed information on test conditions, differential input drive, differential sine-wave clock input drive, 0.1 $\mu F$  capacitor on REFIO, internal reference, digital output pins differential  $R_L = 100\Omega$ ,  $T_A = +25^\circ C$ .)

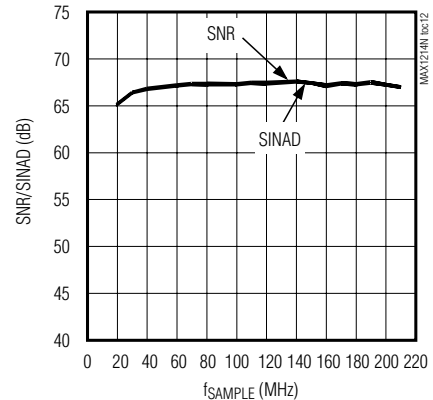
**SFDR/(-THD) vs. ANALOG INPUT AMPLITUDE**  
( $f_{SAMPLE} = 210MHz$ ,  $f_{IN} = 65.087MHz$ )



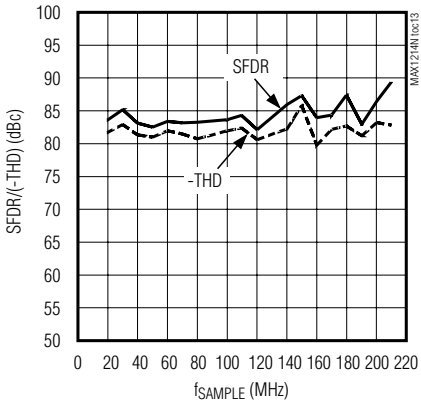
**HD2/HD3 vs. ANALOG INPUT AMPLITUDE**  
( $f_{SAMPLE} = 210MHz$ ,  $f_{IN} = 65.087MHz$ )



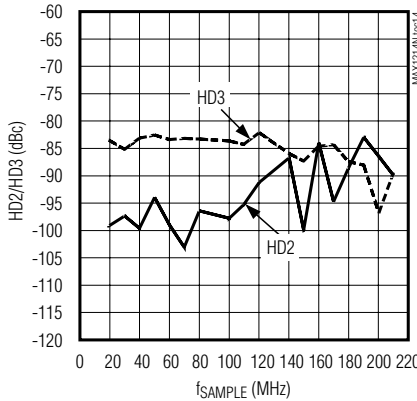
**SNR/SINAD vs. SAMPLE FREQUENCY**  
( $f_{IN} = 65.087MHz$ ,  $A_{IN} = -1dBFS$ )



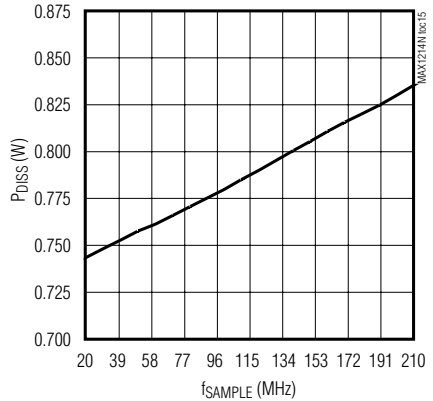
**SFDR/(-THD) vs. SAMPLE FREQUENCY**  
( $f_{IN} = 65.087MHz$ ,  $A_{IN} = -1dBFS$ )



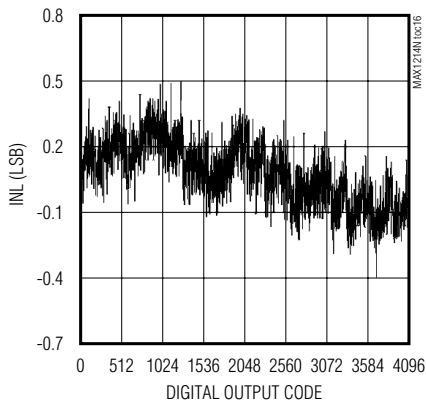
**HD2/HD3 vs. SAMPLE FREQUENCY**  
( $f_{IN} = 65.087MHz$ ,  $A_{IN} = -1dBFS$ )



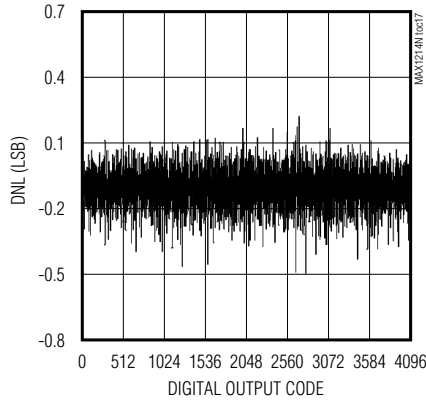
**TOTAL POWER DISSIPATION vs. SAMPLE FREQUENCY**  
( $f_{IN} = 65.087MHz$ ,  $A_{IN} = -1dBFS$ )



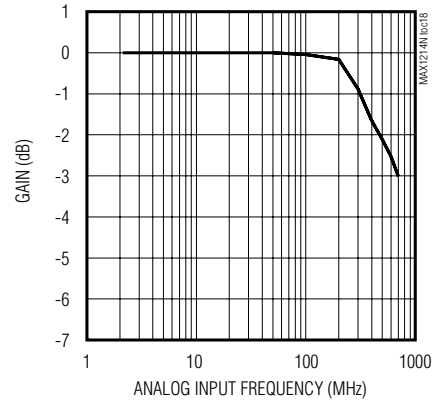
**INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE**



**DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE**



**GAIN BANDWIDTH PLOT**  
( $f_{SAMPLE} = 210MHz$ ,  $A_{IN} = -1dBFS$ )

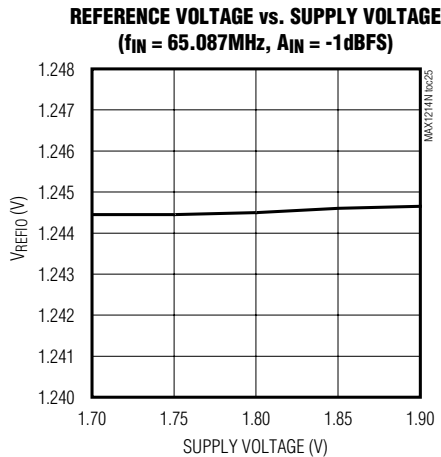
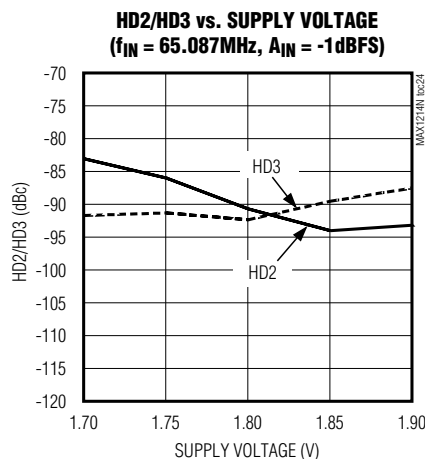
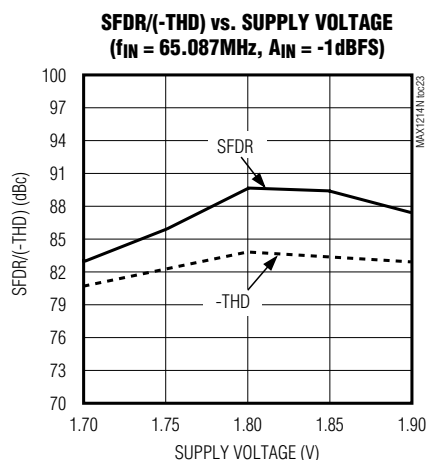
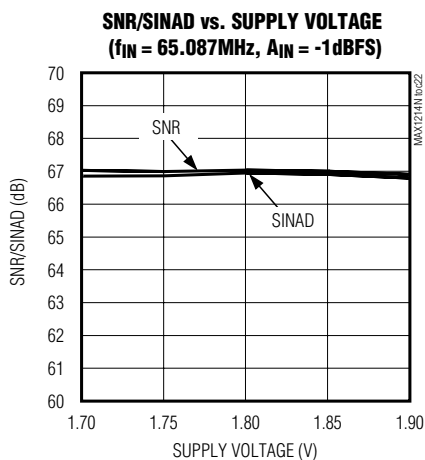
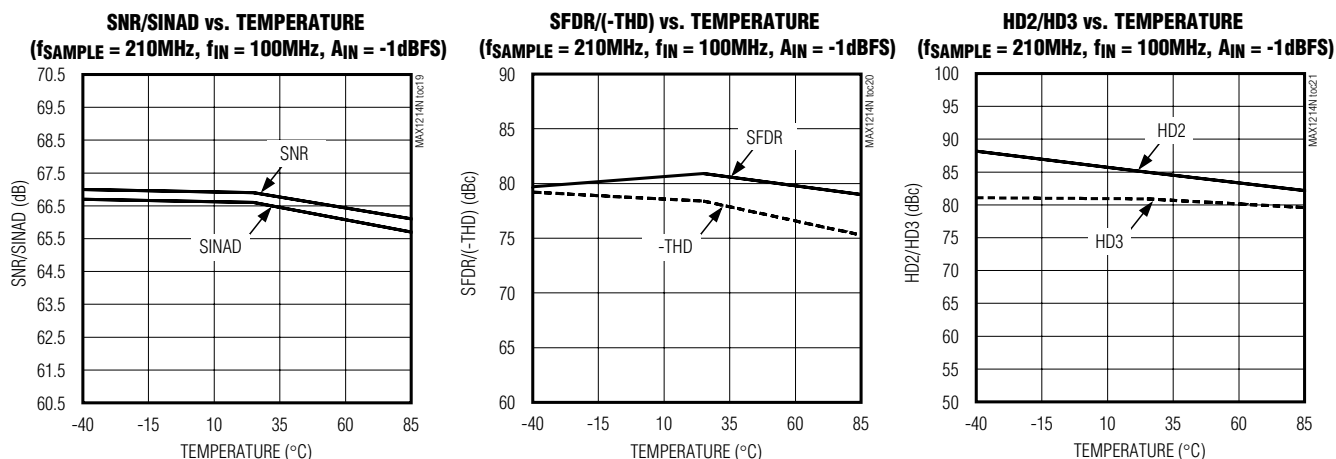


# 1.8V, Low-Power, 12-Bit, 210Mps ADC for Broadband Applications

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## Typical Operating Characteristics (continued)

( $V_{CC} = OV_{CC} = 1.8V$ ,  $AGND = OGND = 0$ ,  $f_{SAMPLE} = 210MHz$ ,  $A_{IN} = -1dBFS$ ; see each TOC for detailed information on test conditions, differential input drive, differential sine-wave clock input drive,  $0.1\mu F$  capacitor on REFIO, internal reference, digital output pins differential  $R_L = 100\Omega$ ,  $T_A = +25^\circ C$ .)



# 1.8V, Low-Power, 12-Bit, 210Mps ADC for Broadband Applications

## Pin Description

PIN	NAME	FUNCTION
1, 6, 11–14, 20, 25, 62, 63, 65	AV <sub>CC</sub>	Analog Supply Voltage. Bypass AV <sub>CC</sub> to AGND with a parallel combination of 0.1μF and 0.22μF capacitors for best decoupling results. Connect all AV <sub>CC</sub> inputs together. See the <i>Grounding, Bypassing, and Board Layout Considerations</i> section.
2, 5, 7, 10, 15, 16, 18, 19, 21, 24, 64, 66, 67	AGND	Analog Converter Ground. Connect all AGND inputs together.
3	REFIO	Reference Input/Output. Pull REFADJ high to allow REFIO to accept an external reference. Pull REFADJ low to activate the internal 1.24V-bandgap reference. Connect a 0.1μF capacitor from REFIO to AGND for both internal and external reference.
4	REFADJ	Reference Adjust Input. REFADJ allows for FSR adjustments by placing a resistor or trim potentiometer between REFADJ and AGND (decreases FSR) or REFADJ and REFIO (increases FSR). Connect REFADJ to AV <sub>CC</sub> to override the internal reference with an external source connected to REFIO. Connect REFADJ to AGND to allow the internal reference to determine the FSR of the data converter. See the <i>FSR Adjustment Using the Internal Bandgap Reference</i> section.
8	INP	Positive Analog Input Terminal. Internally self-biased to 0.7V.
9	INN	Negative Analog Input Terminal. Internally self-biased to 0.7V.
17	CLKDIV	Clock Divider Input. CLKDIV controls the sampling frequency relative to the input clock frequency. CLKDIV has an internal pulldown resistor. CLKDIV = 0: Sampling frequency is at one-half the input clock frequency. CLKDIV = 1: Sampling frequency is equal to the input clock frequency.
22	CLKP	True Clock Input. Apply an LVDS-compatible input level to CLKP. Internally self-biased to 1.15V.
23	CLKN	Complementary Clock Input. Apply an LVDS-compatible input level to CLKN. Internally self-biased to 1.15V.
26, 45, 61	OGND	Digital Converter Ground. Ground connection for digital circuitry and output drivers. Connect all OGND inputs together.
27, 28, 41, 44, 60	OV <sub>CC</sub>	Digital Supply Voltage. Bypass OV <sub>CC</sub> with a 0.1μF capacitor to OGND. Connect all OV <sub>CC</sub> inputs together. See the <i>Grounding, Bypassing, and Board Layout Considerations</i> section.
29	D0N	Complementary Output Bit 0 (LSB)
30	D0P	True Output Bit 0 (LSB)
31	D1N	Complementary Output Bit 1
32	D1P	True Output Bit 1
33	D2N	Complementary Output Bit 2
34	D2P	True Output Bit 2
35	D3N	Complementary Output Bit 3
36	D3P	True Output Bit 3



# 1.8V, Low-Power, 12-Bit, 210MSPS ADC for Broadband Applications

## Pin Description (continued)

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PIN	NAME	FUNCTION
37	D4N	Complementary Output Bit 4
38	D4P	True Output Bit 4
39	D5N	Complementary Output Bit 5
40	D5P	True Output Bit 5
42	DCLKN	Complementary Clock Output. This output provides an LVDS-compatible output level and can be used to synchronize external devices to the converter clock.
43	DCLKP	True Clock Output. This output provides an LVDS-compatible output level and can be used to synchronize external devices to the converter clock.
46	D6N	Complementary Output Bit 6
47	D6P	True Output Bit 6
48	D7N	Complementary Output Bit 7
49	D7P	True Output Bit 7
50	D8N	Complementary Output Bit 8
51	D8P	True Output Bit 8
52	D9N	Complementary Output Bit 9
53	D9P	True Output Bit 9
54	D10N	Complementary Output Bit 10
55	D10P	True Output Bit 10
56	D11N	Complementary Output Bit 11 (MSB)
57	D11P	True Output Bit 11 (MSB)
58	ORN	Complementary Out-of-Range Control Bit Output. If an out-of-range condition is detected, bit ORN flags this condition by transitioning low.
59	ORP	True Out-of-Range Control Bit Output. If an out-of-range condition is detected, bit ORP flags this condition by transitioning high.
68	$\bar{T}/B$	Output Format Select. This LVCMOS-compatible input controls the digital output format of the MAX1214N. $\bar{T}/B$ has an internal pulldown resistor. $\bar{T}/B = 0$ : Two's-complement output format. $\bar{T}/B = 1$ : Binary output format.
—	EP	Exposed Paddle. The exposed paddle is located on the backside of the chip and must be connected to AGND.

# 1.8V, Low-Power, 12-Bit, 210MSPS ADC for Broadband Applications

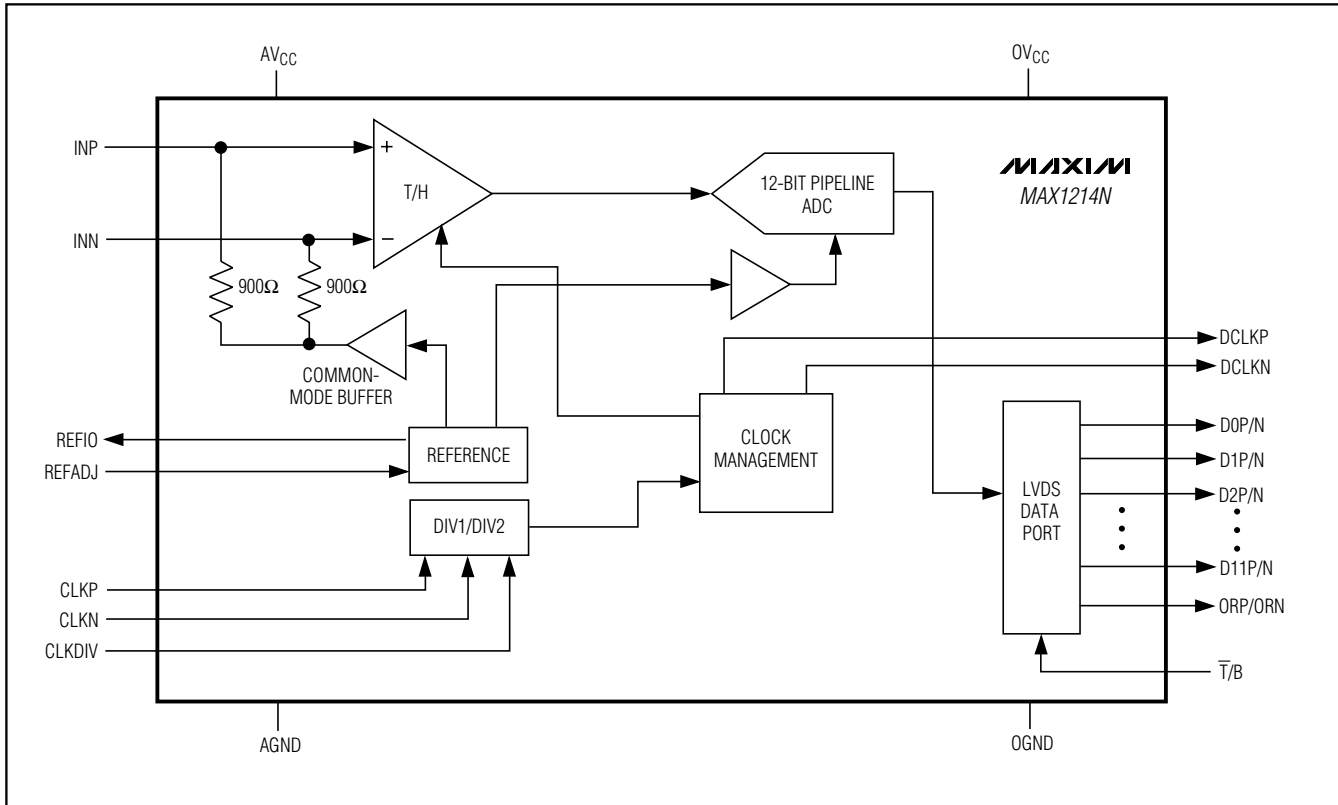


Figure 1. Block Diagram

## Detailed Description— Theory of Operation

The MAX1214N uses a fully differential pipelined architecture that allows for high-speed conversion, optimized accuracy, and linearity while minimizing power consumption.

Both positive (INP) and negative/complementary analog input terminals (INN) are centered around a 0.7V common-mode voltage, and accept a differential analog input voltage swing of  $\pm V_{FS} / 4$  each, resulting in a typical 1.39V<sub>P-P</sub> differential full-scale signal swing. Inputs INP and INN are sampled when the differential sampling clock signal transitions high. When using the clock-divide mode, the analog inputs are sampled at every other high transition of the differential sampling clock.

Each pipeline converter stage converts its input voltage to a digital output code. At every stage, except the last, the error between the input voltage and the digital output code is multiplied and passed along to the next

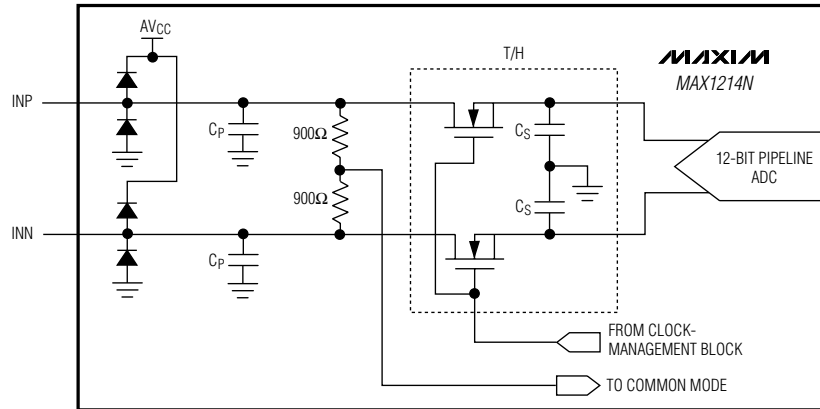
pipeline stage. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes. The result is a 12-bit parallel digital output word in user-selectable two's-complement or offset binary output formats with LVDS-compatible output levels. See Figure 1 for a more detailed view of the MAX1214N architecture.

### Analog Inputs (INP, INN)

INP and INN are the fully differential inputs of the MAX1214N. Differential inputs usually feature good rejection of even-order harmonics, which allows for enhanced AC performance as the signals are progressing through the analog stages. The MAX1214N analog inputs are self-biased at a 0.7V common-mode voltage and allow a 1.39V<sub>P-P</sub> differential input voltage swing (Figure 2). Both inputs are self-biased through 900Ω resistors, resulting in a typical differential input resistance of 1.8kΩ. Drive the analog inputs of the MAX1214N in AC-coupled configuration to achieve the best dynamic performance. See the *Transformer-Coupled, Differential Analog Input Drive* section.

# 1.8V, Low-Power, 12-Bit, 210MSPS ADC for Broadband Applications

MAX1214N



$C_S$  IS THE SAMPLING CAPACITANCE.  
 $C_P$  IS THE PARASITIC CAPACITANCE - 1pF.

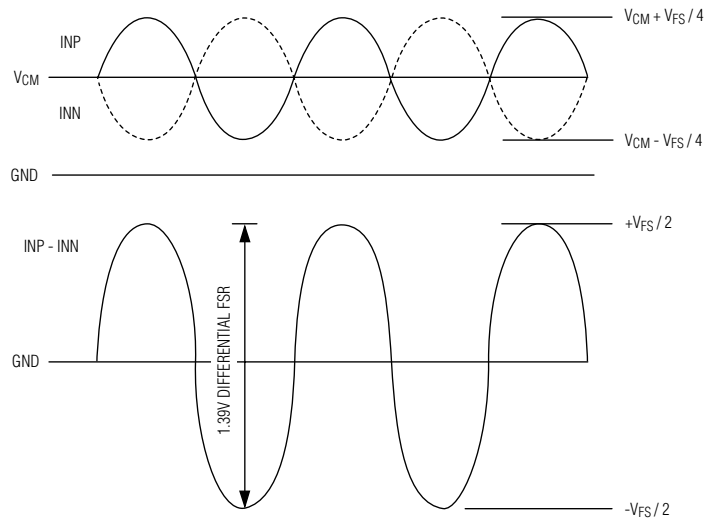


Figure 2. Simplified Analog Input Architecture and Allowable Input Voltage Range



# 1.8V, Low-Power, 12-Bit, 210Mps ADC for Broadband Applications

MAX1214N

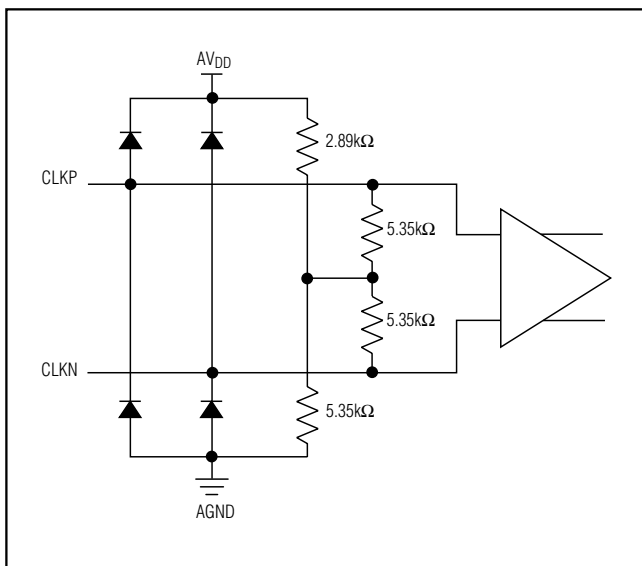


Figure 4. Simplified Clock Input Architecture

## System Timing Requirements

Figure 5 shows the relationship between the clock input and output, analog input, sampling event, and data output. The MAX1214N samples on the rising (falling) edge of CLKP (CLKN). Output data is valid on the next rising (falling) edge of the DCLKP (DCLKN) clock, but has an internal latency of 11 clock cycles.

## Digital Outputs (D0P/N–D11P/N, DCLKP/N, ORP/N) and Control Input $\bar{T}/B$

Digital outputs D0P/N–D11P/N, DCLKP/N, and ORP/N are LVDS compatible, and data on D0P/N–D11P/N is presented in either binary or two's-complement format (Table 1). The  $\bar{T}/B$  control line is an LVCMOS-compatible input, which allows the user to select the desired output format. Pulling  $\bar{T}/B$  low outputs data in two's complement and pulling it high presents data in offset binary format on the 12-bit parallel bus.  $\bar{T}/B$  has an internal pulldown resistor and may be left unconnected in applications using only two's-complement output format. All LVDS outputs provide a typical 0.325V voltage swing around a 1.2V common-mode voltage, and must be terminated at the far end of each transmission line pair (true and complementary) with 100Ω. Apply a 1.7V to 1.9V voltage supply at  $OV_{CC}$  to power the LVDS outputs.

The MAX1214N offers an additional differential output pair (ORP, ORN) to flag out-of-range conditions, where out-of-range is above positive or below negative full scale. An out-of-range condition is identified with ORP (ORN) transitioning high (low).

**Note:** Although a differential LVDS output architecture reduces single-ended transients to the supply and ground planes, capacitive loading on the digital outputs should still be kept as low as possible. Using LVDS buffers on the digital outputs of the ADC when driving larger loads may improve overall performance and reduce system-timing constraints.

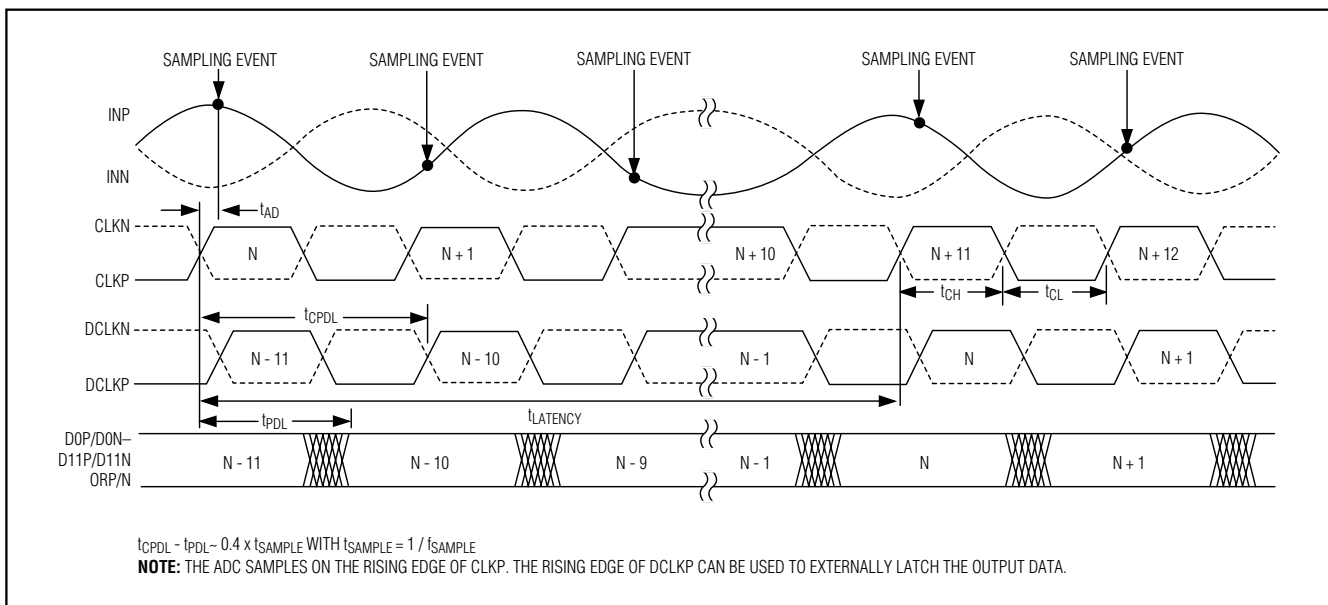


Figure 5. System and Output Timing Diagram

# 1.8V, Low-Power, 12-Bit, 210Mps ADC for Broadband Applications

**Table 1. MAX1214N Digital Output Coding**

INP ANALOG INPUT VOLTAGE LEVEL	INN ANALOG INPUT VOLTAGE LEVEL	OUT-OF-RANGE ORP (ORN)	BINARY DIGITAL OUTPUT CODE (D11P/N–D0P/N)	TWO'S-COMPLEMENT DIGITAL OUTPUT CODE (D11P/N–D0P/N)
$> V_{CM} + V_{FS} / 4$	$< V_{CM} - V_{FS} / 4$	1 (0)	1111 1111 1111 (exceeds +FS, OR set)	0111 1111 1111 (exceeds +FS, OR set)
$V_{CM} + V_{FS} / 4$	$V_{CM} - V_{FS} / 4$	0 (1)	1111 1111 1111 (+FS)	0111 1111 1111 (+FS)
$V_{CM}$	$V_{CM}$	0 (1)	1000 0000 0000 or 0111 1111 1111 (FS/2)	0000 0000 0000 or 1111 1111 1111 (FS/2)
$V_{CM} - V_{FS} / 4$	$V_{CM} + V_{FS} / 4$	0 (1)	0000 0000 0000 (-FS)	1000 0000 0000 (-FS)
$< V_{CM} + V_{FS} / 4$	$> V_{CM} - V_{FS} / 4$	1 (0)	0000 0000 0000 (exceeds -FS, OR set)	1000 0000 0000 (exceeds -FS, OR set)

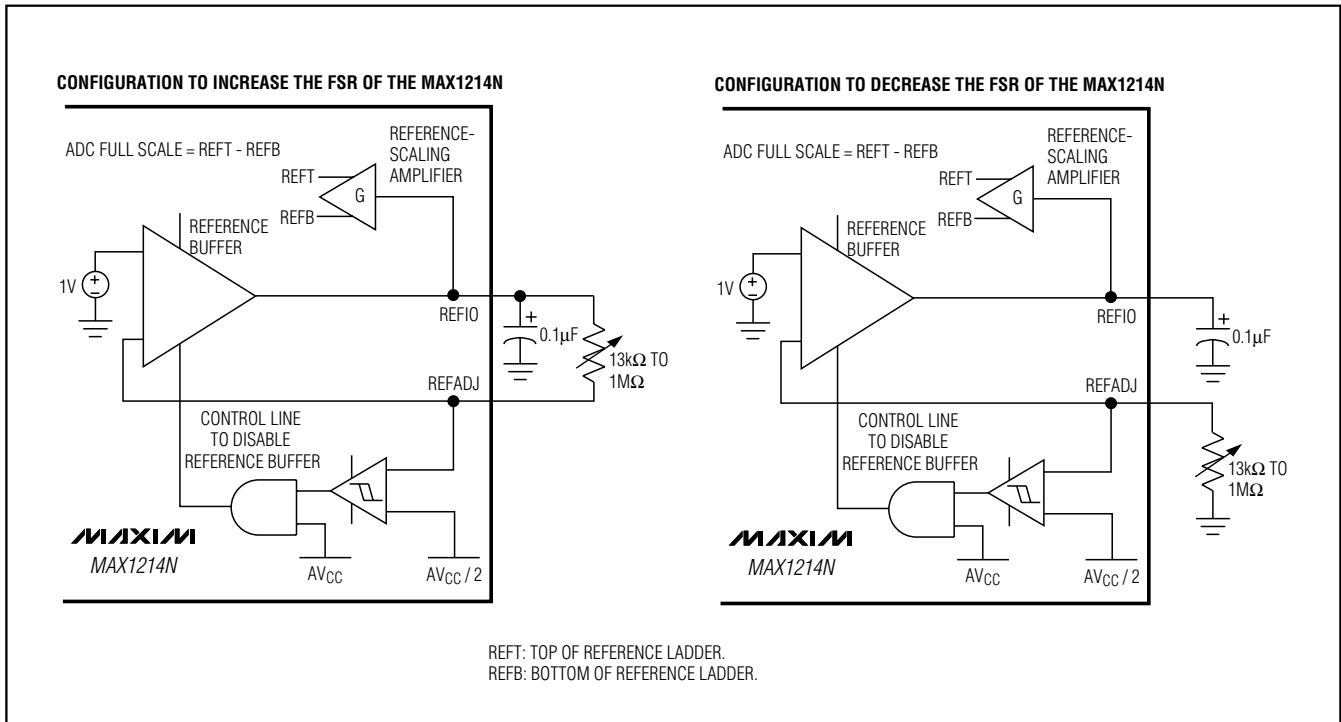


Figure 6a. Circuit Suggestions to Adjust the ADC's Full-Scale Range

## Applications Information

### FSR Adjustments Using the Internal Bandgap Reference

The MAX1214N supports a 10% ( $\pm 5\%$ ) full-scale adjustment range. To decrease the full-scale signal range, add an external resistor value ranging from 13k $\Omega$  to 1M $\Omega$  between REFADJ and AGND. Adding a variable resistor, potentiometer, or predetermined resis-

tor value between REFADJ and REFIO increases the FSR of the data converter. Figure 6a shows the two possible configurations and their impact on the overall full-scale range adjustment of the MAX1214N. Do not use resistor values of less than 13k $\Omega$  to avoid instability of the internal gain regulation loop for the bandgap reference. See Figure 6b for the resulting FSR for a series of resistor values.

# 1.8V, Low-Power, 12-Bit, 210Mps ADC for Broadband Applications

**MAX1214N**

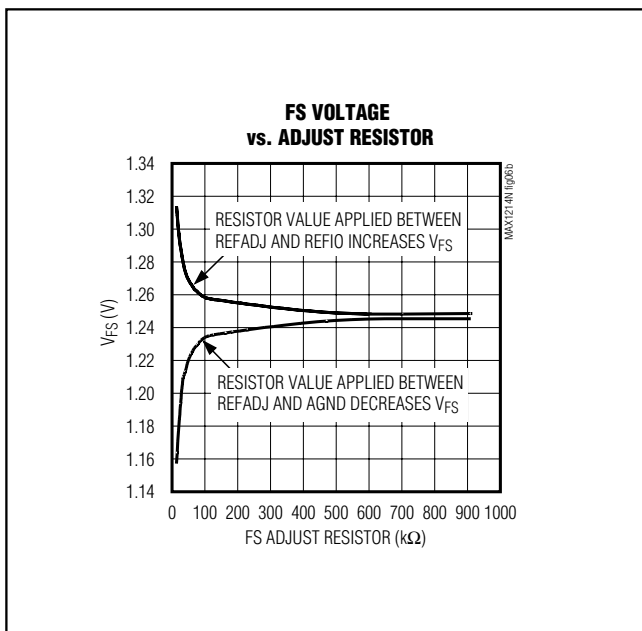


Figure 6b. FS Adjustment Range vs. FS Adjustment Resistor

## Differential, AC-Coupled, LVPECL-Compatible Clock Input

The MAX1214N dynamic performance depends on the use of a very clean clock source. The phase noise floor of the clock source has a negative impact on the SNR performance. Spurious signals on the clock signal source also affect the ADC's dynamic range. The preferred method of clocking the MAX1214N is differentially with LVDS- or LVPECL-compatible input levels. The fast data transition rates of these logic families minimize the clock-input circuitry's transition uncertainty, thereby improving the SNR performance. To accomplish this, a 50Ω reverse-terminated clock signal source with low phase noise is AC-coupled into a fast differential receiver such as the MC100LVEL16 (Figure 7). The receiver produces the necessary LVPECL output levels to drive the clock inputs of the data converter.

## Transformer-Coupled, Differential Analog Input Drive

The MAX1214N provides the best SFDR and THD with fully differential input signals and it is not recommended to drive the ADC inputs in single-ended configuration. In differential input mode, even-order harmonics are usually lower since INP and INN are balanced, and

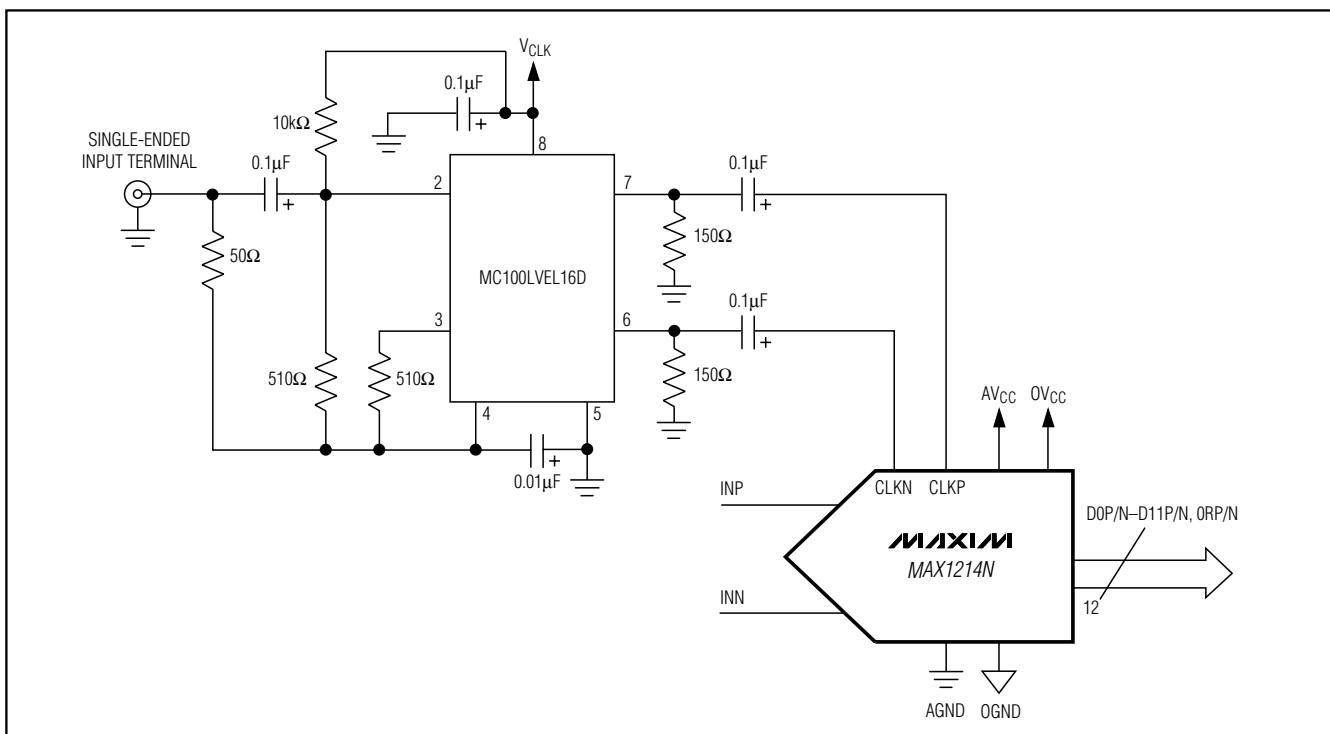


Figure 7. Differential, AC-Coupled, PECL-Compatible Clock Input Configuration

# 1.8V, Low-Power, 12-Bit, 210Msps ADC for Broadband Applications

each of the ADC inputs only requires half the signal swing compared to a single-ended configuration.

Wideband RF transformers provide an excellent solution to convert a single-ended signal to a fully differential signal, required by the MAX1214N to reach its optimum dynamic performance. Apply a secondary-side termination of a 1:1 transformer (e.g., Mini-Circuit's ADT1-1WT) into two separate 24.9Ω resistors. Higher source impedance values can be used at the expense of degradation in dynamic performance. This configuration optimizes THD and SFDR performance of the ADC by reducing the effects of transformer parasitics. However, the source impedance combined with the shunt capacitance provided by a PC board and the ADC's parasitic capacitance limit the ADC's full-power input bandwidth.

To further enhance THD and SFDR performance at high input frequencies (> 100MHz), a second transformer (Figure 8) should be placed in series with the single-ended-to-differential conversion transformer. This transformer reduces the increase of even-order harmonics at high frequencies.

### Single-Ended, AC-Coupled Analog Inputs

Although not recommended, the MAX1214N can be used in single-ended mode (Figure 9). AC-couple the analog signals to the positive input INP through a 0.1μF capacitor terminated with a 49.9Ω resistor to AGND. Terminate the negative input INN with a 49.9Ω resistor in series with a 0.1μF capacitor to AGND. In single-ended mode, the input range is limited to approximately half of the FSR of the device, and dynamic performance usually degrades.

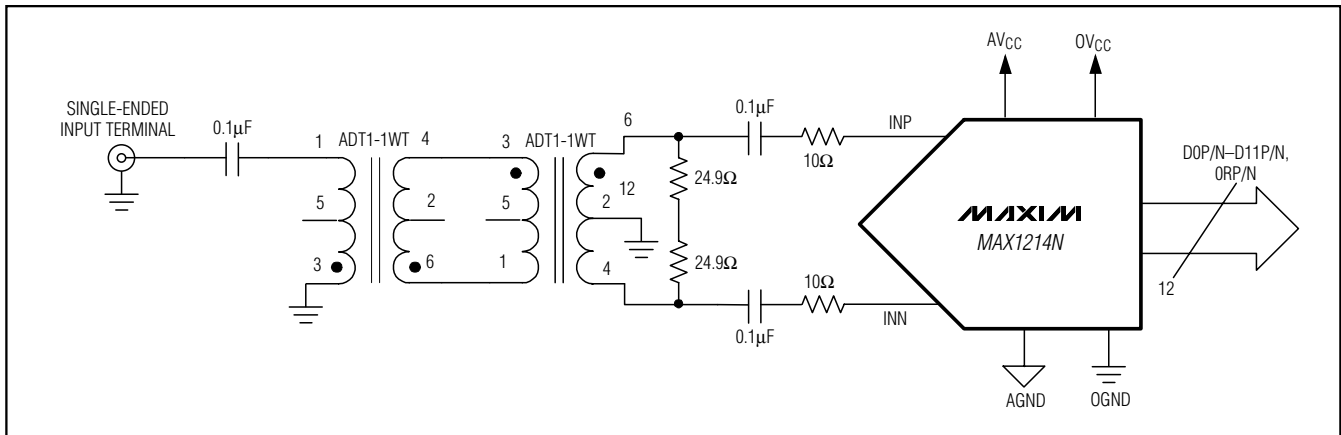


Figure 8. Analog Input Configuration with Back-to-Back Transformers and Secondary-Side Termination

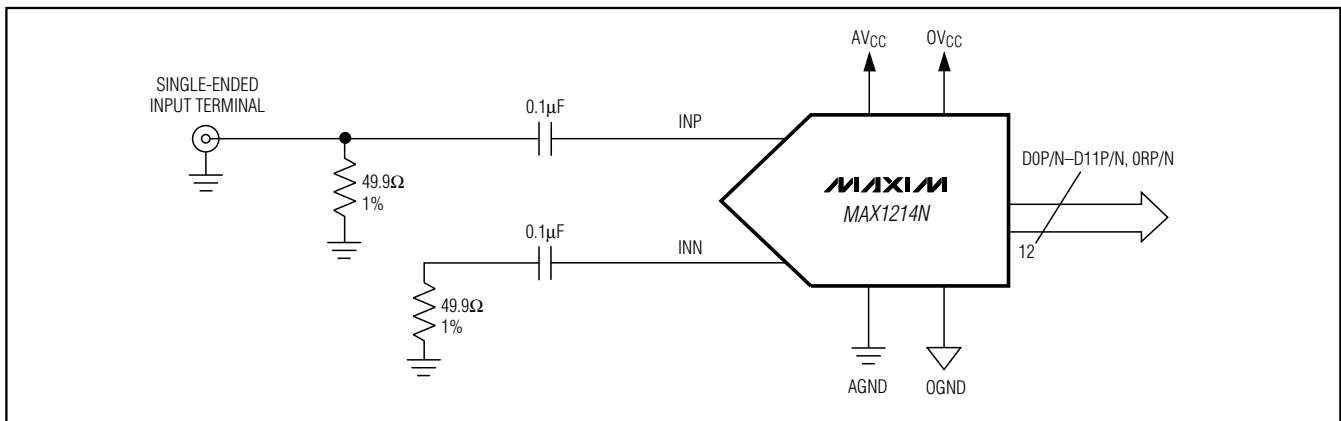


Figure 9. Single-Ended, AC-Coupled Analog Input Configuration



# 1.8V, Low-Power, 12-Bit, 210MSPS ADC for Broadband Applications

## Grounding, Bypassing, and Board Layout Considerations

The MAX1214N requires board-layout design techniques suitable for high-speed data converters. This ADC provides separate analog and digital power supplies. The analog and digital supply voltage pins accept 1.7V to 1.9V input voltage ranges. Although both supply types can be combined and supplied from one source, it is recommended to use separate sources to cut down on performance degradation caused by digital switching currents, which can couple into the analog supply network. Isolate analog and digital supplies (AV<sub>CC</sub> and OV<sub>CC</sub>) where they enter the PC board with separate networks of ferrite beads and capacitors to their corresponding grounds (AGND, OGND).

To achieve optimum performance, provide each supply with a separate network of a 47 $\mu$ F tantalum capacitor and parallel combinations of 10 $\mu$ F and 1 $\mu$ F ceramic capacitors. Additionally, the ADC requires each supply pin to be bypassed with separate 0.1 $\mu$ F ceramic capacitors (Figure 10). Locate these capacitors directly at the ADC supply pins or as close as possible to the MAX1214N. Choose surface-mount capacitors, whose preferred location should be on the same side as the converter to save space and minimize the inductance. If close placement on the same side is not possible, these bypassing capacitors may be routed through vias to the bottom side of the PC board.

Multilayer boards with separated ground and power planes produce the highest level of signal integrity. Consider the use of a split ground plane arranged to

match the physical location of analog and digital ground on the ADC's package. The two ground planes should be joined at a single point so the noisy digital ground currents do not interfere with the analog ground plane. The dynamic currents that may need to travel long distances before they are recombined at a common source ground, resulting in large and undesirable ground loops, are a major concern with this approach. Ground loops can degrade the input noise by coupling back to the analog front-end of the converter, resulting in increased spurious activity, leading to decreased noise performance.

Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy, digital systems ground. To minimize the coupling of the digital output signals from the analog input, segregate the digital output bus carefully from the analog input circuitry. To further minimize the effects of digital noise coupling, ground return vias can be positioned throughout the layout to divert digital switching currents away from the sensitive analog sections of the ADC. This approach does not require split ground planes, but can be accomplished by placing substantial ground connections between the analog front-end and the digital outputs.

The MAX1214N is packaged in a 68-pin QFN-EP package (**package code: G6800-4**), providing greater design flexibility, increased thermal dissipation, and optimized AC performance of the ADC. **The exposed paddle (EP) must be soldered down to AGND.**

In this package, the data converter die is attached to an EP lead frame with the back of this frame exposed

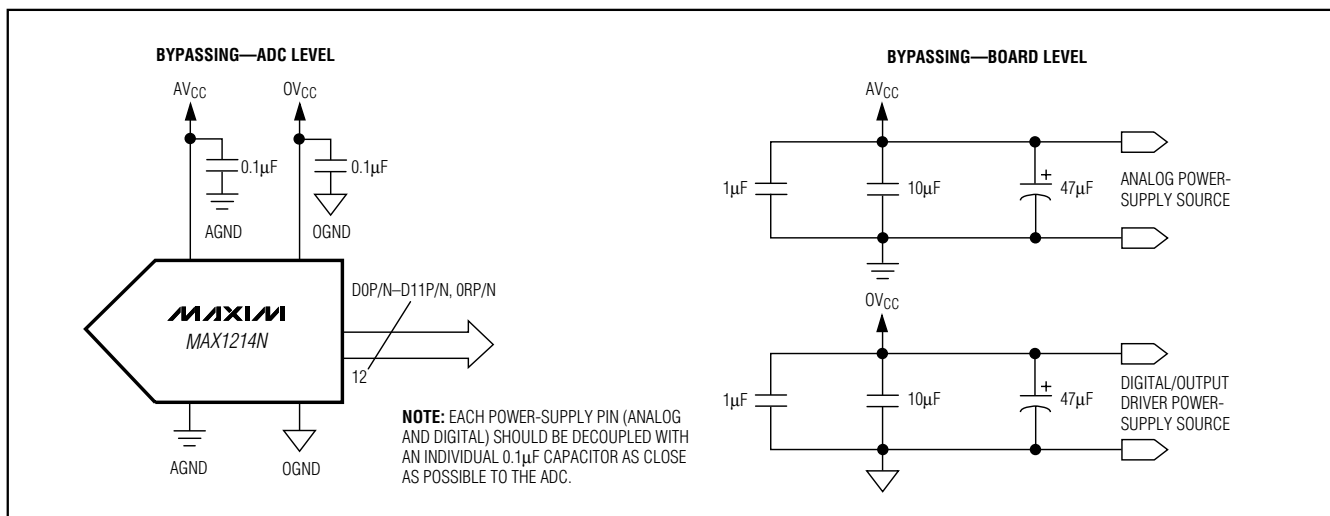


Figure 10. Grounding, Bypassing, and Decoupling Recommendations for the MAX1214N

# 1.8V, Low-Power, 12-Bit, 210Msps ADC for Broadband Applications

at the package bottom surface, facing the PC board side of the package. This allows a solid attachment of the package to the board with standard infrared (IR) flow soldering techniques.

Thermal efficiency is one of the factors for selecting a package with an exposed paddle for the MAX1214N. The exposed paddle improves thermal and ensures a solid ground connection between the ADC and the PC board's analog ground layer.

Considerable care must be taken when routing the digital output traces for a high-speed, high-resolution data converter. Keep trace lengths at a minimum and place minimal capacitive loading (less than 5pF) on any digital trace to prevent coupling to sensitive analog sections of the ADC. It is recommended running the LVDS output traces as differential lines with 100Ω matched impedance from the ADC to the LVDS load device.

## Static Parameter Definitions

### Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1214N are measured using the histogram method with a 10MHz input frequency.

### Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. The MAX1214N's DNL specification is measured with the histogram method based on a 10MHz input tone.

## Dynamic Parameter Definitions

### Aperture Jitter

Figure 11 shows the aperture jitter ( $t_{AJ}$ ), which is the sample-to-sample variation in the aperture delay.

### Aperture Delay

Aperture delay ( $t_{AD}$ ) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 11).

### Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$\text{SNR}_{[\text{max}]} = 6.02 \times N + 1.76$$

In reality, other noise sources such as thermal noise, clock jitter, signal phase noise, and transfer function nonlinearities also contribute to the SNR calculation and should be considered when determining the signal-to-noise ratio in ADC. The SNR for the MAX1214N is specified in decibels (dB), however, SNR can also be specified in dBFS. To obtain the SNR in dBFS, simply subtract the amplitude of the input tone (this number is given in dBFS) at which the SNR is measured from the SNR number in dB. For example, an ADC having an SNR of 67dB resulting from an input tone with amplitude -1dBFS will have an SNR of 67 - (-1) = 68dBFS.

### Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components excluding the fundamental and the DC offset. In the case of the MAX1214N, SINAD is computed from a curve fit.

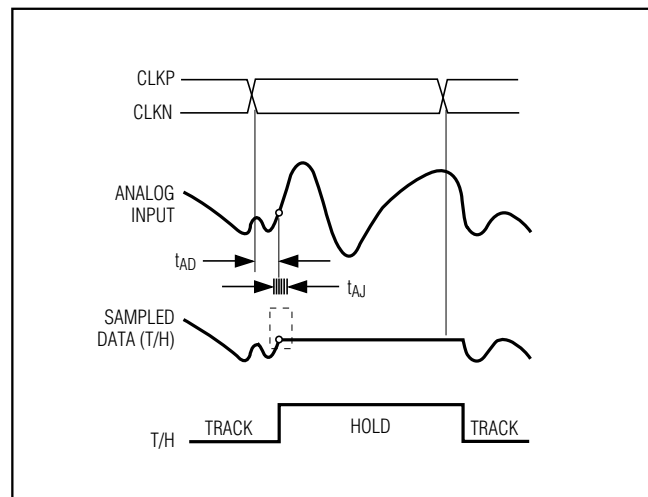


Figure 11. Aperture Jitter/Delay Specifications

# 1.8V, Low-Power, 12-Bit, 210MSPS ADC for Broadband Applications

## Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the carrier frequency (maximum signal component) to the RMS value of the next-largest noise or harmonic distortion component. SFDR is usually measured in dBc with respect to the carrier frequency amplitude or in dBFS with respect to the ADC's full-scale range.

## Intermodulation Distortion (IMD)

IMD is the ratio of the RMS sum of the intermodulation products to the RMS sum of the two fundamental input tones. This is expressed as:

$$IMD = 20 \times \log \left( \frac{\sqrt{V_{IM1}^2 + V_{IM2}^2 + \dots + V_{IM3}^2 + V_{IMn}^2}}{\sqrt{V_1^2 + V_2^2}} \right)$$

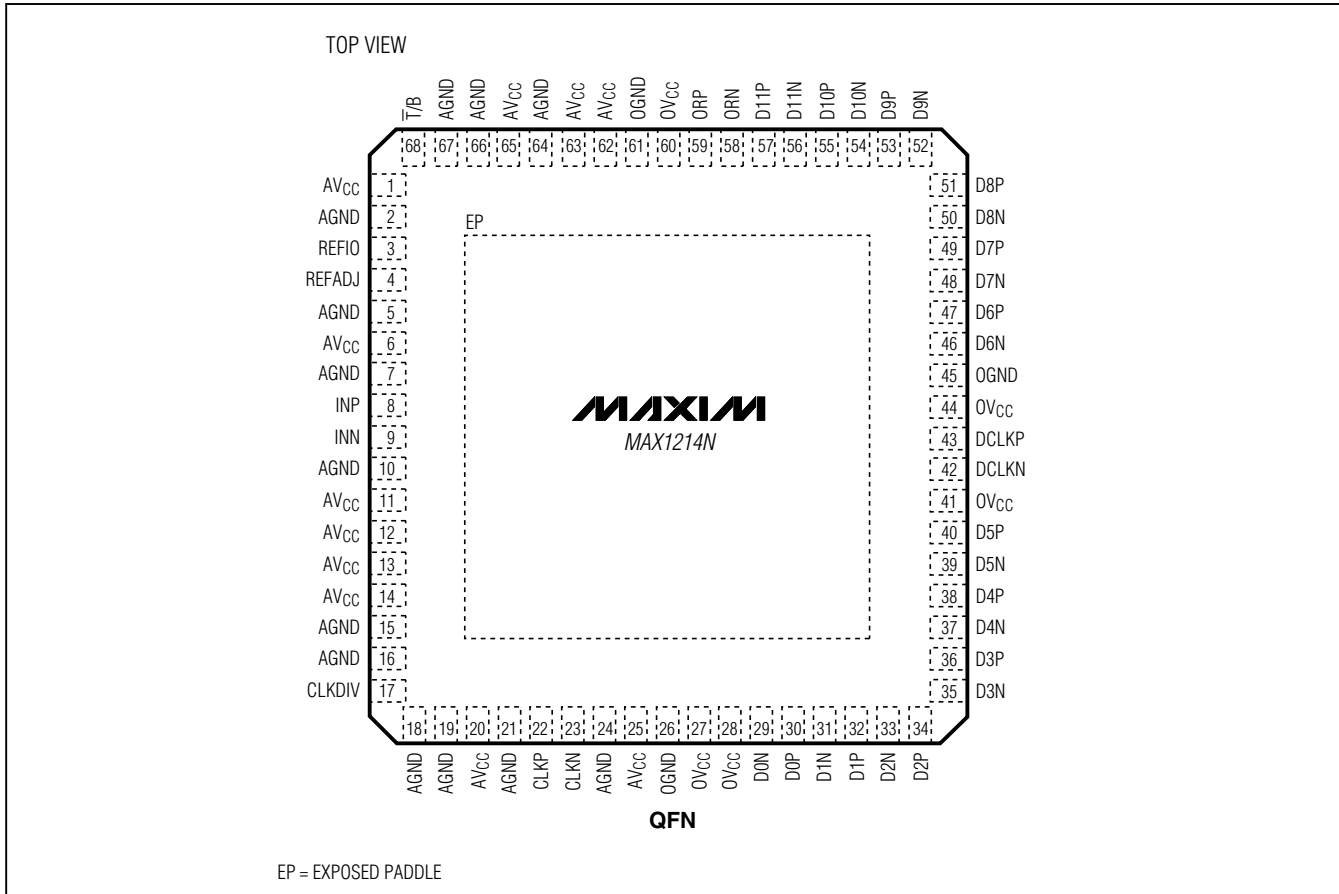
The fundamental input tone amplitudes (V1 and V2) are at -7dBFS. The intermodulation products are the amplitudes of the output spectrum at the following frequencies:

- Second-order intermodulation products:  $f_{IN1} + f_{IN2}$ ,  $f_{IN2} - f_{IN1}$
- Third-order intermodulation products:  $2 \times f_{IN1} - f_{IN2}$ ,  $2 \times f_{IN2} - f_{IN1}$ ,  $2 \times f_{IN1} + f_{IN2}$ ,  $2 \times f_{IN2} + f_{IN1}$
- Fourth-order intermodulation products:  $3 \times f_{IN1} - f_{IN2}$ ,  $3 \times f_{IN2} - f_{IN1}$ ,  $3 \times f_{IN1} + f_{IN2}$ ,  $3 \times f_{IN2} + f_{IN1}$
- Fifth-order intermodulation products:  $3 \times f_{IN1} - 2 \times f_{IN2}$ ,  $3 \times f_{IN2} - 2 \times f_{IN1}$ ,  $3 \times f_{IN1} + 2 \times f_{IN2}$ ,  $3 \times f_{IN2} + 2 \times f_{IN1}$

## Full-Power Bandwidth

A large -1dBFS analog input signal is applied to an ADC and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. The -3dB point is defined as the full-power input bandwidth frequency of the ADC.

## Pin Configuration

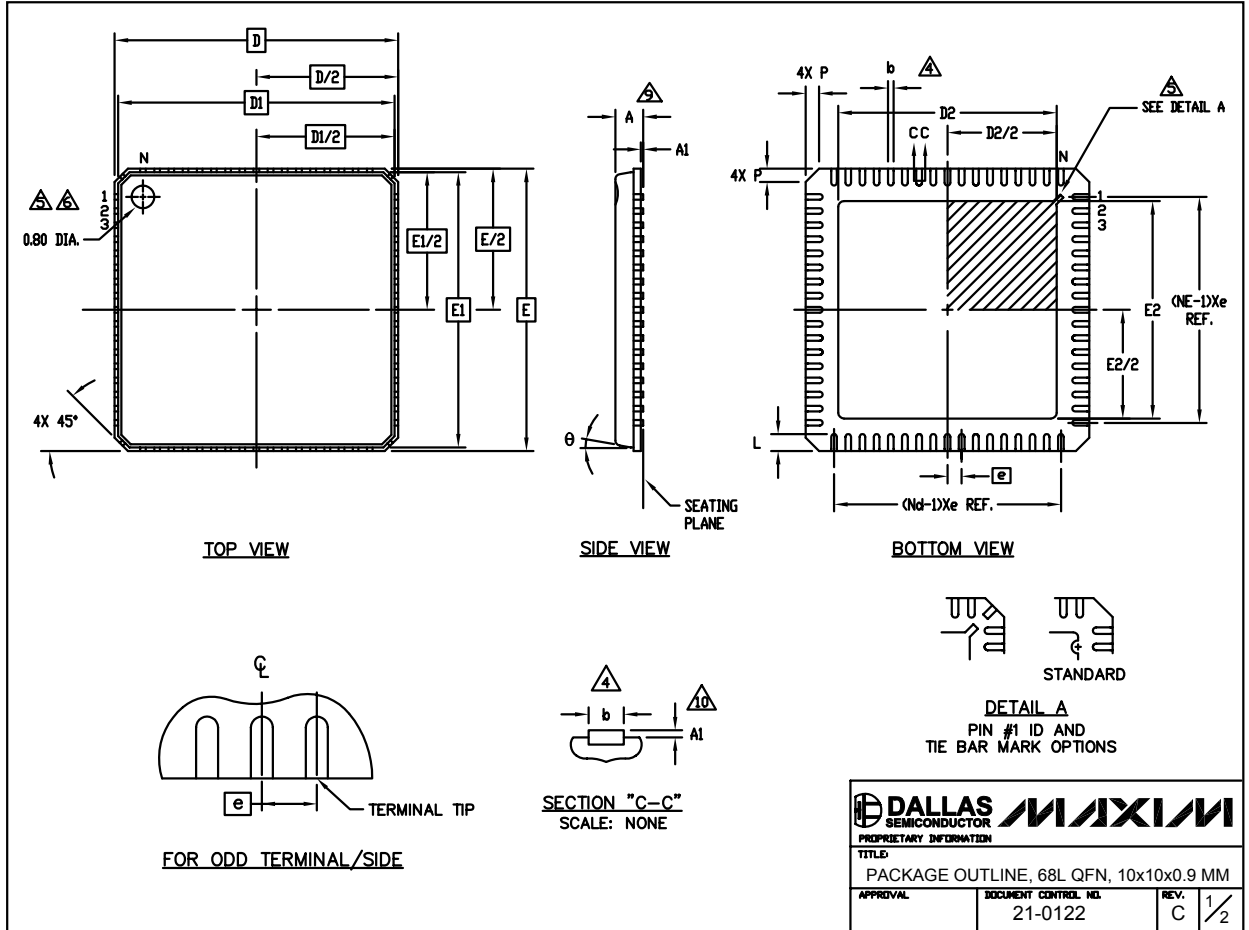


# 1.8V, Low-Power, 12-Bit, 210MSPs ADC for Broadband Applications

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

For the MAX1214N, the package code is G6800-4.









# 1.8V, Low-Power, 12-Bit, 210MSPS ADC for Broadband Applications

MAX1214N

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	—	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D	10.00 BSC			
D1	9.75 BSC			
e	0.50 BSC			
E	10.00 BSC			
E1	9.75 BSC			
L	0.50	0.60	0.65	
N	68			3
Nd	17			3
Ne	17			3
θ	0		12°	
P	0	0.42	0.60	

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.  
 N IS THE NUMBER OF TERMINALS.  
 Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &  
 Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.  

4. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.  

5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.  

7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.10mm.
9. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS  

10. APPLIES ONLY TO TERMINALS.  

11. MEETS JEDEC MO-220.

EXPOSED PAD VARIATIONS						
PKG CODE	D2			E2		
	MIN	NOM	MAX	MIN	NOM	MAX
G6800-2	7.55	7.70	7.85	7.55	7.70	7.85
G6800-4	5.65	5.80	5.95	5.65	5.80	5.95

 	
<small>PROPRIETARY INFORMATION</small>	
<small>TITLE:</small> PACKAGE OUTLINE, 68L QFN, 10x10x0.9 MM	
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO.</small> 21-0122
<small>REV.</small> C	<small>REV.</small> 1/2

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