

Development Board EPC9006C - Rev. 3.0 Quick Start Guide

EPC2007C

100 V Half Bridge with Gate Drive



DESCRIPTION

The EPC9006C development board is a 100 V maximum device voltage, 7 A maximum output current, half bridge with onboard gate drives, featuring the EPC2007C enhancement mode (eGaN®) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2007C eGaN FET by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9006C development board is 2" x 1.5" and contains two EPC2007C eGaN FETs in a half bridge configuration using, the Texas Instruments LM5113 gate driver, supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2007Cs eGaN FET please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

QUICK START GUIDE

Development board EPC9006C is easy to set up to evaluate the performance of the EPC2007C eGaN FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to +V_{IN} (J5, J6) and ground / return to -V_{IN} (J7, J8).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive supply to +V_{DD} (J1, Pin-1) and ground return to -V_{DD} (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the controller / PWM input.
7. Turn on the bus voltage supply, starting a zero, and adjust to the required value (do not exceed the absolute maximum voltage of 100 V on V_{OUT}) and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

Table 1: Performance Summary (T_A = 25°C)

Symbol	Parameter	Conditions	Min	Max	Units
V _{DD}	Gate Drive Input Supply Range		7	12	V
V _{IN}	Bus Input Voltage Range			80*	V
V _{OUT}	Switch Node Output Voltage			100	V
I _{OUT}	Switch Node Output Current			7*	A
V _{PWM}	PWM Logic Input Voltage Threshold	Input 'High' Input 'Low'	3.5 0	6 1.5	V V
	Minimum 'High' State Input Pulse Width	V _{PWM} rise and fall time < 10 ns	50		ns
	Minimum 'Low' State Input Pulse Width	V _{PWM} rise and fall time < 10 ns	100#		ns

*Assumes inductive load, maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermals.

Limited by time needed to 'refresh' high side bootstrap supply voltage.

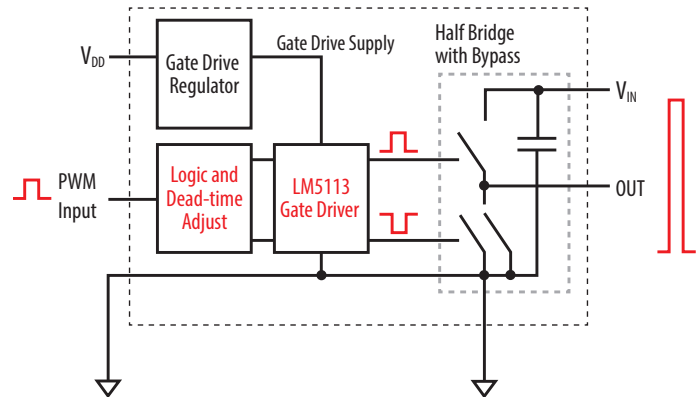


Figure 1: Block Diagram of EPC9006C Development Board

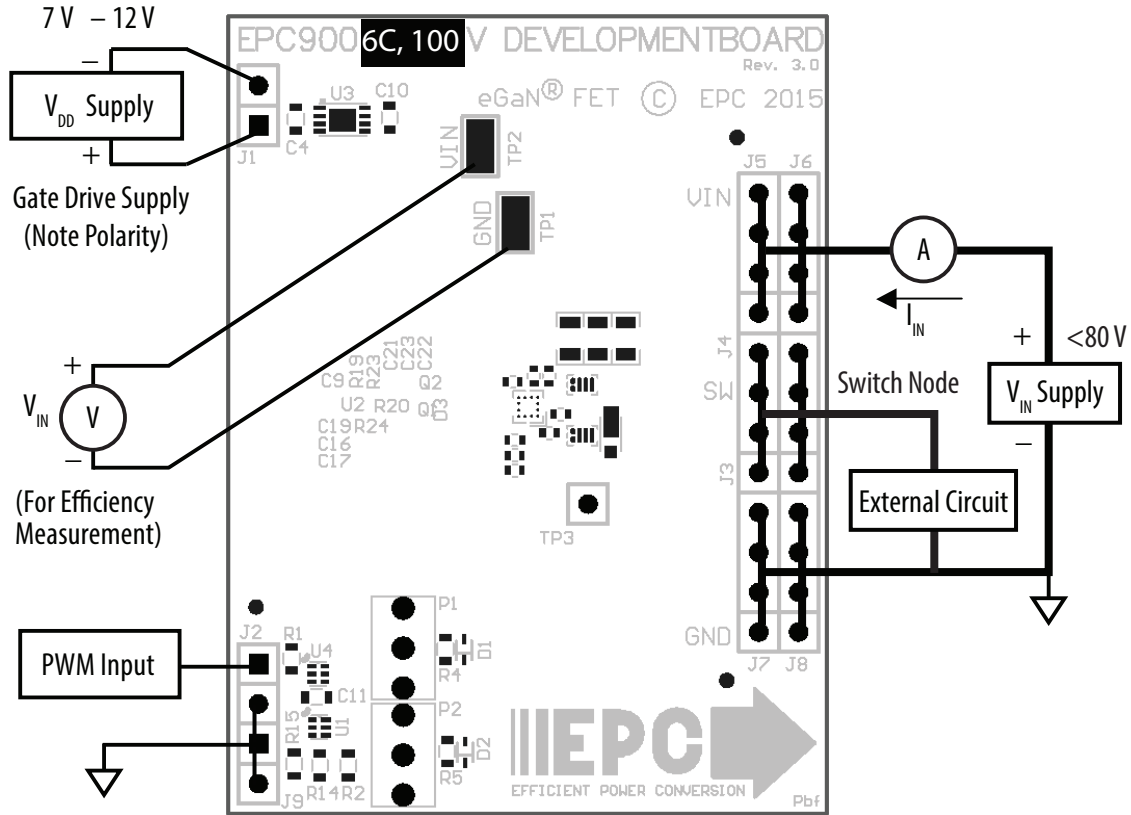


Figure 2: Proper Connection and Measurement Setup

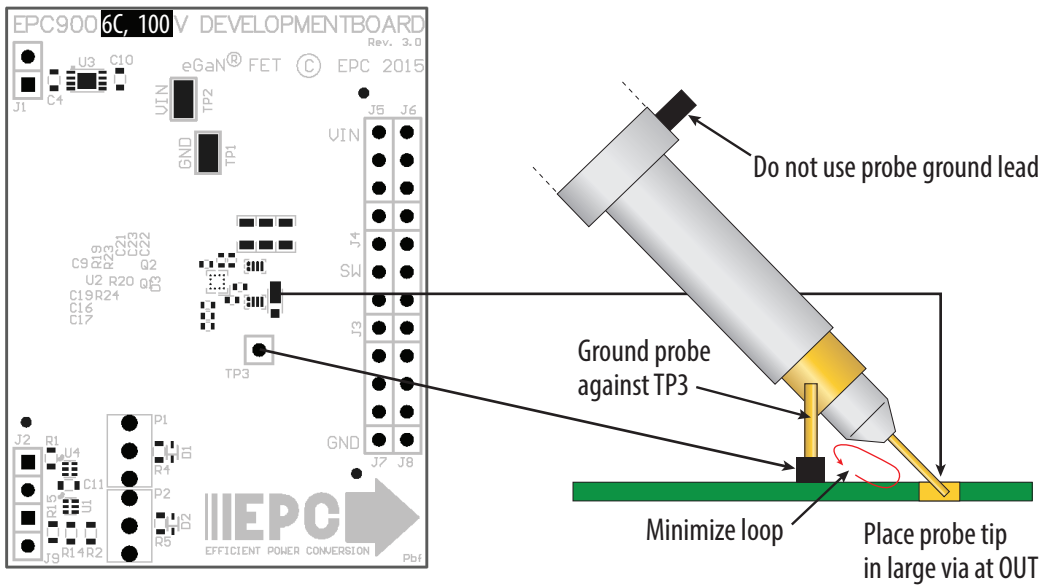


Figure 3: Proper Measurement of Switch Node – V_{SW}

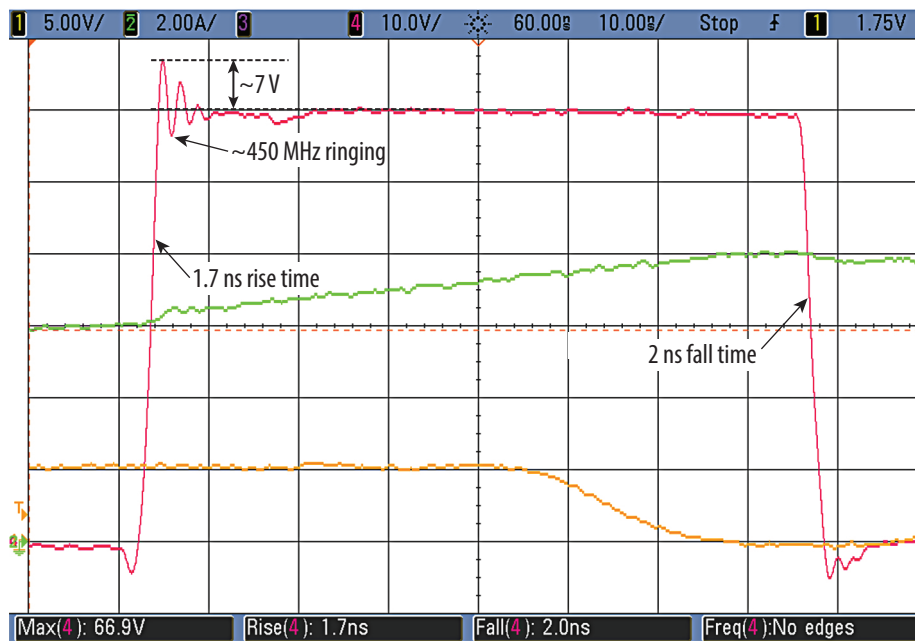


Figure 4: Typical Waveforms for $V_{IN} = 60\text{ V}$ to $2\text{ V}/7\text{ A}$ (500 kHz) Buck converter
 CH1: V_{PWM} Input voltage – CH2: (I_{OUT}) Switch node current – CH4: (V_{OUT}) Switch node voltage

THERMAL CONSIDERATIONS

The EPC9006C development board showcases the EPC2007C eGaN FET. Although the electrical performance surpasses that for traditional silicon devices, their relatively smaller size does magnify the thermal management requirements. The EPC9006C is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-

sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die junction temperature of 150°C.

NOTE. The EPC9006C development board does not have any current or thermal protection on board.

Item	Qty	Reference	Part Description	Manufacturer	Part #
1	3	C4, C10, C11	Capacitor, 1 μF , 10%, 25 V, X5R	Murata	GRM188R61E105KA12D
2	2	C16, C17	Capacitor, 100 pF, 5%, 50 V, NP0	Kemet	C0402C101K5GACTU
3	2	C9, C19	Capacitor, 0.1 μF , 10%, 25 V, X5R	TDK	C1005X5R1E104K
4	3	C21, C22, C23	Capacitor, 1 μF , 10%, 100 V, X7R	TDK	CGA4J3X7S2A105K125AE
5	2	D1, D2	Schottky Diode, 30 V	Diodes Inc.	SDM03U40-7
6	3	J1, J2, J9	Connector	2pins of Tyco	4-103185-0
7	1	J3, J4, J5, J6, J7, J8	Connector	FCI	68602-224HLF
8	2	Q1, Q2	eGaN [®] FET	EPC	EPC2007C
9	1	R1	Resistor, 10.0 K, 5%, 1/8 W	Stackpole	RMCF0603FT10K0
10	2	R2, R15	Resistor, 0 Ω , 1/8 W	Stackpole	RMCF0603ZTOR00
11	1	R4	Resistor, 22 Ω , 1%, 1/8 W	Stackpole	RMCF0603FT22R0
12	1	R5	Resistor, 47 Ω , 1%, 1/8 W	Stackpole	RMCF0603FT47R0
13	6	R19, R20, R23, R24	Resistor, 0 Ω , 1/16 W	Stackpole	RMCF0402ZTOR00
14	2	TP1, TP2	Test Point	Keystone Elect	5015
15	1	TP3	Connector	1/40th of Tyco	4-103185-0
16	1	U1	I.C., Logic	Fairchild	NC7SZ00L6X
17	1	U2	I.C., Gate driver	Texas Instruments	LM5113TME
18	1	U3	I.C., Regulator	Microchip	MCP1703T-5002E/MC
19	1	U4	I.C., Logic	Fairchild	NC7SZ08L6X
20	0	R14	Optional Resistor		
21	0	D3	Optional Diode		
22	0	P1, P2	Optional Potentiometer		

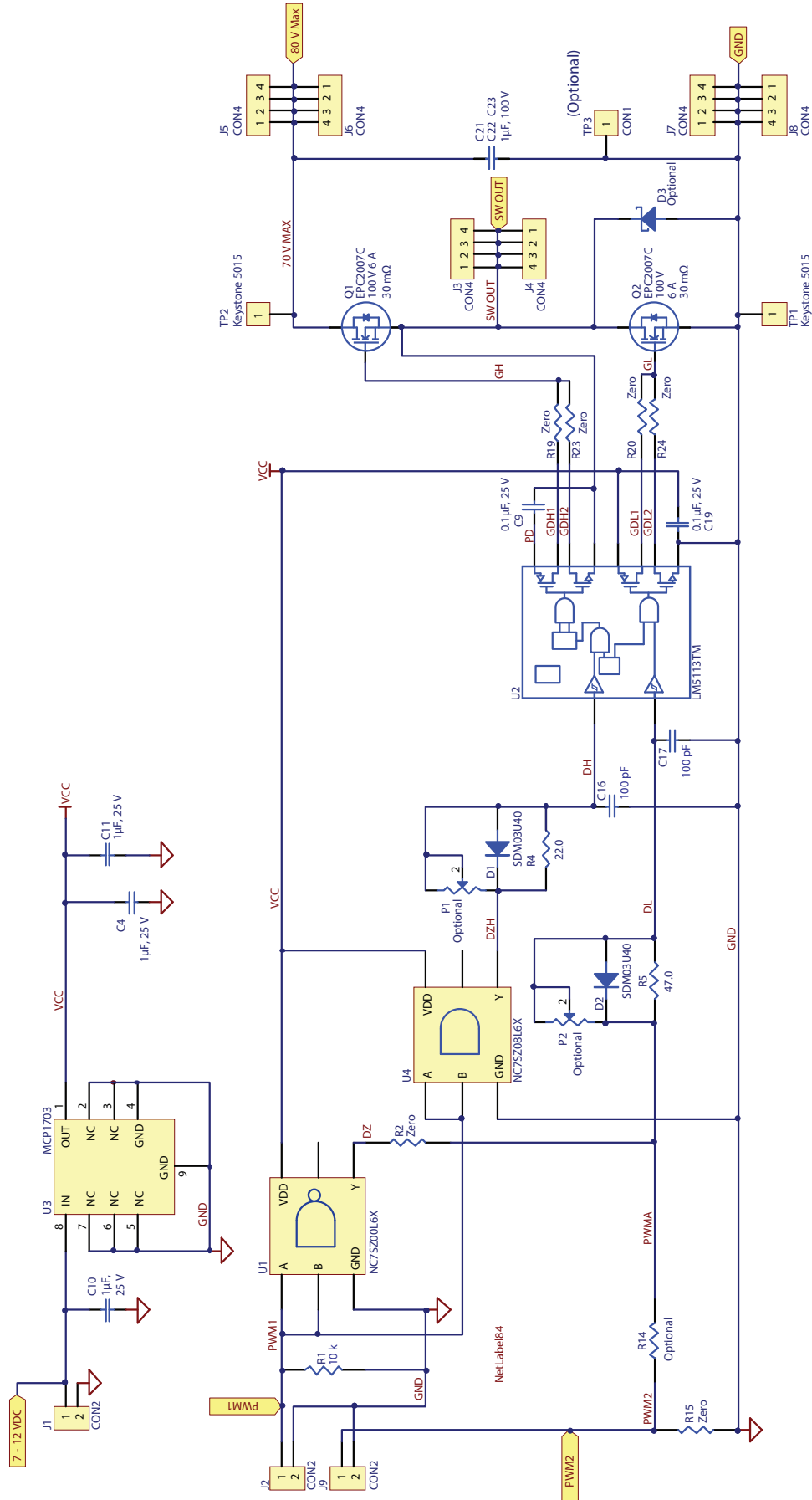


Figure 5: Development Board EPC9006C Schematic

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