R9A02G011

ASSP (USB Power Delivery Controller)

R19DS0088EJ0210
Rev.2.10
Apr. 22, 2022

1. OVERVIEW

The R9A02G011 is a USB Power Delivery Controller that is based on the Universal Serial Bus (USB) Power Delivery Specification Revision 3.1 and USB Type-C™ Cable and Connecter Specification Release 2.1. The R9A02G011 performs negotiation for more current and/or higher voltages over the USB cable (VBUS) than are defined in the USB2.0, USB3.0 or BC1.2 specifications, and controls circuitry to select local power source or power sink. The R9A02G011 uses a 300kbps BMC modulated signal through the CC wire in the USB Type-C™ cable. It comes in two types of packages, 32-pin QFN for easy implementation, and 42-pin BGA for reducing space, so that it can choose according to the application and PCB space. In addition, the R9A02G011 incorporates Renesas' low-power technologies.

1.1 Features

- Compliant with USB Power Delivery Specification Revision 3.1 and USB Type-C™ Cable and Connector Specification Release 2.1
  - Certified by USB Implementers Forum: TID= 64651080009 (Silicon), 1020074 (E-marker)
  - Supports Standard Power Range including Programmable Power Supply
    * Not cover Extended Power Range including Adjustable Voltage Supply
  - Supports IEC63002
  - Supports up to 260 bytes data transfer
  - Supports all USB Type-C™ Connection State Diagrams for USB Type-C™ port control
  - Supports alternate mode and electronically marked cables
  - Supports Dual Role operation and Role Swap protocol
  - Supports Dead Battery operation
- Integrated CC-PHY and CC-logic and many peripheral components
- Single Power Supply with wide voltage range
  - From 3.0 to 5.5V: R9A02G011GNP
  - From 2.7 to 5.5V: R9A02G011GBG
- On-chip Flash ROM, Oscillator, and Power-On-Reset (POR) circuit
- Selectable two types of packages according to the application and PCB space
- Supports SMBus Master and Slave interfaces
- Suitable for Energy Star and EuP specifications for low-power PC peripheral systems.

1.2 Applications

AC Adapter, Power outlet, USB PD Hub, PC, Tablet, Smartphone, Docking Station, PC Peripheral Device (Monitor, Printer, Router, External HDD), Consumer Electronics (DTV, STB, Home Gateway), USB Type-C™ Cable (E-Marker) etc.

Remark E-Marker: Electric marker that can return information about the cable's specifications, its manufacturer, and more.

1.3 Ordering Information

Part Number	Package	Remark
R9A02G011GNP#AC0	32-pin QFN (5 × 5 mm)	Lead-free product
R9A02G011GBG#AC0	42-pin BGA (3.6 x 3.1 mm)	Lead-free product

1.4 Block Diagram

Figure 1-1. R9A02G011 Block Diagram

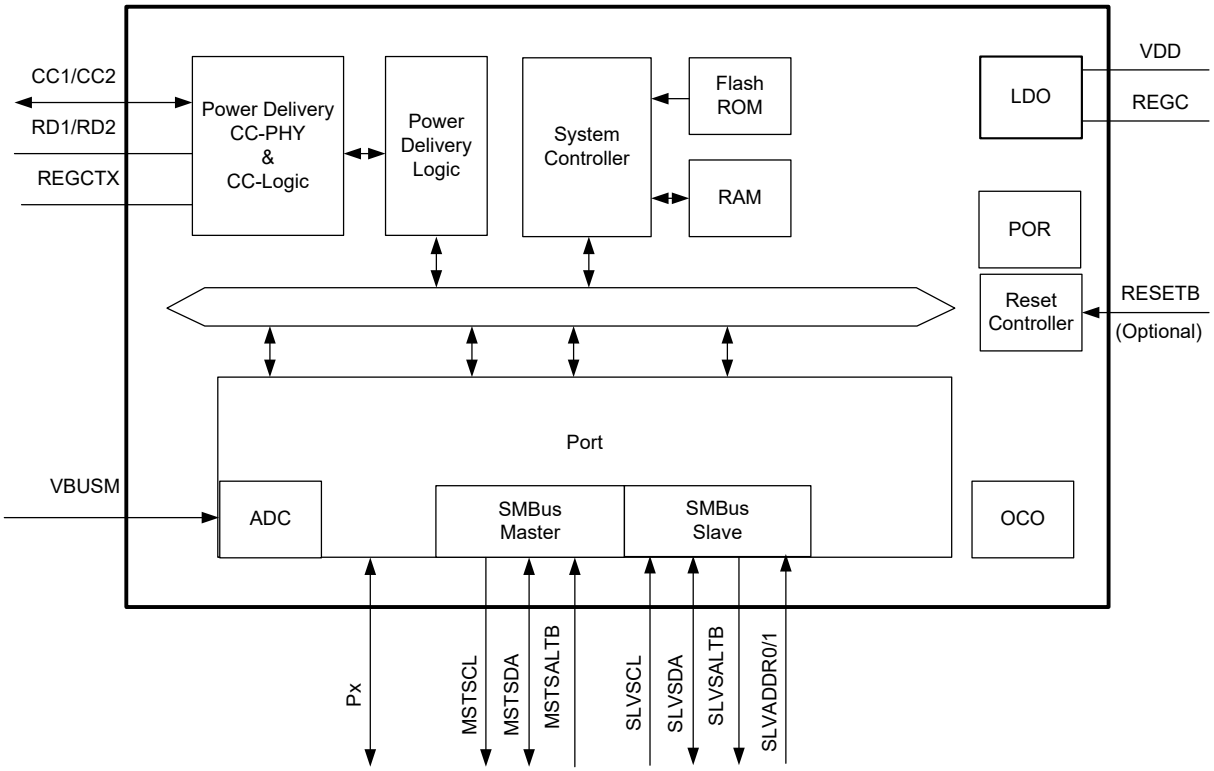


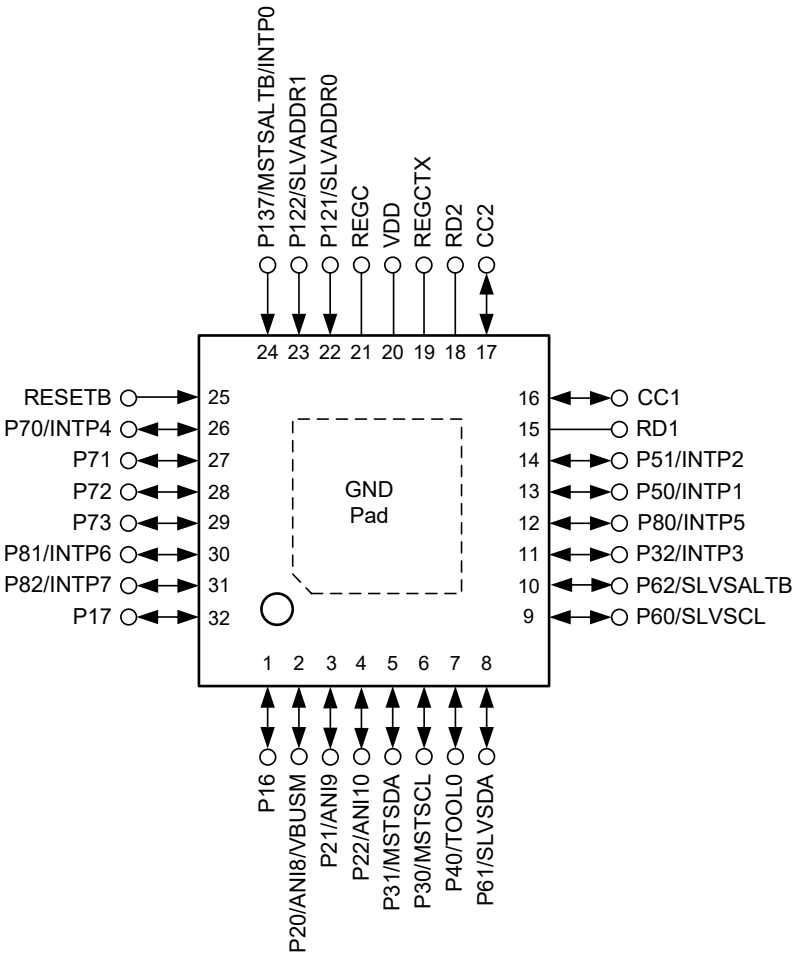
Table 1-1. Terminology

Block Name	Description
Power Delivery CC-PHY & Logic	CC-PHY (Tx/Rx), CC-logic, and LDO used for CC-PHY
Power Delivery Logic	Power Delivery logic controller
System Controller	System CPU core (RL78)
Flash ROM	Internal Flash ROM
RAM	Internal SRAM
SMBus Slave	Interface signals to external SMBus Master.
SMBus Master	Interface signals to external SMBus Slave.
Port	Controls Port I/O signals
OCO	On-Chip Oscillator
POR	Internal Power-On-Reset circuit
Reset Controller	External reset signal (Optional)
ADC	AD Converter
LDO	Low Drop Out regulator integrated in this IC

1.5 Pin Configuration

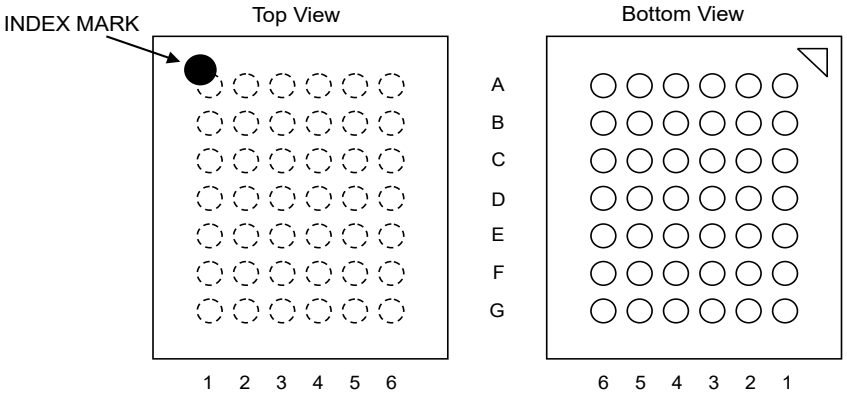
- **32-pin QFN (5 × 5 mm)**

Figure 1-2. Pin Configuration of R9A02G011 32-pin QFN (Top View)



- **42-pin BGA (3.6 x 3.1 mm)**

Figure 1-3. Pin Configuration of R9A02G011 42-pin BGA (Top View)



	1	2	3	4	5	6	
A	VSS	P17	P81/ INTP6	(NC)	RESETB	P137/ MSTSALTB/ INTP0	A
B	VSS	P16	P73	P72	P70/ INTP4	P122/ SLVADDR1	B
C	P21/ ANI9	P20/ ANI8/ VBUSM	P82/ INTP7	P71	P121/ SLVADDR0	REGC	C
D	P30/ MSTSCL	P22/ ANI10	(NC)	VDD	VDD	VDD	D
E	P31/ MSTSDA	(NC)	P32/ INTP3	(NC)	RD2	REGCTX	E
F	(NC)	P60/ SLVSCL	P62/ SLVSALTB	P80/ INTP5	RD1	CC2	F
G	P40/ TOOL0	P61/ SLVSDA	P50/ INTP1	P51/ INTP2	CC1	VSS	G
	1	2	3	4	5	6	

2. PIN FUNCTION

This section describes each pin's function.

2.1 Power supply

Pin Name	QFN Pin No.	BGA Ball No.	I/O Type	Function
VDD	20	D4/D5/D6	Power	Power supply (from 3.0V to 5.5V: R9A02G011GNP) (from 2.7V to 5.5V: R9A02G011GBG)
REGCTX	19	E6	Power	Regulator capacitance for CC-PHY. Connecting regulator output stabilization capacitance for internal operation.
REGC	21	C6	Power	Regulator capacitance. Connecting regulator output stabilization capacitance for internal operation.
VSS	Die Pad	A1/B1/G6	-	Ground

2.2 System Interface Pins

Pin Name	QFN Pin No.	BGA Ball No.	I/O Type	Function
RESETB	25	A5	IN	Chip Reset Input (L active)

2.3 USB PD and Type-C™ Port Pins

Pin Name	QFN Pin No.	BGA Ball No.	I/O Type	Function
RD1	15	F5	I/O	Rd resistor 1, Analog pin from CC-PHY.
CC1	16	G5	I/O	Configuration Channel 1, Analog pin from CC-PHY
CC2	17	F6	I/O	Configuration Channel 2, Analog pin from CC-PHY
RD2	18	E5	I/O	Rd resistor 2, Analog pin from CC-PHY

2.4 I/O Port Pins

Pin Name	QFN Pin No.	BGA Ball No.	I/O Type	During reset	After reset	Function
P16	1	B2	I/O	Input	Input	Port 1, 2 bit I/O port.
P17	32	A2	I/O	Input	Input	Port 1, 2 bit I/O port.

Pin Name	QFN Pin No.	BGA Ball No.	I/O Type	During reset	After reset	Function
P20	2	C2	I/O	Input	Input	Port 2, 3 bit I/O port. It is also configurable as VBUSM or ANI8
P21	3	C1	I/O	Input	Input	Port 2, 3 bit I/O port. It is also configurable as ANI9
P22	4	D2	I/O	Input	Input	Port 2, 3 bit I/O port. It is also configurable as ANI10
P30	6	D1	I/O	Input	Input	Port 3, 3 bit I/O port. It is also configurable as MSTSCL.
P31	5	E1	I/O	Input	Input	Port 3, 3 bit I/O port. It is also configurable as MSTSDA
P32	11	E3	I/O	Input	Input	Port 3, 3 bit I/O port. It is also configurable as INTP3
P40	7	G1	I/O	Input	Input Pull-up	Port 4, 1 bit I/O port. It is also configurable as TOOL0
P50	13	G3	I/O	Input	Input	Port 5, 2 bit I/O port. It is also configurable as INTP1
P51	14	G4	I/O	Input	Input	Port 5, 2 bit I/O port. It is also configurable as INTP2
P60	9	F2	I/O	Input	Input	Port 6, 3 bit I/O port. It is also configurable as SLVSCL
P61	8	G2	I/O	Input	Input	Port 6, 3 bit I/O port. It is also configurable as SLVSDA
P62	10	F3	I/O	Input	Input	Port 6, 3 bit I/O port. It is also configurable as SLVSALTB
P70	26	B5	I/O	Input	Input	Port 7, 4 bit I/O port. It is also configurable as INTP4
P71	27	C4	I/O	Input	Input	Port 7, 4 bit I/O port.
P72	28	B4	I/O	Input	Input	Port 7, 4 bit I/O port.
P73	29	B3	I/O	Input	Input	Port 7, 4 bit I/O port.
P80	12	F4	I/O	Input	Input	Port 8, 3 bit I/O port. It is also configurable as INTP5
P81	30	A3	I/O	Input	Input	Port 8, 3 bit I/O port. It is also configurable as INTP6
P82	31	C3	I/O	Input	Input	Port 8, 3 bit I/O port. It is also configurable as INTP7
P121	22	C5	IN	Input	Input	Port 12, 2 bit Input port. It is also configurable as SLVADDR0
P122	23	B6	IN	Input	Input	Port 12, 2 bit Input port. It is also configurable as SLVADDR1
P137	24	A6	IN	Input	Input	Port 13, 1 bit Input port. It is also configurable as MSTSALTB or INTP0.

2.5 Alternate Functions on I/O Port Pins

I/O ports support the following alternate functions.

Function Name	I/O	Function
ANI8 to ANI10	Input	Analog Input
MSTSCL	I/O	SMBus master clock input/output (open-drain) Note 1
MSTSDA	I/O	SMBus master data input/output (open-drain) Note 1
MSTSALTB	Input	SMBus master alert input Note 1
SLVSCL	I/O	SMBus slave clock input/output (open-drain) Note 2
SLVSDA	I/O	SMBus slave data input/output (open-drain) Note 2
SLVSALTB	Output	SMBus slave alert output (open-drain)
SLVADDR0	input	SMBus slave address bit [1] Note 2
SLVADDR1	input	SMBus slave address bit [2] Note 2
VBUSM	Input	VBUS voltage monitor input. The pin assignment is fixed to this function.
INTP0 to INTP7	Input	Interrupt detection input. The valid edge (rising edge, falling edge, or rising and falling edges) can be specified.
TOOL0	I/O	Data input/output for flash programming tool. The pin assignment is fixed to this function.

Note 1. The pin assignment is fixed to this function when SMBus Master is enabled.
Note 2. The pin assignment is fixed to this function when SMBus Slave is enabled.

3. ELECTRICAL SPECIFICATIONS

This chapter describes the following electrical specifications.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
	$V_{IREGCTX}$	REGCTX	−0.3 to +2.8	V
Input voltage	V_I	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82, P121, P122, P137, RESETB	−0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_O	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82	−0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI8 to ANI10	−0.3 to V_{DD} +0.3 Note 2	V
	V_{AI2}	CC1, CC2, RD1, RD2	−0.5 to +6.5	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. V_{SS} : Reference voltage

Absolute Maximum Ratings (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to 73, P80 to P82	–40	mA
		Total of all pins		-170	mA
Output current, low	I_{OL1}	Per pin	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to 73, P80 to P82	40	mA
		Total of all pins		170	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +105: R9A02G011GNP –40 to +90: R9A02G011GBG	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			–65 to +150: R9A02G011GNP –55 to +90: R9A02G011GBG	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 On-chip oscillator characteristics of R9A02G011GNP

(T_A = –40 to +105°C, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1	f_{IH}				24		MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85 °C	3.0 V ≤ V_{DD} ≤ 5.5 V	-1		+1	%
		–40 to –20 °C	3.0 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
		+85 to +105 °C	3.0 V ≤ V_{DD} ≤ 5.5 V	-2		+2	%

Notes 1. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

3.2.2 On-chip oscillator characteristics of R9A02G011GBG

(T_A = –40 to +90°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 2	f_{IH}				24		MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85 °C	2.7 V ≤ V_{DD} ≤ 5.5 V	-1		+1	%
		–40 to –20 °C	2.7 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
		+85 to +90 °C	2.7 V ≤ V_{DD} ≤ 5.5 V	-2		+2	%

Notes 2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics of R9A02G011GNP

(T_A = –40 to +105°C, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/3)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P16, P17, P20 to P22, P30 to P32, P50, P51, P60 to P62, P70 to P73, P80 to P82	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 3.0 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
	V_{IH2}	P40, P121, P122, P137, RESETB		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P16, P17, P20 to P22, P30 to P32, P50, P51, P60 to P62, P70 to P73, P80 to P82	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 3.0 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL2}	P40, P121, P122, P137, RESETB		0		0.2 V_{DD}	V

Caution The maximum value of all pins is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/3)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82	3.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –1.5 mA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82	3.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V

Caution All pins do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (3/3)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82, P137, RESETB	V_I = V_{DD}			1	μA
	I_{LIH2}	P121, P122	V_I = V_{DD}, In input port			1	μA
Input leakage current, low	I_{LIL1}	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82, P137, RESETB	V_I = V_{SS}			–1	μA
	I_{LIL2}	P121, P122	V_I = V_{SS}, In input port			–1	μA
On-chip pull-up resistance	R_U	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82	V_I = V_{SS}, In input port	10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Pin characteristics of R9A02G011GBG

(T_A = –40 to +90°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/3)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P16, P17, P20 to P22, P30 to P32, P50, P51, P60 to P62, P70 to P73, P80 to P82	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 2.7 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
	V_{IH2}	P40, P121, P122, P137, RESETB		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P16, P17, P20 to P22, P30 to P32, P50, P51, P60 to P62, P70 to P73, P80 to P82	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 2.7 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL2}	P40, P121, P122, P137, RESETB		0		0.2 V_{DD}	V

Caution The maximum value of all pins is V_{DD}, even in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +90°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/3)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –1.5 mA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V

Caution All pins do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +90°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (3/3)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to 73, P80 to P82, P137, RESETB	V_{I1} = V_{DD}			1	μA
	I_{LIH2}	P121, P122	V_{I1} = V_{DD}, In input port			1	μA
Input leakage current, low	I_{LIL1}	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to 73, P80 to P82, P137, RESETB	V_{I1} = V_{SS}			–1	μA
	I_{LIL2}	P121, P122	V_{I1} = V_{SS}, In input port			–1	μA
On-chip pull-up resistance	R_U	P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to 73, P80 to P82	V_{I1} = V_{SS}, In input port	10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

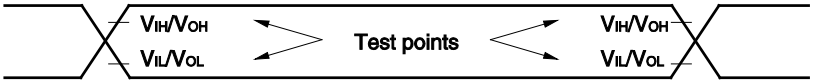
3.4 AC Characteristics

R9A02G011GNP: **(T_A = –40 to +105°C, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

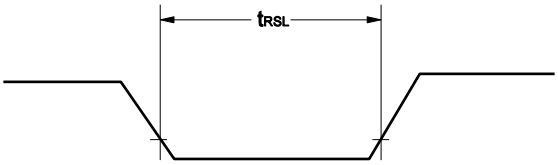
R9A02G011GBG: (T_A = –40 to +90°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RESETB low-level width	t_{RSL}		10			µs

AC Timing Test Points



RESETB Input Timing



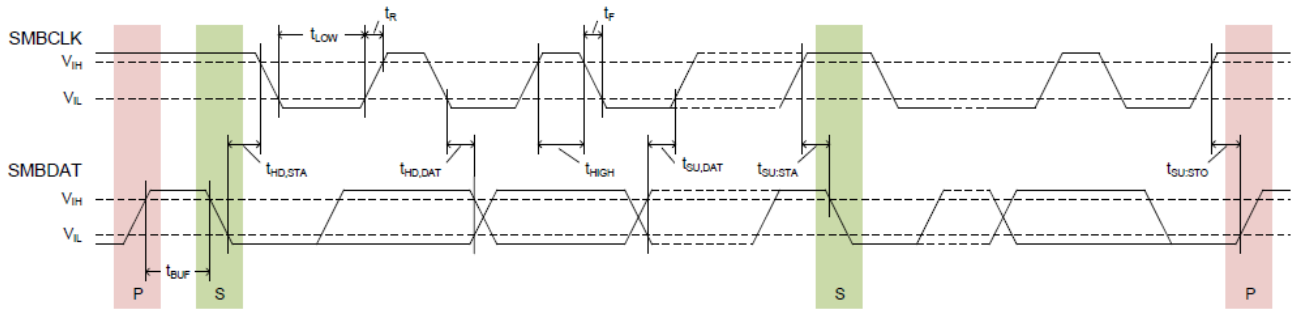
3.5 Peripheral Functions Characteristics

3.5.1 SMBus Interface

R9A02G011GNP: (T_A = –40 to +105°C, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)
R9A02G011GBG: (T_A = –40 to +90°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	100 kHz Class		400 kHz Class		1 MHz Class		Units
			MIN	MAX	MIN	MAX	MIN	MAX	
SMBus operating frequency	F_{SMB}		10	100	10	400	10	1000	kHz
Bus free time between stop and start condition	T_{BUF}		4.7		1.3		0.5		µs
Hold time after (Repeated) start condition. After this period, the first clock is generated.	$T_{HD:STA}$		4.0		0.6		0.26		µs
Repeated start condition setup time	$T_{SU:STA}$		4.7		0.6		0.26		µs
Stop condition setup time	$T_{SU:STO}$		4.0		0.6		0.26		µs
Data hold time	$T_{HD:DAT}$		0		0		0		ns
Data setup time	$T_{SU:DAT}$		250		100		50		ns
Clock low period	T_{LOW}		4.7		1.3		0.5		µs
Clock high period	T_{HIGH}		4.0	50	0.6	50	0.26	50	µs
Cumulative clock low extend time (slave device)	$T_{LOW:SEXT}$			25		25		25	ms
Cumulative clock low extend time (master device)	$T_{LOW:MEXT}$			10		10		10	ms
Clock/Data fall time	T_F			300		300		120	ns
Clock/Data rise time	T_R			1000		300		120	ns
Noise spike suppression time	T_{spike}				0	50	0	50	ns
Operational time after power-on reset	T_{POR}			500		500		500	ms

Figure 3-1. SMBus Signal Timing



3.6 Analog Characteristics

3.6.1 A/D converter characteristics of R9A02G011GNP

(T_A = –40 to +105°C, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Notes 1, 2]	AINL	10-bit resolution	3.0 V ≤ VDD ≤ 5.5 V		1.2	±7.0	LSB
Analog input voltage	VAIN	ANI8 to ANI10		0		VDD	V

3.6.2 A/D converter characteristics of R9A02G011GBG

(T_A = –40 to +90°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Notes 1, 2]	AINL	10-bit resolution	2.7 V ≤ VDD ≤ 5.5 V		1.2	±7.0	LSB
Analog input voltage	VAIN	ANI8 to ANI10		0		VDD	V

Notes 1. Excludes quantization error (±1/2 LSB).

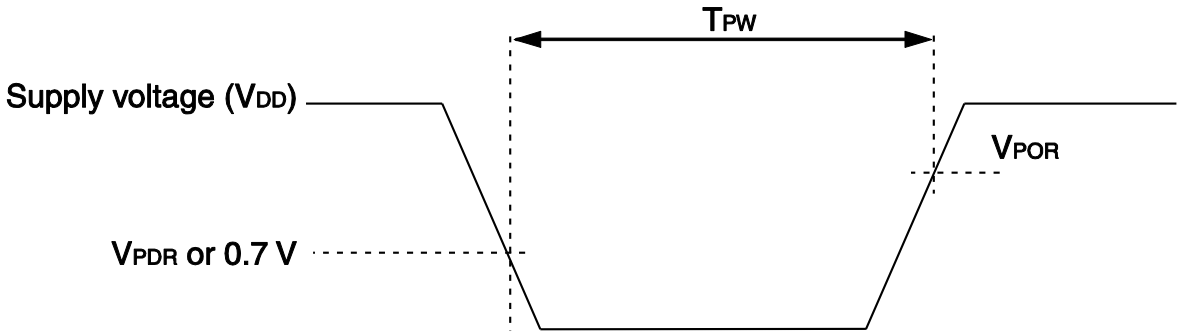
2. This value is indicated as a ratio (%FSR) to the full-scale value.

3.6.3 POR circuit characteristics

R9A02G011GNP: (T_A = –40 to +105°C, V_{SS} = 0 V)
R9A02G011GBG: (T_A = –40 to +90°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.43	1.51	1.59	V
	V_{PDR}	Power supply fall time	1.42	1.50	1.58	V
Minimum pulse width	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.4 Power supply voltage rising slope characteristics

R9A02G011GNP: (T_A = –40 to +105°C, V_{SS} = 0 V)
R9A02G011GBG: (T_A = –40 to +90°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range.

3.6.5 CC-PHY characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CC Current Source (Default)	I80u		64	80	96	µA
CC Current Source (1.5A)	I180u		166	180	194	µA
CC Current Source (3A)	I330u		304	330	356	µA
Transmitter Output Impedance	zDriver		33		75	Ω
Transmitter Rise Time	tRISE_TX		300			ns
Transmitter Fall Time	tFALL_TX		300			ns
Receiver Input Impedance	zBMCRX		1			MΩ

3.7 Flash Memory Programming Characteristics

3.7.1 Flash Memory Programming Characteristics of R9A02G011GNP

(T_A = –40 to +105° C, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	3.0 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
Number of code flash rewrites Notes 1,2,3	C_{erwr}	Retained for 20 years	T_A = 85° C Notes 4	1,000			Times

3.7.2 Flash Memory Programming Characteristics of R9A02G011GBG

(T_A = –40 to +90° C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
Number of code flash rewrites Notes 1,2,3	C_{erwr}	Retained for 20 years	T_A = 85° C Notes 4	1,000			Times

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self-programming library.

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4. This temperature is the average value at which data are retained.

3.8 Pin Capacitance

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System Interface Pin capacitance	C_{SYS}				5	pF
I/O Port Pin capacitance	C_{IO}				5	pF

3.9 Power Consumption

3.9.1 Power Consumption for applications other than E-Marker

(T_A = 25° C, V_{DD} = 3.3 V, V_{SS} = 0 V)

Parameter	Conditions		TYP.	Unit
Operating current as Source role	Sink attached.	No PD Communication.	3.2	mA
		PD Communication.	4.1	mA
Operating current as Sink role	Source attached.	No PD Communication.	2.7	mA
		PD Communication.	3.6	mA
Supply current in sleep mode	Unplugged. SMBus, WAKEUP/INTP and CC enabled for wakeup. Source role.		205	µA
Supply current in deep sleep mode	Unplugged. SMBus and WAKEUP/INTP enabled for wakeup.		2.8	µA

(T_A = 25° C, V_{DD} = 5.0 V, V_{SS} = 0 V)

Parameter	Conditions		TYP.	Unit
Operating current as Source role	Sink attached.	No PD Communication.	3.9	mA
		PD Communication.	4.8	mA
Operating current as Sink role	Source attached.	No PD Communication.	3.4	mA
		PD Communication.	4.3	mA
Supply current in sleep mode	Unplugged. SMBus, WAKEUP/INTP and CC enabled for wakeup. Source role.		230	µA
Supply current in deep sleep mode	Unplugged. SMBus and WAKEUP/INTP enabled for wakeup.		3.2	µA

3.9.2 Power Consumption for E-Marker in a USB Type-C™ Cable

(T_A = 25° C, V_{DD} = 3.3 V, V_{SS} = 0 V)

Parameter	Conditions		TYP.	Unit
Operating current as Cable Plug	Attached between a Port Pair	No PD Communication	2.2	mA
		PD Communication	3.5	mA

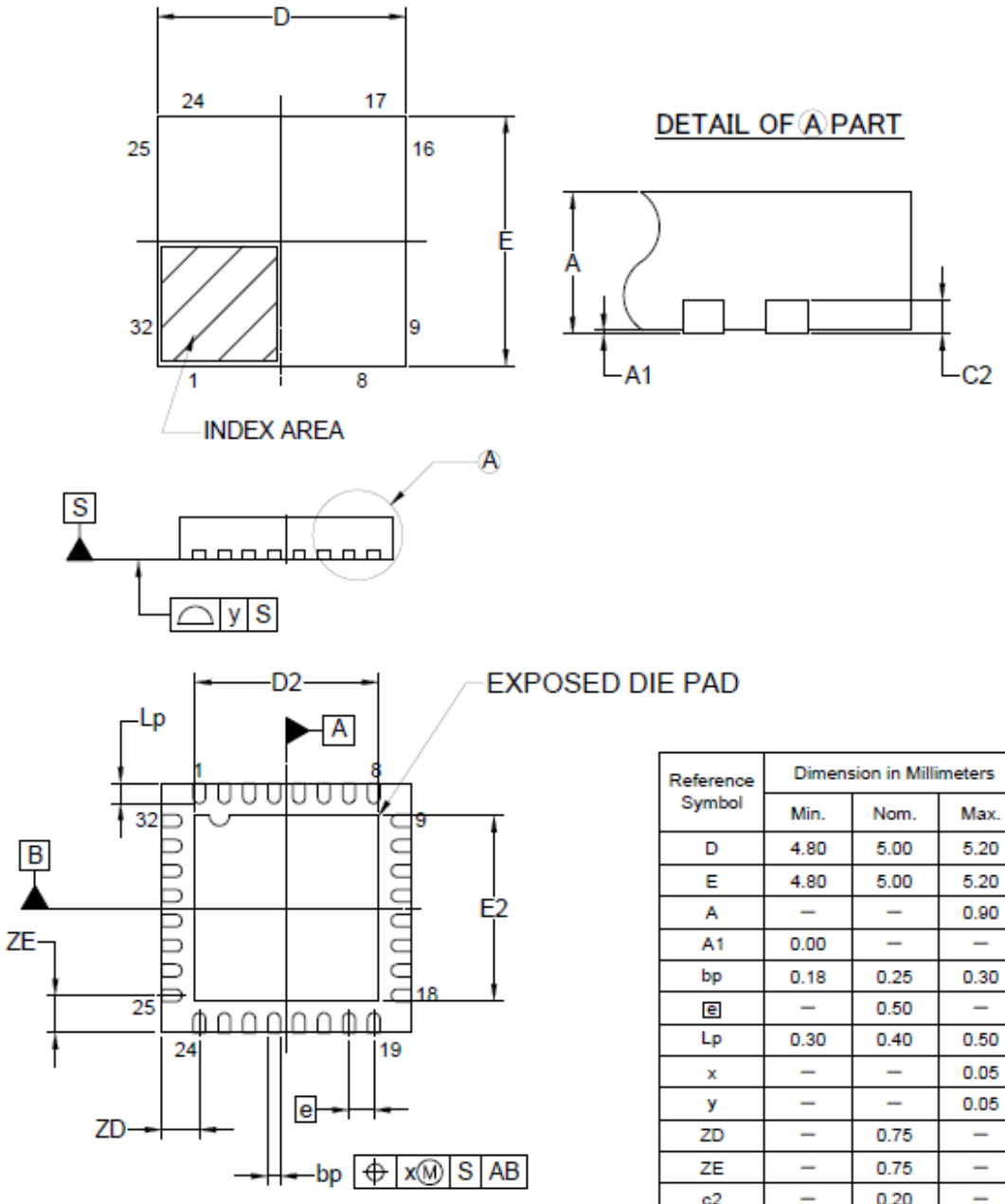
(T_A = 25° C, V_{DD} = 5.0 V, V_{SS} = 0 V)

Parameter	Conditions		TYP.	Unit
Operating current as Cable Plug	Attached between a Port Pair	No PD Communication	2.5	mA
		PD Communication	4.0	mA

4. PACKAGE DRAWINGS

32-PIN QFN (5 x 5 mm)

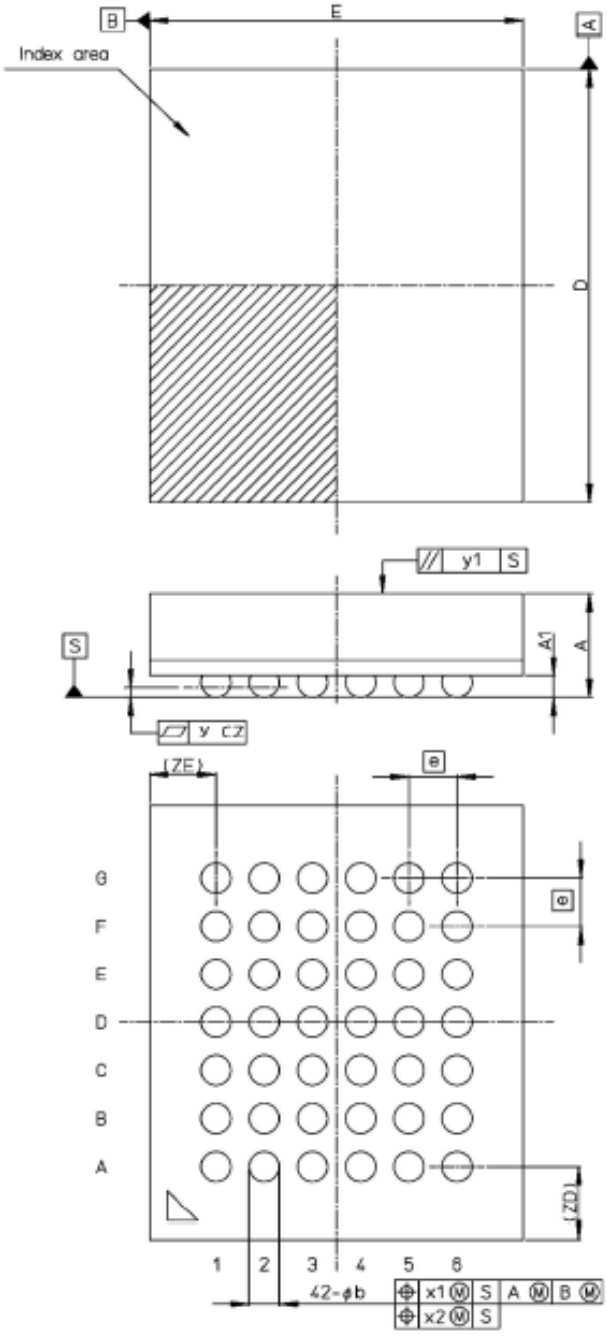
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HVQFN32-5x5-0.50	PVQN0032KG-A	T32K8-50-BAP	0.07



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	4.80	5.00	5.20
E	4.80	5.00	5.20
A	—	—	0.90
A1	0.00	—	—
bp	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
ZD	—	0.75	—
ZE	—	0.75	—
c2	—	0.20	—
D2	—	3.60	—
E2	—	3.60	—

42-pin BGA (3.6 x 3.1 mm)

JEITA Package Code	RENESAS Code	MASS[Typ.]
P-VBGA42-3.6x3.1-0.40	PVBG0042LA-A	0.02g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.5	3.6	3.7
E	3.0	3.1	3.2
A	—	—	1.00
A1	0.13	0.18	0.23
e	—	0.4	—
b	0.20	0.25	0.30
x1	—	—	0.15
x2	—	—	0.05
y	—	—	0.08
y1	—	—	0.20
ZD	—	0.60	—
ZE	—	0.55	—

Revision History	R9A02G011 Data Sheet

Rev.	Date	Description	
		Page	Summary
1.0	Nov. 25, 2016	-	First Edition issued
1.01	Feb. 17, 2017	3	Updated Figure 1-2
		5	Updated section 2.4
		6	Updated section 2.5
1.02	Oct. 24, 2017	1	Updated section 1, section 1.1
		-	Corrected writing errors
1.10	Jan. 29, 2018	1	Updated section 1, section 1.1, section 1.3
		3	Updated section 1.5
		15	Updated section 3.6.2
		18	Updated section 3.9
		19	Updated section 4
1.20	Mar. 27, 2018	1	Updated section 1.1
1.30	Jan. 29, 2019	4-6	Updated section 2.4, section 2.6
2.00	Dec. 23, 2021	-	Completely revised with the addition of R9A02G011GBG.
		1	Updated section 1, section 1.1
2.10	Apr. 22, 2022	1	Updated section 1, section 1.1

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The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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