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PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

Table of Contents

1.0	Applicable Products	2
2.0	General Description	2
3.0	Functional Diagram	2
4.0	Pin Descriptions	3
5.0	Reference Input Stage	4
6.0	Reference Path 'R' Divider	4
7.0	RF Path 'N' Divider	4
8.0	Charge Pump & Phase Frequency Detector	4
9.0	Phase Frequency Detector Test Functions	4
10.0	Phase Frequency Detector Jitter & Lock Detect Background	5
11.0	Phase Frequency Detector Lock Detect	6
12.0	Cycle Slip Prevention (CSP)	8
13.0	Charge Pump Gain	8
14.0	Charge Pump Gain Trim	8
15.0	Charge Pump Phase Offset	9
16.0	Charge Pump Operation Near the Rail	9
17.0	Fractional Mode	10
17.1	Fractional Frequency Tuning	10
17.2	FSK Modulation	11
18.0	Integer Mode	12
18.1	Integer Frequency Tuning	12
18.2	Soft Reset and Power on Reset	12
18.3	Power Down Mode	12
18.4	Chip Identification	12
19.0	SERIAL PORT	13
19.1	Serial Port WRITE Operation	13
19.2	Serial Port READ Operation	14
20.2	Reg 00h RST Strobe Register	15
	For write operations to register 00h, it is a Write Only strobe register as defined below.	15
20.3	Reg 01h RST Register	15
20.4	Reg 02h REFDIV Register	15
20.0	Register Map	15
20.1	Reg 00h ID (Read Only) Register	15
	Note: For Read Operations from register 00h, it is Read Only containing the chip ID. Current Hittite PLL with Inte- grated VCO chip IDs are shown below.	15
20.5	Reg 03h Frequency Register - Integer Part	16
20.6	Reg 04h Frequency - Fractional Part Register	16
20.7	Reg 05h SD Seed Register	16
20.8	Reg 06h SD CFG Register	17
20.9	Reg 07h LKD/CSP Register	18
20.10	Reg 08h Analog EN Register	18
20.11	Reg 09h CP Register	19
20.12	Reg 0Ah CP Op Amp Register	20
20.13	Reg 0Bh PFD Register	20
20.14	Reg 0Ch VCO SPI Register	20
20.15	Reg 0Dh GPO_SPI_RDIV Register	21
20.16	Reg 0Fh LD State Register (Read Only)	21

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PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

1.0 Applicable Products

HMC764LP6CE, HMC765LP6CE, HMC783LP6CE & HMC807LP6CE

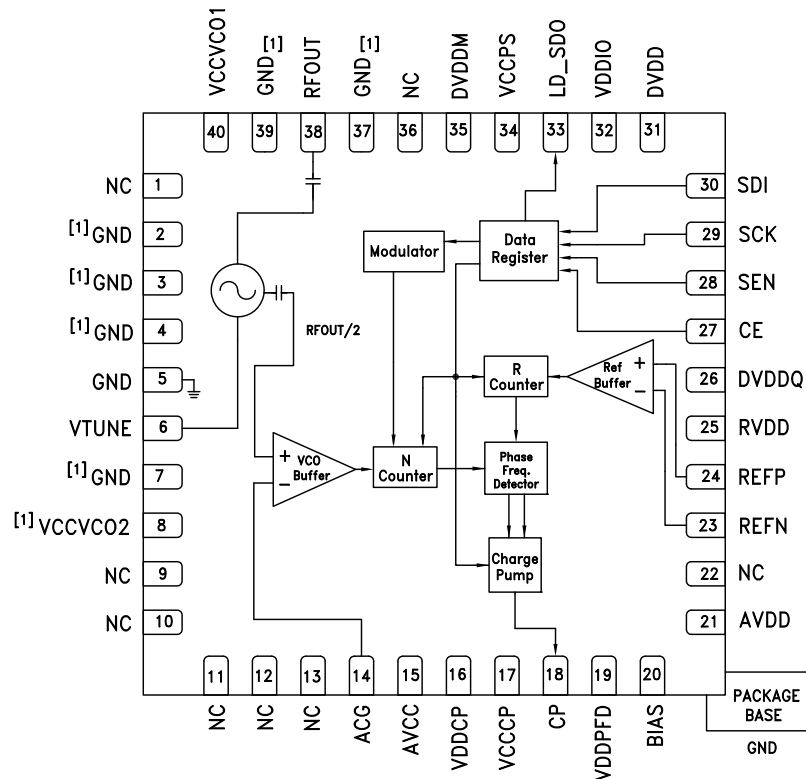
2.0 General Description

This operating guide applies to the specified family of PLL with integrated VCO's. The purpose of this guide is to describe all common features of the IC with the exception of the VCO. The unique characteristics for the individual VCOs are described in detail on the respective Hittite product data sheet.

The PLL with Integrated VCO includes a very low noise digital phase frequency detector (PFD), and a precision controlled charge pump. The fractional PLL with Integrated VCO features an advanced delta-sigma modulator design that allows both ultra-fine step sizes and very low spurious products. Spurious outputs are low enough to eliminate the need for costly Direct Digital Synthesis (DDS) references in many applications.

The PFD features cycle slip protection (CSP) technology that allows faster frequency hopping times. Ultra low close-in phase noise and low spurious also permit architectures with wider loop bandwidths for faster frequency hopping and low micro-phonics. FSK mode allows the PLL with Integrated VCO to be used as a simple low cost direct FM transmitter source.

3.0 Functional Diagram





PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

4.0 Pin Descriptions

Pin Number	Function	Description
1, 9 - 13, 22, 36	N/C	No Connection. These pins may be connected to RF/DC ground. Performance will not be affected.
2 - 4, 7, 37, 39	GND [1]	These pins must be connected to RF/DC Ground
5	GND	These pins and package bottom must be connected to RF/DC Ground
8	VCCVCO2 [2]	+5V Power Supply for VCO
40	VCCVCO1	
6	VTUNE	Control Voltage Input. Modulation port bandwidth dependent on drive source impedance.
14	ACG	AC Ground. This pin must be connected to an external capacitor to ground.
15	AVCC	Analog Power supply pin for the RF Section. A decoupling capacitor to the ground plane should be placed as close as possible to this pin. Nominally 3.3V
16	VDDCP	+5V Power Supply for charge pump digital section
17	VCCCP	+5V Power Supply for the charge pump analog section
18	CP	Charge pump output
19	VDDPFD	Analog Power supply for the phase frequency detector, Nominally 3.3V
20	BIAS [3]	External bypass decoupling for precision bias circuits, 1.920V ±20 mV is generated internally
21	AVDD	Analog Power supply for analog ref paths, Nominally 3.3V
23	REFN	Reference input (Negative or AC coupled to GND)
24	REFP	Reference input (Positive)
25	RVDD	Ref path supply
26	DVDDQ	Digital supply for Substrate, Nominally 3.3V
27	CE	Chip Enable
28	SEN	Serial port latch enable input
29	SCK	Serial port clock input
30	SDI	Serial port data input
31	DVDD	Power supply pin for internal digital circuitry. Nominally 3.3V
32	VDDIO	Power Supply for digital I/O driver
33	LD_SDO	Lock Detect, Main Serial Data Output or VCO Serial Port Data Out
34	VCCPS	Analog Power Supply for Prescaler, Nominally 3.3V
35	DVDDM	Digital Power Supply for M-Counter, Nominally 3.3V
38	RFOUT	RF output (AC coupled).

[1] This pin is not connected internally, however, this pin must be connected to GND to maintain product family pin for pin compatibility.

[2] This pin is not connected internally, however, this pin must be connected to Vcc to maintain product family pin for pin compatibility.

[3] BIAS ref voltage (pin 20) cannot drive an external load, and must be measured with a 10 GOhm meter such as Agilent 34410A; a typical 10 Mohm DVM will read erroneously.



PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

pdf_dn_en in [Reg 0Bh](#) allows masking of the PFD down output, which effectively prevents the charge pump from pumping down.

De-asserting both *pdf_up_en* and *pdf_dn_en* effectively tri-states the charge pump while leaving all other functions operating internally.

10.0 Phase Frequency Detector Jitter & Lock Detect Background

In normal phase locked operation the divided VCO signal arrives at the phase frequency detector in phase with the divided crystal signal, known as the PFD reference signal. Despite the fact that the device is in lock, the phase of the VCO signal and the PFD reference signal vary in time due to the phase noise of the reference and VCO oscillators, the loop bandwidth used and the presence of fractional modulation or not. The total integrated noise from the VCO normally dominates the variations in the two arrival times at the phase frequency detector in integer mode.

If we wish to detect if the VCO is in lock or not we need to distinguish between normal phase jitter when in lock and phase jitter when not in lock.

First, we need to understand what is the jitter of the PLL with Integrated VCO, measured at the phase frequency detector in integer or fractional modes.

The standard deviation of the arrival time of the VCO signal, or the jitter, in integer mode may be estimated with a simple approximation if we assume that the locked VCO has a constant phase noise, $\Phi^2(f_0)$, at offsets less than the loop 3 dB bandwidth and a 20 dB per decade rolloff at greater offsets. The simple locked VCO phase noise approximation is shown in [Figure 2](#).

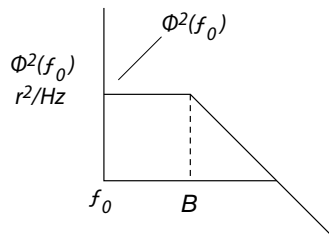


Figure 2. PLL with Integrated VCO Phase Noise & Jitter

With this simplification the total integrated VCO phase noise, ϕ^2 , in rads^2 at the phase frequency detector is given by

$$\phi^2 = \phi^2(f_0) B \pi / N^2 \quad (\text{EQ 1})$$

where

B is the 3 dB corner frequency of the closed loop PLL

N is the division ratio of the prescaler

Since the simple integral of (EQ 1) is just a product of constants, we can easily do the integral in the log domain. For example if the VCO phase noise inside the loop is -100 dBc/Hz at 10 kHz offset and the loop bandwidth is 100 kHz, and the division ratio is 100, then the integrated phase noise at the phase frequency detector, in dB, is given by:

$$\phi_{dB}^2 = 10 \log (\phi^2(f_0) B \pi / N^2) = -100 + 50 + 5 - 40 = 85 \text{ dB rads}^2$$

or equivalently, $\phi = 10^{-85/20} = 94.4 \text{ urads} = 5.4 \text{ milli-degrees rms}$.

While the phase noise reduces by a factor of $20 \log N$ after division to the reference, due to the increased period of the PFD reference signal, the jitter is constant.

The rms jitter from the phase noise is then given by $T_{jpn} = T_{PFD} \phi / 2\pi$



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In this example if the PFD reference was 50 MHz, $T_{PFD} = 20\text{nsec}$, and hence $T_{jpn} = 0.30\text{ psec}$.

A normal 3 sigma variation in the arrival time therefore would be $\pm 3T_{jpn} = \pm 0.9\text{ psec}$.

If the PLL with Integrated VCO was in fractional mode, the fractional modulation of the VCO divider will dominate the jitter. The exact standard deviation of the divided VCO signal will vary based upon the modulator type chosen, however a typical modulator will vary by about ± 3 division ratios, ± 4 division ratios, worst case.

If, for example a nominal VCO at 5 GHz is divided by 100 to equal the PFD reference at 50 MHz, then the worst case division ratios will vary by 100 ± 4 . Hence the peak variation in the arrival times caused by $\Delta\Sigma$ modulation of the fractional PLL with Integrated VCO at the reference will be

$$T_{j\Delta\Sigma pk} = \pm T_{vco} \cdot (N_{max} - N_{min})/2 \quad (\text{EQ 2})$$

If we note that the distribution of the delta sigma modulation is approximately Gaussian, we could approximate $T_{j\Delta\Sigma pk}$ as a 3 sigma jitter, and hence we could estimate the rms jitter of the $\Delta\Sigma$ modulator as about $1/3$ of $T_{j\Delta\Sigma pk}$ or about 266 psec in this example.

Hence the total rms jitter T_j , expected from the delta sigma modulation plus the phase noise of the VCO would be given by the rms sum, where

$$T_j = \sqrt{T_{jpn}^2 + \left(\frac{T_{j\Delta\Sigma pk}}{3}\right)^2} \quad (\text{EQ 3})$$

In this example the jitter contribution of the phase noise calculated previously would add only 0.18psec more jitter at the reference, hence we see that the jitter at the phase frequency detector is totally dominated by the fractional modulation.

Hence, we have to expect about $\pm 800\text{ psec}$ of normal variation in the phase frequency detector arrival times when in fractional mode. In addition, lower VCO frequencies with high PFD reference frequencies will have much larger variations. For example a 1 GHz VCO operating at near the minimum nominal divider ratio of 36, would according to (EQ 2) exhibit about $\pm 4\text{nsec}$ of peak variation at the phase frequency detector, under normal operation.

In summary, the lock detect circuit must not interpret fractional modulation or normal phase noise related jitter as being out of lock, while at the same time declaring loss of lock when truly out of lock.

11.0 Phase Frequency Detector Lock Detect

lkd_enable in [Reg 07h](#) enables the lock detect functions.

The Lock Detect circuit places a one shot window around the reference. The one shot window may be generated by either an analog one shot circuit or a digital one shot based upon an internal ring oscillator. Clearing *ringosc_oneshot_sel* ([Reg 07h](#)) will result in a fixed analog based nominal $\pm 10\text{ nsec}$ window, as shown in [Figure 3](#). Setting *ringosc_oneshot_sel* will result in a variable length widow based upon a high frequency internal ring oscillator. The ring oscillator frequency is controlled by *ringosc_cfg*. The resulting lock detect window period is then generated by the number of ring oscillator periods defined in *oneshot_duration*, both in [Reg 07h](#).

wincnt_max in [Reg 07h](#) defines the number of consecutive counts of the divided VCO that must land inside the lock detect window to declare lock. If for example we set *wincnt_max* = 1000, then the VCO arrival would have to occur inside the $\pm 10\text{ nsec}$ widow 1000 times in a row to be declared locked, which results in a Lock Detect Flag high. A single occurrence outside of the window will result in an out of lock, i.e. Lock Detect Flag low. Once low, the Lock Detect Flag will stay low until the *wincnt_max* = 1000 condition is met again.



PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

The Lock Detect Flag is output to LD_SDO pin according to *pdf_LD_opEn* (Reg 0Bh) or to the internal SPI read only register if *locked = 1* (Reg 0Fh). Setting *pdf_LD_opEn* will display the Lock Detect Flag on LD_SDO except when a serial port read is requested, in which case the pin reverts temporarily to the Serial Data Out pin, and returns to the Lock Detect Flag after the read is completed. Timing of the Lock Detect and Serial Data Out functions are shown in Figure 3.

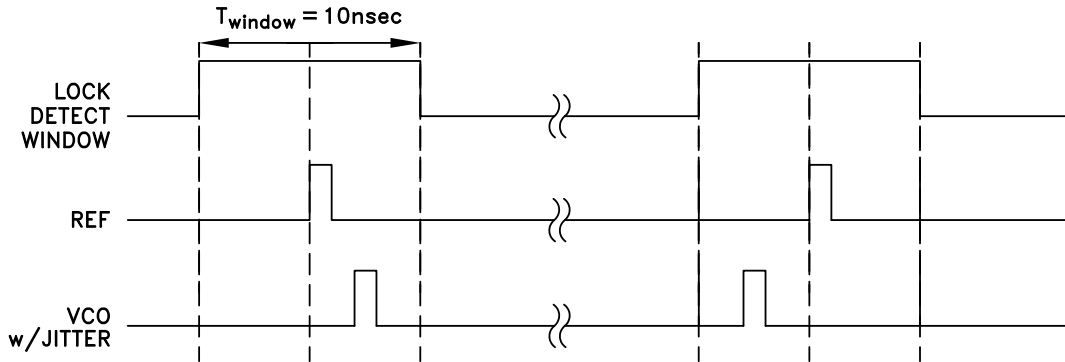


Figure 3. Normal Lock Detect Window

When operating in fractional mode the linearity of the charge pump and phase frequency detector are much more critical than in integer mode. The phase frequency detector linearity is worse when operated with zero phase offset. Hence in fractional mode it is necessary to offset the phase of the PFD reference and the VCO at the phase frequency detector. In such a case, for example with an offset delay, as shown in Figure 4, the VCO arrival will always occur after the reference. The lock detect circuit can accommodate a fixed offset delay by setting *lkd_win_asym_enable* and *win_asym_up_sel* in Reg 07h. Similarly the offset can be in advance of the reference by clearing *lkd_win_asym_up_sel* while leaving *lkd_win_asym_enable* set both in Reg 07h. There are certain conditions, such as operating near the supply limits of the charge pump which make it advantageous to use advanced or delayed phase offset, hence both are available.

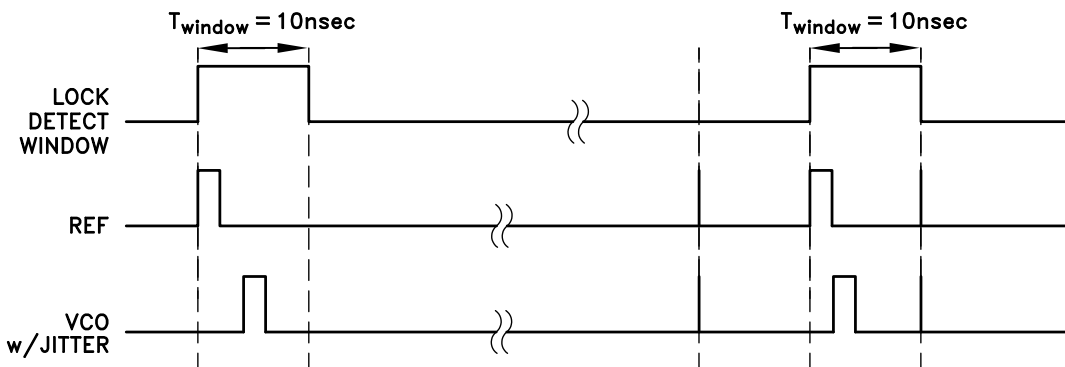


Figure 4. Delayed Lock Detect Window



12.0 Cycle Slip Prevention (CSP)

When the VCO is not yet locked to the reference, the instantaneous frequencies of the two paths are different, and the phase difference of the two paths at the PFD varies rapidly over a range much greater than $\pm 2\pi$ radians. Since the gain of the PFD varies linearly with phase up to $\pm 2\pi$, the gain of a conventional PFD will cycle from high gain, when the phase difference approaches a multiple of 2π , to low gain, when the phase difference is slightly larger than a multiple of 0 radians. The charge on the loop filter small cap may actually discharge slightly during the low gain portion of the cycle. This can make the VCO frequency actually reverse temporarily during locking. This phenomena is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically as shown in the red curve in [Figure 5](#), and increases the time to lock to a value far greater than that predicted by normal small signal Laplace analysis.

The internal PFD features an ability to virtually eliminate cycle slipping during acquisition. When enabled, the Cycle Slip Prevention (CSP) feature essentially holds the PFD gain at maximum until such time as the frequency difference is near zero. Cycle Slip Prevention, allows faster lock times as shown in [Figure 5](#). The use of the cycle slip feature is enabled with `csp_enable` (see [Reg 07h](#)).

The Cycle Slip Prevention feature may be optimized for a given set of PLL dynamics by adjusting the PFD sensitivity to cycle slipping. This is achieved by adjusting `csp_corr_magn` in [Reg 06h](#).

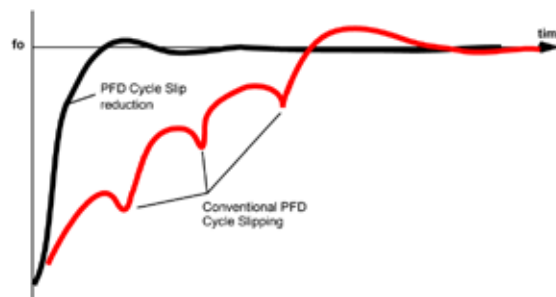


Figure 5. Cycle Slip Prevention (CSP)

13.0 Charge Pump Gain

A simplified diagram of the charge pump is shown in [Figure 6](#). Charge pump up and down gains are set by `cp_UPcurrent_sel` and `cpDNcurrent_sel` respectively ([Reg 09h](#)). Each of the UP and DN charge pumps consist of two 500 μA current sources and one 1000 μA current source. The current gain of the pump in radians/Amp is equal to the gain setting of this register divided by 2π . For example if both `cp_UPcurrent_sel` and `cpDNcurrent_sel` are set to '010' the output current of each pump will be 1mA and the phase frequency detector gain $K_p = 1\text{mA}/2\pi$ radians, or 159 $\mu\text{A}/\text{rad}$.

14.0 Charge Pump Gain Trim

Each of the UP and DN pumps may be trimmed to more precise values to improve current source matching or to allow finer control of pump gain. The pump trim controls are 4-bits, binary weighted for UP and DN, in `cp_UPtrim_sel` and `cp_DNtrim_sel` respectively ([Reg 09h](#)). LSB weight is 7 μA , maximum trim is 105 μA .



PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

15.0 Charge Pump Phase Offset

Ideally the phase frequency detector operates with zero offset, that is, the divided reference signal and the divided VCO signal arrive at the phase frequency detector inputs at exactly the same time. In some modes of operation, such as fractional mode, charge pump linearity and ultimately, phase noise, is better if the VCO and reference inputs are operated with a phase offset. Normally integer mode of operation is best with no phase offset. A phase offset is implemented by adding a constant DC leakage to one of the charge pumps. DC leakage may be added to the UP or DN pumps using *chp_UPoffset_sel* or *chp_DNoffset_sel*. These are 3-bit registers with 55 μ A LSB. Maximum offset is 385 μ A.

16.0 Charge Pump Operation Near the Rail

It should be noted that the charge pump is a non-ideal device. Phase locked operation with the tuning voltage very near the positive charge pump supply voltage or very near ground will degrade the phase noise performance of the PLL with Integrated VCO. Exactly how close to the supply limits that one should operate is a question of margin needed for the application in question and user judgement. It should be noted that if operation is necessary very near the supply limits, for example less than 500 mV from the supply limit, then it is recommended to operate with a DC leakage that leaks in the direction of the supply. For example, if the charge pump supply is 5.5V and locked operation is required with a VCO tune voltage of 5.2V, then operating with UP leakage on the charge pump will improve operation in this region. Similarly if phase locked operation is needed, with a VCO tune voltage of say 300 mV, then operating with DN leakage is recommended.

As an example, if the main pump gain was set at 1 mA, an offset of 385 μ A would represent a phase offset of about $(385/1000) \times 360 = 138$ degrees. Normally it is sufficient to offset the pump by just slightly larger than the delta sigma excursions for best phase noise. Best spurious operation usually occurs with larger DN offsets.

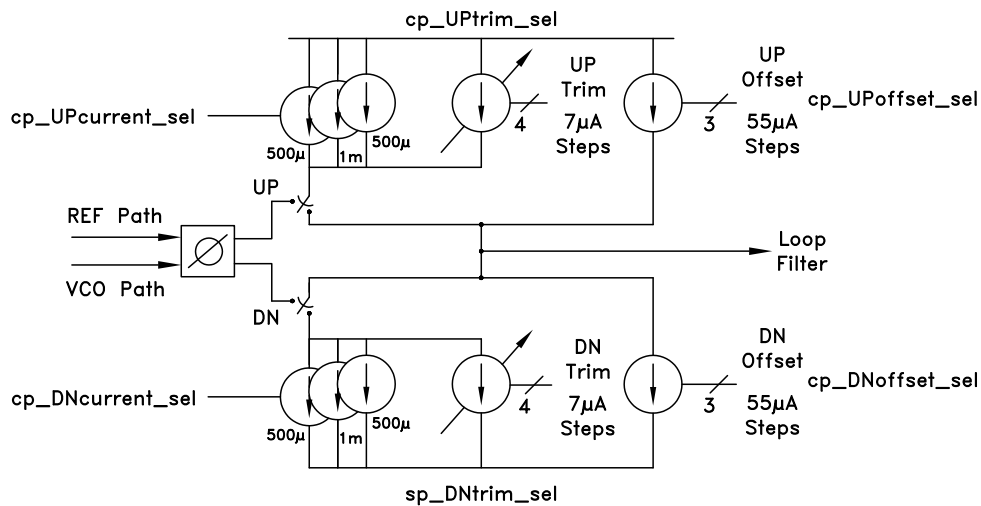


Figure 6. Charge Pump Gain & Offset Control



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17.0 Fractional Mode

17.1 Fractional Frequency Tuning

The PLL with Integrated VCO in fractional mode can achieve frequencies at fractional multiples of the reference. The output frequency of the PLL with Integrated VCO is given by

$$f_{vco} = \frac{f_{xtal}}{R} N_{int} + \frac{f_{xtal} \cdot N_{frac}}{R \cdot 2^{24}} = f_{int} + f_{frac} \quad (\text{EQ 4})$$

Where	
N_{int}	is the integer division ratio, an integer number between 36 and 65,567 (see intg Table 10)
N_{frac}	is the fractional part, a number from 1 to 2^{24} see frac Table 11
R	is the reference path division ratio, see rdv Table 9
f_{xtal}	is the frequency of the reference oscillator input
f_{PFD}	is the PFD operating frequency f_{xtal} / R
As an Example	
f_{xtal}	= 50 MHz
R	= 1
f_{PFD}	= 50 MHz
N_{int}	= 45
N_{frac}	= 1

$$f_{vco} = \frac{50e6}{1} 45 + \frac{50e6 \cdot 1}{1 \cdot 2^{24}} = 2.3GHz + 2.98Hz \quad (\text{EQ 5})$$

In this example the output frequency of 2,300,000,002.98 Hz is achieved by programming the 10-bit binary value of 46d = 2Eh = 0000 0000 0010 1110 into *intg* [Reg 03h](#).

Similarly the 24-bit binary value of the fractional word is written into *frac* in [Reg 04h](#),

16,777,215d = FFF FFFh = 1111 1111 1111 1111 1111

1d = 000 001h = 0000 0000 0000 0000 0000 0001

Example 2: Set the output to 4.600 025 GHz using a 100 MHz reference, R=2.

Find the nearest integer value, N_{int} , $N_{int} = 92$, $f_{int} = 4.600 000$ GHz

This leaves the fractional part to be $f_{frac} = 25$ kHz

$$N_{frac} = \frac{2^{24} \cdot R \cdot f_{frac}}{f_{xtal}} = \frac{2^{24} \cdot 2 \cdot 25e3}{100e6} = 8389 \quad (\text{EQ 6})$$

Since N_{frac} must be an integer number, the actual fractional frequency will be 4,600,025,001.17 Hz, an error of 1.17 Hz or 0.00025 ppm.

Here we program the 16-bit $N_{int} = 92d = 5Ch = 0000 0000 0101 1100$ and

The 24-bit $N_{frac} = 8389d = 20C5h = 0000 0010 0000 1100 0101$

In addition to the above frequency programming words, the fractional mode must be enabled by setting *frac_rstb* and *buff_rstb* [Reg 06h](#). Other DSM configuration registers should be set to the recommended register values.



17.2 FSK Modulation

The PLL with Integrated VCO with integrated VCO is capable of a simple binary Frequency Shift Keying (FSK) modulation. The internal modulation is unshaped FSK. The loop bandwidth of the PLL with Integrated VCO must be fixed by the user to achieve symbol shaping as required.

When the FSK mode of operation is enabled, via *fsk_enable* (Reg 06h), and SEN is held high, the PLL with Integrated VCO will output binary FSK frequency hops in response to data input on the SDI pin. When SEN is reset, the FSK modulation will stop and return to f_0 . SCK must not be toggled when transmitting data in FSK mode.

FSK modulation is normally defined by a deviation, Δf , and a modulation rate, f_m . The deviation is defined as the difference between the frequency transmitted when input data is 0, f_0 , and the frequency transmitted when the input data is 1, f_1 .

f_0 is the frequency programmed in the frequency registers as was defined in (EQ 4), that is:

$$f_0 = \frac{f_{ref} N_{int}}{R} + \frac{f_{ref} N_{frac}}{R \cdot 2^{24}} = f_{int} + f_{frac} \quad (\text{EQ 7})$$

f_1 is the fractional frequency achieved by adding the value in the seed register to the value in the frac register, that is:

$$f_1 = \frac{f_{ref} N_{int}}{R} + \frac{f_{ref} (N_{frac} + N_{seed})}{R \cdot 2^{24}} = f_{int} + f_{frac} + f_{seed} \quad (\text{EQ 8})$$

Where

N_{int} is the integer division ratio, an integer number between 36 and 65,567 (see integer register)

N_{frac} is the fractional part, a number from 1 to 2^{24}

N_{seed} is the seed part, a number from 1 to 2^{24}

R is the reference path division ratio

f_{ref} is the frequency of the external reference input

In this case the deviation Δf is given simply by

$$\Delta f = f_1 - f_0 = f_{seed} \quad (\text{EQ 9})$$

FSK data bits on SDI will be latched into the PLL with Integrated VCO on the falling edge of the divided reference rate, f_{PFD} . If for example $R=1$, and $f_{ref} = 50$ MHz, the input FSK data would be oversampled every 20nsec on the falling edge of the input reference.

The f_m rate of the FSK data is simply the inverse of twice the period of the data bits. For example, if the data bit period is 1msec the f_m rate is 500 Hz.

If an unshaped binary FSK is desired, the closed loop bandwidth of the PLL with Integrated VCO should be larger than the f_m rate by a sufficient margin. For practical FSK transmissions the f_m rate is limited by the radio link budget, channel spectral emission restrictions and practical closed loop bandwidths of the fractional PLL with Integrated VCO.



PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

18.0 Integer Mode

The PLL with Integrated VCO is capable of operating in integer mode. In integer mode the PLL with Integrated VCO step size is fixed to that of the PFD frequency, f_{PFD} . Integer mode typically has the lower phase noise for a given PFD operating frequency, than fractional mode. The advantage is usually of the order of 1 to 3 dB. Integer mode, however, often requires a lower PFD frequency to meet step size requirements. The fractional mode advantage is that higher PFD frequencies can be used, hence lower phase noise can often be realized in fractional mode.

18.1 Integer Frequency Tuning

In integer mode the digital $\Delta\Sigma$ modulator is shut off and the division ratio of the prescaler is set at a fixed value. To run in integer mode clear *frac_rstb* and *buffrstb* [Reg 06h](#). Then program the integer portion of the frequency as explained by (EQ 4), ignoring the fractional part.

18.2 Soft Reset and Power on Reset

The PLL with Integrated VCO portion of the IC features a hardware Power on Reset (POR). All chip registers will be reset to default states approximately 250us after power up. The SPI registers may also be soft reset by an SPI write to strobe register *rst_swrst* ([Reg 00h](#))

18.3 Power Down Mode

PLL with Integrated VCO Power Down is done by deasserting Chip Enable, CE, pin 27 (Low = Disabled). This will result in all analog functions and internal clocks disabled. Current consumption will typically drop below 10 μ A in Power Down state. During Power Down, the serial register writes will still operate, however, serial data output is disabled so Read operations will not work.

It is possible to control Power Down Mode from the serial port register *rst_chipen_from_spi* by clearing *rst_chipen_pin_select* ([Reg 01h](#)).

It is also possible to leave various blocks on when in Power Down (see [Reg 01h](#)), including:

- a. Digital Clocks
- b. Internal bias reference sources
- c. PFD block
- d. Charge Pump Block
- e. Reference Path buffer
- f. VCO Path buffer
- g. Digital I/O Test pads

18.4 Chip Identification

The version of the PLL with Integrated VCO is described in [Reg 00h](#). Version information may be read from the PLL with Integrated VCO by reading the content of *chip_ID* in [Reg 00h](#).



**PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS
PRODUCT & OPERATING GUIDE**

19.0 SERIAL PORT

Typical serial port operation can be run with SCK at speeds up to 50 MHz.

19.1 Serial Port WRITE Operation

AVDD = DVDD = 3V ±10%, AGND = DGND = 0V

Parameter	Conditions	Min	Typ	Max	Units
t ₁	SEN to SCK Setup Time	8			nsec
t ₂	SDI to SCK Setup Time	10			nsec
t ₃	SDI to SCK Setup Time	10			nsec
t ₄	SCK High Duration	8			nsec
t ₅	SCK Low Duration	8			nsec
t ₆	SEN High Duration	640			nsec
t ₇	SEN Low Duration	20			nsec

A typical WRITE cycle is shown in [Figure 7](#).

- The Master (host) both asserts SEN (Serial Port Enable) and clears SDI to indicate a WRITE cycle, followed by a rising edge of SCK.
- The slave (PLL with Integrated VCO) reads SDI on the 1st rising edge of SCK after SEN. SDI low initiates the Write cycle (/WR).
- Host places the six address bits on the next six falling edges of SCK, MSB first.
- Slave registers the address bits in the next six rising edges of SCK (2-7).
- Host places the 24 data bits on the next 24 falling edges of SCK, MSB first .
- Slave registers the data bits on the next 24 rising edges of SCK (8-31).
- SEN is de-asserted on the 32nd falling edge of SCK.
- The 32nd falling edge of SCK completes the cycle.

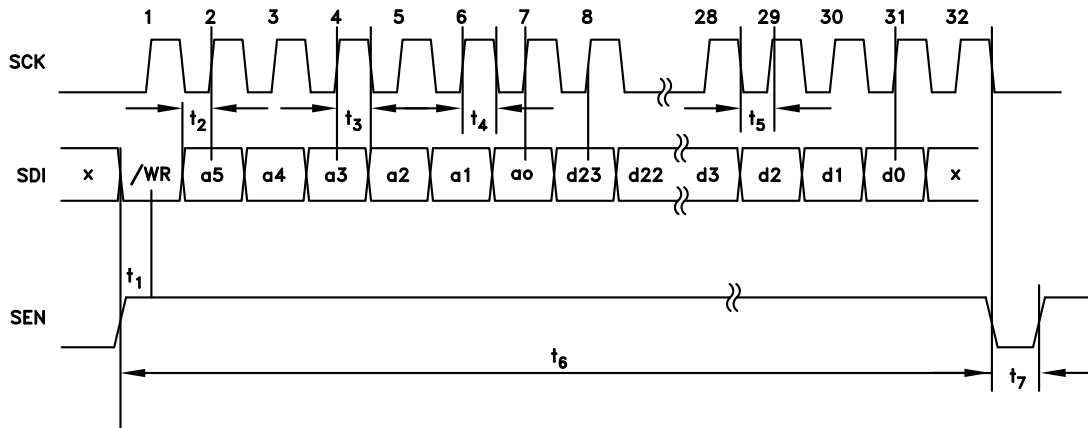


Figure 7. Serial Port Timing Diagram - Write Serial Port WRITE Operation

19.2 Serial Port READ Operation

A typical READ cycle is shown in [Figure 8](#).

- The Master (host) asserts both SEN (Serial Port Enable) and SDI to indicate a READ cycle, followed by a rising edge SCK. Note: The Lock Detect function is multiplexed onto the LD_SDO pin. It is suggested that lock detect (LD) only be considered valid when SEN is low. In fact LD will not toggle until the first active data bit toggles on LD_SDO, and will be restored immediately after the trailing edge of the LSB of serial data out as shown in [Figure 7](#).
- The slave (PLL with Integrated VCO) reads SDI on the 1st rising edge of SCK after SEN. SDI high initiates the READ cycle (RD).
- Host places the six address bits on the next six falling edges of SCK, MSB first.
- Slave registers the address bits on the next six rising edges of SCK (2-7).
- Slave switches from Lock Detect and places the requested 24 data bits on SD_LDO on the next 24 rising edges of SCK (8-31), MSB first.
- Host registers the data bits on the next 24 falling edges of SCK (8-31).
- Slave restores Lock Detect on the 32nd rising edge of SCK.
- SEN is de-asserted on the 32nd falling edge of SCK.
- The 32nd falling edge of SCK completes the READ cycle.

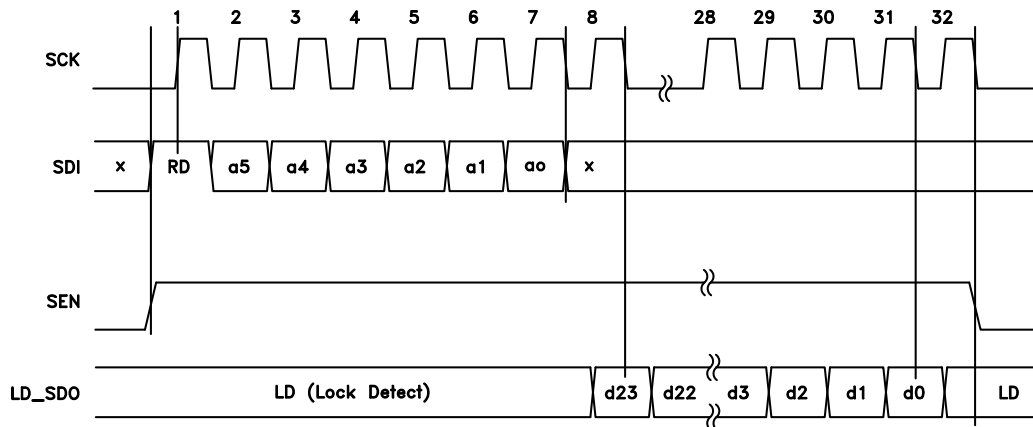


Figure 8. Serial Port Timing Diagram - READ Serial Port Operation



PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

20.0 Register Map

20.1 Reg 00h ID (Read Only) Register

Note: For Read Operations from register 00h, it is Read Only containing the chip ID. Current Hittite PLL with Integrated VCO chip IDs are shown below.

Bit	Name	Width	Default	Description
[23:0]	chip_ID	24	485901	PLL Identification

20.2 Reg 00h RST Strobe Register

For write operations to register 00h, it is a Write Only strobe register as defined below.

Bit	Name	Width	Default	Description
[0]	rst_swrst	1	n/a	Strobe (WRITE ONLY) generates soft reset. Resets all digital and registers to default states.

20.3 Reg 01h RST Register

Bit	Name	Width	Default	Description
[0]	rst_chipen_pin_select	1	1	1 = Chip enable via CE pin, CE (Pin 23) enables chip. CE low puts chip in power down. 0 = Chip enable via SPI (rst_chipen_from_spi), CE Pin is ignored
[1]	rst_chipen_from_spi	1	0	1= Chip Enable when rst_chipen_pin_select = 0 0= Power Down when rst_chipen_pin_select = 0 see Power Down Mode description and csp_enable Reg07 <20> If rst_chipen_pin_select =1 this register is ignored
[2]	rst_chipen_digclks_keep_on	1	0	keeps digital clocks on when chip is Power Down from any source
[3]	rst_chipen_bias_keep_on	1	0	keeps chip internal bias generators on when chip is Power Down from any source
[4]	rst_chipen_pfd_keep_on	1	0	keeps internal PFD block on when chip is Power Down from any source
[5]	rst_chipen_chp_keep_on	1	0	keeps internal Charge Pump block on when chip is Power Down from any source
[6]	rst_chipen_refbuf_keep_on	1	0	keeps reference path buffer on when chip is Power Down from any source
[7]	rst_chipen_vcobuf_keep_on	1	0	keeps VCO path RF buffer on when chip is Power Down from any source
[8]	rst_chipen_dig_io_keep_on	1	0	keeps digital IO pins on when chip is Power Down from any source
[9]	rst_chipen_rdiv_fe_sync	1	0	Tri-states the PFD on the next falling edge of the ref clock and also puts the chip to sleep

20.4 Reg 02h REFDIV Register

Bit	Name	Width	Default	Description
[13:0]	rdiv	14	1	Reference Divider 'R' Value (EQ 4) 00h - illegal 01h - divide-by-1 (bypass) 01h - divide-by-2 01h - divide-by-3 etc ... 3FFFh - divide-by-16, 383 The reference divider is controlled by several bits in register 8. See register 8 description for details.



PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

20.5 Reg 03h Frequency Register - Integer Part

Bit	Name	Width	Default	Description		
[15:0]	intg	16	C8h	VCO Divider Integer part, used in all modes, see (EQ 4)		
				<table border="1"> <tr> <td>Fractional Mode min 36d max $2^{16} - 1 = 65,535d$</td> <td>Integer Mode min 32d max $2^{16} + 31 = 65,567d$</td> </tr> </table>	Fractional Mode min 36d max $2^{16} - 1 = 65,535d$	Integer Mode min 32d max $2^{16} + 31 = 65,567d$
Fractional Mode min 36d max $2^{16} - 1 = 65,535d$	Integer Mode min 32d max $2^{16} + 31 = 65,567d$					

20.6 Reg 04h Frequency - Fractional Part Register

Bit	Name	Width	Default	Description		
[23:0]	frac	24	0	VCO Divider Fractional part (24-bit unsigned) see section Fractional Frequency Tuning		
				<table border="1"> <tr> <td>Used in Fractional Mode only min 0d max $2^{24} - 1$</td> <td></td> </tr> </table>	Used in Fractional Mode only min 0d max $2^{24} - 1$	
Used in Fractional Mode only min 0d max $2^{24} - 1$						

20.7 Reg 05h SD Seed Register

Bit	Name	Width	Default	Description
[23:0]	seed	24	0	Fractional Mode: Seeds fractional modulator FSK Mode: Sets f1 in FSK mode when fsk_enable=1 (see section FSK Modulation)



PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

20.8 Reg 06h SD CFG Register

Bit	Name	Width	Default	Description
[7:0]	reserved		87h	
[9:8]	order	2	2h	Select the Modulator Type 0 - not used 1 - not used 2 - Type 1 3 - Type 2
[10]	frac_rstb	1	1	0 holds the frac core in reset reset is used for integer mode or integer mode with CSP
[11]	buff_rstb	1	1	0 holds the frac core buffers in reset reset is used with frac_rstb=0 for integer mode, no CSP
[12]	bypass_mode	1	0	1 fractional modulator output is ignored, but fractional modulator continues to be clocked, used to test the isolation of the digital fractional modulator from the VCO output in integer mode
[13]	AutoSeed_mode	1	1	loads the seed whenever the frac register is written
[14]	reserved	1	0	Must be kept at 0
[15]	fsk_enable	1	0	enables the FSK mode of operation and FSK input on SDI pin, (see section FSK Modulation)
[16]	reserved	1	0	
[17]	clkqr_refdiv_sel	1	0	selects the SD clock source 1 = reference divider clock 0 = VCO divider clock
[18]	clkqr_invert_clk	1	1	inverts the selected sd clock
[19]	sd_spare_out	1	0	spare
[23:20]	csp_corr_magn	4	8h	CSP magnitude correction (see section Cycle Slip Prevention (CSP)) 0000 low magnitude 1111 high magnitude sign of the correction is determined automatically by the CSP state machine

See section PFD Lock Detect for more information about this register.

Note: To Enable Frac Mode:

Set Reg 6 [12:10]= 011

Also, Reg 9[9:7] or Reg 9[4:2] must be adjusted to mitigate spurs in frac mode (Dn or Up Leakage)



PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

20.9 Reg 07h LKD/CSP Register

Bit	Name	Width	Default	Description
[9:0]	wincnt_max	10	250	lock detect window sets the number of consecutive counts of divided VCO that must land inside the Lock Detect Window to declare LOCK
[10]	lkd_enable	1	1	enables internal lock detect function, Note output to Lock Detect Flag on LD_SDO as per Figure 13 controlled by pfd_LD_opEn, Reg 0Bh PFD Register
[11]	lkd_winasym_enable	1	0	asymmetrical window enables lock detect window to only lag or only lead the divided reference signal at the PFD, see Figure 9
[12]	lkd_win_asym_up_sel	1	0	1 selects lead window when lkd_winasym_enable=1 0 selects lag window when lkd_winasym_enable=1
[13]	ringosc_oneshot_sel	1	0	1 ring osc based one shot for lock detection mode 0 nominal 20nsec analog one shot for lock detection mode
[16:14]	oneshot_duration	3	0	duration of the ringosc based oneshot pulse in lock detection mode
[18:17]	ringosc_cfg	2	0	Lock Detect ringosc frequency trim "00" fastest "11" slowest
[19]	ringosc_mode	1	0	force ringosc ON
[20]	csp_enable	1	1	cycle slip prevention (CSP) enable

See section PFD Lock Detect for more information about this register.

20.10 Reg 08h Analog EN Register

Bit	Name	Width	Default	Description
[0]	bias_en	1	1	enables main chip bias reference
[1]	cp_en	1	1	charge pump enable
[2]	pfd_en	1	1	pfd enable
[3]	refbuf_en		1	reference path buffer enable. Set to 1 for normal operation.
[4]	vcobuf_en	1	1	vco path RF buffer enable
[5]	gpio_pads_en	1	1	gpio pads enable, Pi ns D0 and D1 required for use of GPO port or VCO Serial Port
[6]	sdo_pad_en	1	1	LD_SDO pad driver enable (Pin 5) required for use of Lock Detect, Serial Port Read Operation or VCO Serial Port operation
[7]	vcodiv_digclk_en	1	1	vco divider output clk to digital enable
[8]	vcodiv_en	1	1	enable vco divider
[9]	reserved	1	0	
[10]	vcodiv_dutycyc_mode	1	0	vcodiv duty cycle mode stretches the VCO divider output when N>32
[11]	reserved	1	0	Set to 0 for normal operation
[12]	rdiv_ref_to_dig_en	1	1	reference input applied to digital when set to 1, non-divided reference signal is fed to digital (required for normal operation)
[13]	rdiv_refdiv_to_dig_en	1	1	reference divider applied to digital, when set to 1, divided reference signal is fed to digital (required for normal operation)

Charge Pump control register. see [Figure 6](#)



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20.11 Reg 09h CP Register

Bit	Name	Width	Default	Description
[1:0]	Reserved set them to 0	2	0	
[4:2]	cp_UPoffset_sel	3	0	Charge Pump UP Offset Control 55 μ A/step 000 = 0 μ A 001 = 55 μ A 010 = 110 μ A ... 111 = 385 μ A
[6:5]	Reserved Set them to 0	2	0	
[9:7]	cp_DNoffset_sel	3	0	Charge Pump DN Offset Control 55 μ A/step 000 = 0 μ A 001 = 55 μ A 010 = 110 μ A ... 111 = 385 μ A Charge Pump Register Addr 9 Bit Functions: Bits [1:0] Reserved Set them to 0 Bits [4:2] cp_UPoffset_sel Bits [6:5] Reserved Set them to 0 Bits [9:7] cp_DNoffset_sel"
[13:10]	cfg_cp_UPtrim_sel	4	0	Charge Pump UP Current Trim 7 μ A/step 0000 = 0 μ A 0001 = 7 μ A 0010 = 14 μ A 0100 = 28 μ A 1000 = 56 μ A 1111 = 105 μ A
[17:14]	cp_DNtrim_sel	4	0	Charge Pump DN Current Trim 7 μ A/step 0000 = 0 μ A 0001 = 7 μ A 0010 = 14 μ A 0100 = 28 μ A 1000 = 56 μ A 1111 = 105 μ A
[20:18]	cp_UPcurrent_sel	3	0	Charge Pump UP MAIN Current Control 500 μ A step 000 tristate if PFD also disabled 001 500 μ A 010 1000 μ A 011 1500 μ A 100 2000 μ A 101 2000 μ A 110 2000 μ A 111 2000 μ A
[23:21]	cp_DNcurrent_sel	3	0	Charge Pump UP MAIN Current Control 500 μ A step 000 tristate if PFD also disabled 001 500 μ A 010 1000 μ A 011 1500 μ A 100 2000 μ A 101 2000 μ A 110 2000 μ A 111 2000 μ A



PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS PRODUCT & OPERATING GUIDE

20.12 Reg 0Ah CP Op Amp Register

Bit	Name	Width	Default	Description
[1:0]	cp_opamp_bias_sel	2	0	Charge Pump Internal Op-Amp bias select 00 - 540 μ A 01 - 689 μ A 10 - 943 μ A 11 - 1503 μ A Enabled with Chg Pump enable Note: this circuit affects internal charge pump operation and linearity. Default setting is recommended. Enabled with Reg08h[1] cp_en

20.13 Reg 0Bh PFD Register

Bit	Name	Width	Default	Description
[2:0]	pfd_del_sel	3	0	sets PFD reset path delay When in Integer mode, Reg B Bits [2:0] should not be 000 because it doesn't ensure sufficient 'on' time for the CP at 50MHz. This isn't an issue in Fractional Mode;
[3]	pfd_phase_sel	1	0	Swaps the PFD inputs 1 negative VCO tuning slope 0 positive VCO tuning slope
[4]	pfd_up_en	1	1	enables the PFD UP output according to state of pfd_mute_when_locked_enable, see Reg0B<9>
[5]	pfd_dn_en	1	1	enables the PFD DN output according to state of pfd_mute_when_locked_enable, see Reg0B<9>
[6]	pfd_LD_opEn	1	1	pfd Lock Detect Output Enable, enables Lock Detect flag output to LD_SDO pin
[7]	pfd_pullup_ctrl	1	0	Forces PFD UP output on
[8]	pfd_puldn_ctrl	1	0	Forces PFD DN output on
[9]	pfd_mute_when_locked_enable	1	0	1: if set: when locked disables UP if pfd_up_en=1 when locked disables DN if pfd_dn_en=1 when NOT locked, allows both UP and DN to be active and ignores pfd_up_en and pfd_dn_en 0: if clear, pfd_dn_en and pfd_up_en enable UP and DN outputs at all times
[10]	spare0	1	0	reserved
[11]	spare1	1	1	reserved

20.14 Reg 0Ch VCO SPI Register

Bit	Name	Width	Default	Description
[9:0]	vcospi_vco_data	10	0	data register contents, when written automatically outputs this data via VCO SPI when to_gpo_sdo=1 Reg09<7>



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20.15 Reg 0Dh GPO_SPI_RDIV Register

Bit	Name	Width	Default	Description
[3:0]	gpo_select	4	10d	Test signals selected here are output to gpo pi ns when <i>gpo_pads_en=1</i> (Reg 0Bh) D1 & D0 0: clk_vcdiv & clk_refdiv 1: pfd_up & pfd_dn 2: refOut & refDivOut 3: seed_stb_sypulse_test & frac_stb_sypulse_test 4: intg_inbuff_enable_test & clk_sd 5: oneshot_trigg_test & oneshot_pulse_test 6: '0' & ringosc_test 7: csp_corr_add & csp_corr_sub 8: pfd_sat_refdiv & pfd_sat_vcdiv 9: (csp_corr_add or csp_corr_sub) & pfd_sat_rstb 10: gpo_test , see Reg0D<5:4> 11: not used 12: not used 13: not used 14: not used 15: not used
[5:4]	gpo_test	2	0	data written to this register is output to D0 and D1 pi ns when gpo_select = 10d
[6]	refclkdiv4	1	0	1: sel ref divby4 for clocking the vco_spi 0: sel ref divby1 for clocking the vco_spi
[7]	to_gpo_sdo	1	0	enable the automatic output of vcspi_vco_data to LD_SDO Output VCO_SPI clock to D1 (see Reg0D<6>) Output VCO_SPI EN to D0

20.16 Reg 0Fh LD State Register (Read Only)

Bit	Name	Width	Default	Description
[0]	locked	3	0	Read only Lock Detect flag, 1 when locked

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PRODUCT & OPERATING GUIDE**

Notes:

A

PRODUCT & OPERATING GUIDE