

NCP374

Overvoltage Up to +30 V and Down to -30 V with Load Switch Function

NCP374 is an over-voltage and over-current protection device. From IN to VBUS, the part acts as a load switch protection, with programmable current regulation. The current protection is externally adjustable.

Additional voltage protection is available, from VBUS to IN. Due to built-IN low $R_{DS(on)}$ NMOS fet, the host system is protected against positive and negative voltage up to +28 V and down to -28 V.

The both embedded over-current and over-voltage protection allows sustaining extreme conditions from short circuit on USB connector, or defective WA or USB port.

Due to the NCP374 using internal NMOS, the system cost and the PCB area of the application board are minimized.

NCP374 provides a negative going flag (\overline{FLAG}) output, which alerts the system that a fault has occurred.

Features

- Adjustable Over-Current
- Over-voltage Protection Up to 28 V and Down to -28 V
- Logic Pins \overline{EN} and \overline{DIR}
- Thermal Shutdown
- On-Chip Low $R_{DS(on)}$ NMOS Transistors
- Over-Voltage Lockout (OVLO)
- Soft Start.
- Real Shutdown Mode
- Alert \overline{FLAG} Output.
- 12 Leads LLGA 4 x 4 mm Package
- This is a Pb-Free Device

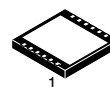
Typical Applications

- USB Ports
- Tablets
- Set Top Box
- Cell Phones



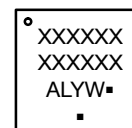
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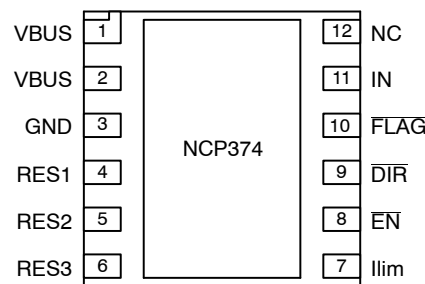
TLLGA12
CASE 513AP

MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 10 of this data sheet.

NCP374

FUNCTIONAL BLOCK DIAGRAM

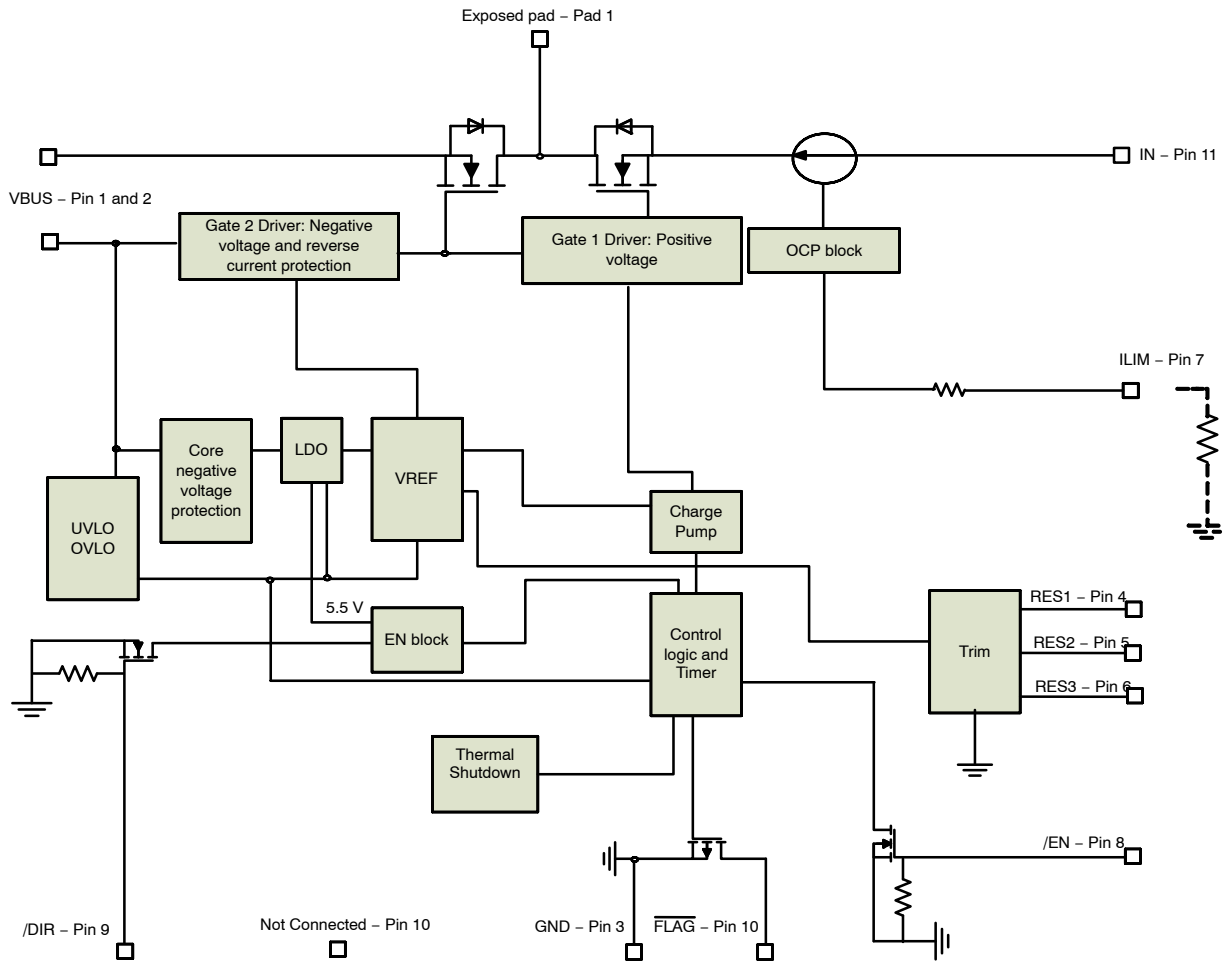


Figure 3. Functional Block Diagram

NCP374

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
1, 2	VBUS	POWER	VBUS voltage pins: must be hardwired together on the PCB. These pins are connected to the VBUS connector, and are protected against positive and negative overvoltage events. A 1 μ F low ESR ceramic capacitor, or larger, must be connected between these pins and GND.
3	GND	POWER	Ground
4	RES1	INPUT	Reserved pin. Must be connected to GND potential and used for IC test.
5	RES2	INPUT	Reserved pin. Must be connected to GND potential and used for IC test.
6	RES3	INPUT	Reserved pin. Must be connected to GND potential and used for IC test.
7	Ilim	OUTPUT	Current Limit Pin. This pin provides the reference, based on the internal band-gap voltage reference, to limit the over current, across internal NMosFet. A 0.1% tolerance resistor shall be used to get the highest accuracy of the Over Current Limit.
8	EN	INPUT	Enable Pin. In combination with DIR, the internal NMOSes are turned on if Battery is applied on the IN pins. (See logic table) In enable mode, the internal Over-Current protection is activated from IN to VBUS. When enable mode is disabled, the NCP374 current consumption, into IN pin, is drastically decreased to limit current leakage of the self powered devices.
9	DIR	INPUT	Direct Mode pin. This pin can be used, in combination with Enable pin, for the front end protection applications like wireless devices. In this case, the part can be used as +/- OVP only. See logic table.
10	FLAG	OUTPUT	Fault indication pin. This pin allows an external system to detect fault condition. The FLAG pin goes low when input voltage exceeds OVLO threshold or drops below UVLO threshold (charging mode), charge current from IN to VBus exceeds current limit or internal temperature exceeds thermal shutdown limit. Since the FLAG pin is open drain functionality, an external pull up resistor to VBat must be added (10 k Ω minimum value).
11	IN	POWER	IN pin. In Front end application this pin is connected to charger device input or PMIC input. In host application, this pin is connected to upstream DCDC. This pin is used as power supply of the core and current from IN to VBUS is then limited to the external
12	NC	NA	Not internally connected. Can be connected to any potential.
13	PAD1	POWER	Drain connection of the back to back MOSFET's. This exposed pad mustn't be connected to any other potential and must be used for thermal dissipation of the internal MOSFETs.

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage (VBus to GND)	Vmin _{VBUS}	-30	V
Minimum Voltage (All others to GND)	Vmin	-0.3	V
Maximum Voltage (Vbus to GND)	Vmax _{VBUS}	30	V
Maximum Voltage (IN to GND)	Vmax _{IN}	10	V
Maximum Voltage (All others to GND)	Vmax	7	V
Maximum DC current NCP374MU075TXG Charge Mode Vbus Mode	I _{in}	2 900	A mA
Thermal Resistance, Junction to Air, (Note 1)	R _{θJA}	80	°C/W
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Junction Operating temperature	T _J	150	°C
Moisture Sensitivity	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The R_{θJA} is highly dependent on the PCB heat sink area (connected to PAD1). See PCB recommendation paragraph.

ELECTRICAL CHARACTERISTICS Min / Max limits values (-40°C < T_A < +85°C) and IN = +5 V (Unless otherwise noted). Typical values are T_A = +25°C

Characteristics	Symbols	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V _{in}		2.5		5.5	V
Vbus Voltage Range	V _{vbus}	All modes			28	V
			-28			V
		All modes IN = 5 V	-23			V
Under Voltage Lockout Threshold	UVLO	Vbus falls down UVLO threshold Disable, Charge mode and Enhance Modes	2.6	2.7	2.8	V
Under Voltage Lockout Hysteresis	UVLO _{hyst}	Vbus rises up UVLO threshold + UVLO _{hyst}	45	60	75	mV
Over voltage Lockout threshold	OVLO	Vbus rises up OVLO threshold	5.6	5.77	5.9	V
Over Voltage Lockout Hysteresis	OVLO _{hyst}	Vbus falls down to OVLO - OVLO _{hyst}	45	65	90	mV
Vbus versus IN Resistance IN versus Vbus Resistance	R _{Dson}	Vbus = 5 V, or IN = 5 V NCP374MU075TXG 25°C 85°C		90	140 155	mΩ
Quiescent Current	I _{ddIN}	No load. Vbus mode, V _{in} = 5 V		200	315	μA
Standby Current	I _{ddSTD}	No load, IN = 5 V. Standby mode, No Vbus		0.02	1	μA
Current limit	I _{OCP}	IN = 5 V, Load on Vbus, Vbus mode R _{LIM} = 0 Ω NCP374MU075TXG	600	750	900	mA

NOTE: Electrical parameters are guaranteed by correlation across the full range of temperature.

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ELECTRICAL CHARACTERISTICS Min / Max limits values ($-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$) and $I_N = +5\text{ V}$ (Unless otherwise noted). Typical values are $T_A = +25^{\circ}\text{C}$

Characteristics	Symbols	Conditions	Min	Typ	Max	Unit
FLAG Output Low Voltage	$V_{ol_{flag}}$	Fault mode Sink 1 mA on FLAG pin			400	mV
FLAG Leakage Current	\overline{FLAG}_{leak}	FLAG level = 5.5 V		1		nA
DIR Voltage High	V_{ih}		1.2			V
DIR Voltage Low	V_{ol}				0.4	V
DIR Leakage Current	\overline{DIR}_{leak}	DIR = 5.5 V		300		nA
EN Voltage High	V_{ih}		1.2			V
EN Voltage Low	V_{ol}				0.4	V
EN Leakage Current	EN_{leak}	EN = 5.5 V		300		nA
Thermal Shutdown temperature	T_{SD}			150		$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	T_{SDHYST}			30		$^{\circ}\text{C}$

TIMINGS

Vbus Mode

Start Up Delay	$T_{onV_{bus}}$	$I_N \geq 2.5\text{ V}$, from $\overline{EN} = 1.2$ to 0.4 to $V_{bus} \geq 0.3\text{ V}$ Vbus Mode	0.6	1.2	1.8	ms
FLAG going up Delay	$T_{startV_{bus}}$	From $I_N \geq 0.3\text{ V}$ FLAG = 1.2 V, Vbus Mode	0.6	1.2	1.8	ms
Rearming Delay	t_{RRD}	$I_N > 2.5\text{ V}$, $R_{in} = 1\ \Omega$ Vbus Mode, after fault	15	30	45	ms
Over Current Regulation Time	t_{reg}	$I_N > 2.6$, $V_{bus} > 0.3\text{ V}$ Vbus Mode	0.5	1.2	1.8	ms
OCP delay time	t_{OCP}	From $I_V_{bus} > I_{lim}$, 1 A/1 μs		5		μs
Vbus Disable time	$T_{V_{bus}DIS}$	From $\overline{EN} = 0.4\text{ V}$ to 1.2 V , to $V_{bus} < 0.3\text{ V}$. $I_N = 5\text{ V}$		165		μs
Turn off delay	t_{off}	From $I_N > OVLO$ to $V_{bus} \leq 0.3\text{ V}$ V_{in} increasing from 5 V to 8 V at 3 V/ μs		1.5	5	μs

Charging Mode

Start Up Delay	t_{on}	From $V_{bus} > UVLO$ to $I_N = 0.3\text{ V}$, charging mode	15	30	45	ms
FLAG going up Delay	t_{start}	From $I_N > 0.3\text{ V}$ to FLAG = 1.2 V	15	30	45	ms
Turn off delay	t_{off}	From $V_{bus} > OVLO$ to $I_N \leq 0.3\text{ V}$ V_{in} increasing from 5 V to 8 V at 3 V/ μs		1.5	5	μs
Alert delay	t_{stop}	From $V_{bus} > OVLO$ to FLAG $\leq 0.4\text{ V}$ See Figures 3 and 9 V_{in} increasing from 5 V to 8 V at 3 V/ μs		1.5		μs
Disable time	t_{dis}	EN = 1.2 V, From DIR = 0.4 to 1.2 V to $I_N \leq 0.3\text{ V}$		2.5		μs

NOTE: Electrical parameters are guaranteed by correlation across the full range of temperature.

TYPICAL OPERATING CHARACTERISTICS

Operation

The NCP374 acts as an over-voltage in charge mode, when wall adapter or Vbus cable is connected to Vbus pin of the device. The downstream system (transceiver, CCCV charger..) are protected up to +30 V if charging voltage exceeds OVLO threshold (5.77 V). Due to a back to back architecture, the Vbus pin is also protected against reverse polarity connection, coming from wrong USB cables. This negative protection acts down to -30 V.

In *disable mode* ($\overline{EN} = 1$, $\overline{DIR} = 1$), there is no current consumption on IN pin and MOSFETs are turned off (Vbus cable disconnected)

The NCP374 provides over-current from IN to Vbus by selecting Vbus mode.

To active *Vbus mode* (USB port on), the \overline{EN} pin must be tied low. In this case, MOSFET are turned on and current is measure in the branch. If the sinking current on the Vbus pin is above the programmed current on Ilim pin (can be programmed up to TBD), the Vbus current is regulated around Iocp during treg time. If the overload is present at the end of this timer, the Mosfet are turned off and automatic rearming cycle is activated. With Treg/Ttrd cycle until overload is present.

Over-voltage Lockout (OVLO)

To protect the connected system on IN pins, from external over-voltage coming from USB connector or Wall Adapter, through Vbus pin, the device has a built-in over-voltage lock out (OVLO) circuit. During over-voltage condition, the output remains disabled until the input voltage exceeds OVLO (Vbus pin).

The OVLO comparator is available in all modes.

Additional OVLO thresholds ranging from OVLO can be manufactured. Please contact your ON Semiconductor representative for further information.

\overline{FLAG} output is tied to low until V_{in} is higher than OVLO. This circuit has a built-in hysteresis to provide noise immunity to transient conditions.

Over-Current Protection (OCP)

This device integrates over current protection function, from IN to Vbus port.

That means the current across the internal NMOS is regulated when the value, set by external Rlim resistor, exceeds Ilimit during an internal timer.

An internal resistor is placed in series with the pin allowing to have a maximum OCP value when Ilim pin is directly connected to GND.

By adding external resistors in series with Ilim and GND, the OCP value is decreased. The Rlim tolerance is important to keep a good accuracy. So a value between 0.1% and 1% won't have an impact on the OCP accuracy. Nevertheless, the higher Rlim value, the lower Over current protection accuracy.

Indeed, the current is measured by a voltage comparator on a serial resistance. If this voltage drop comes very small, the offset of the internal comparator will have an impact on the accuracy. So a division by more than three times with Rlim will degrade drastically the overcurrent accuracy.

The current limit calculation formula for the NCP374MU075TXG is:

$$R_{lim}(\Omega) = 22150/I_{ocp} - 29035$$

During over current event, NMOSes are opened and \overline{FLAG} output is tied to low, allowing the μ Controller to take into account the fault event and then disable reverse charge path.

VBus Mode

To access to the Vbus mode, \overline{DIR} pin must be tied to high (>1.2) and \overline{EN} must be tied from high to low (< 0.4 V).

In that case, the core of the NCP374 will be supplied by the IN, with a 2.5 V minimum voltage and 5.5V maximum voltage.

In this state, OCP, OVLO and thermal modes are available.

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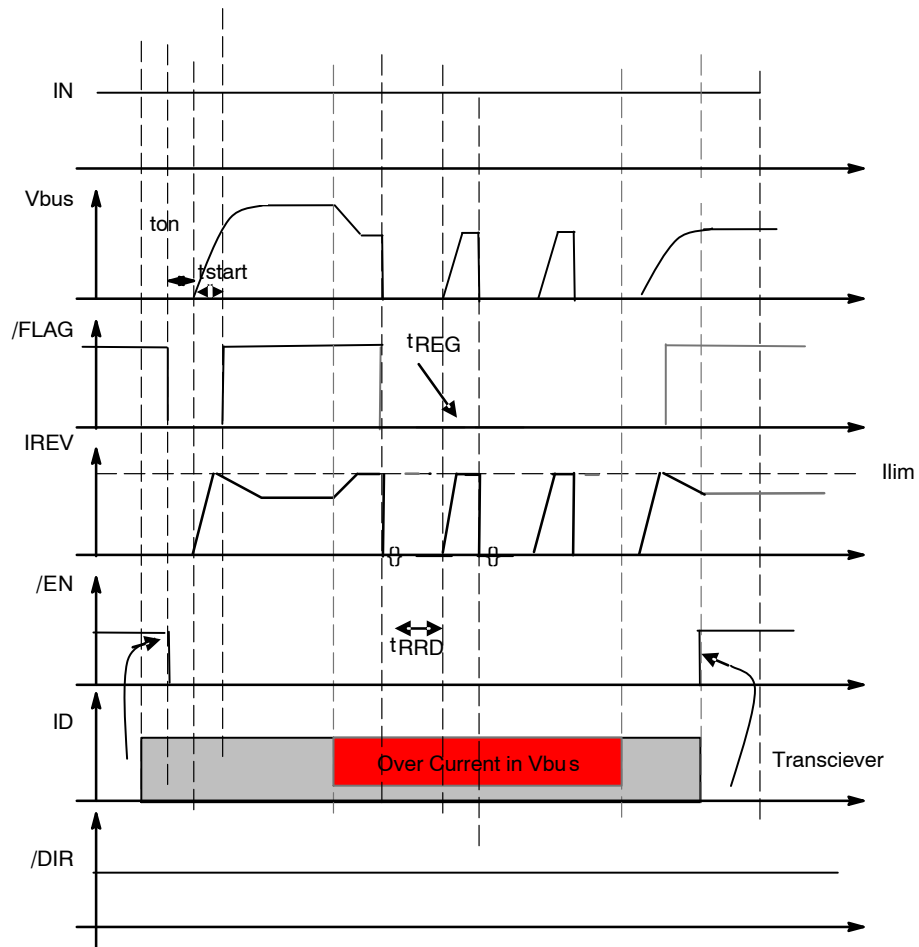


Figure 4. Over Current Protection sequence

In Vbus Mode, \overline{FLAG} pin remains available, allowing the μ controller to have a status regarding over-voltage

condition, over-current condition or thermal shutdown condition.

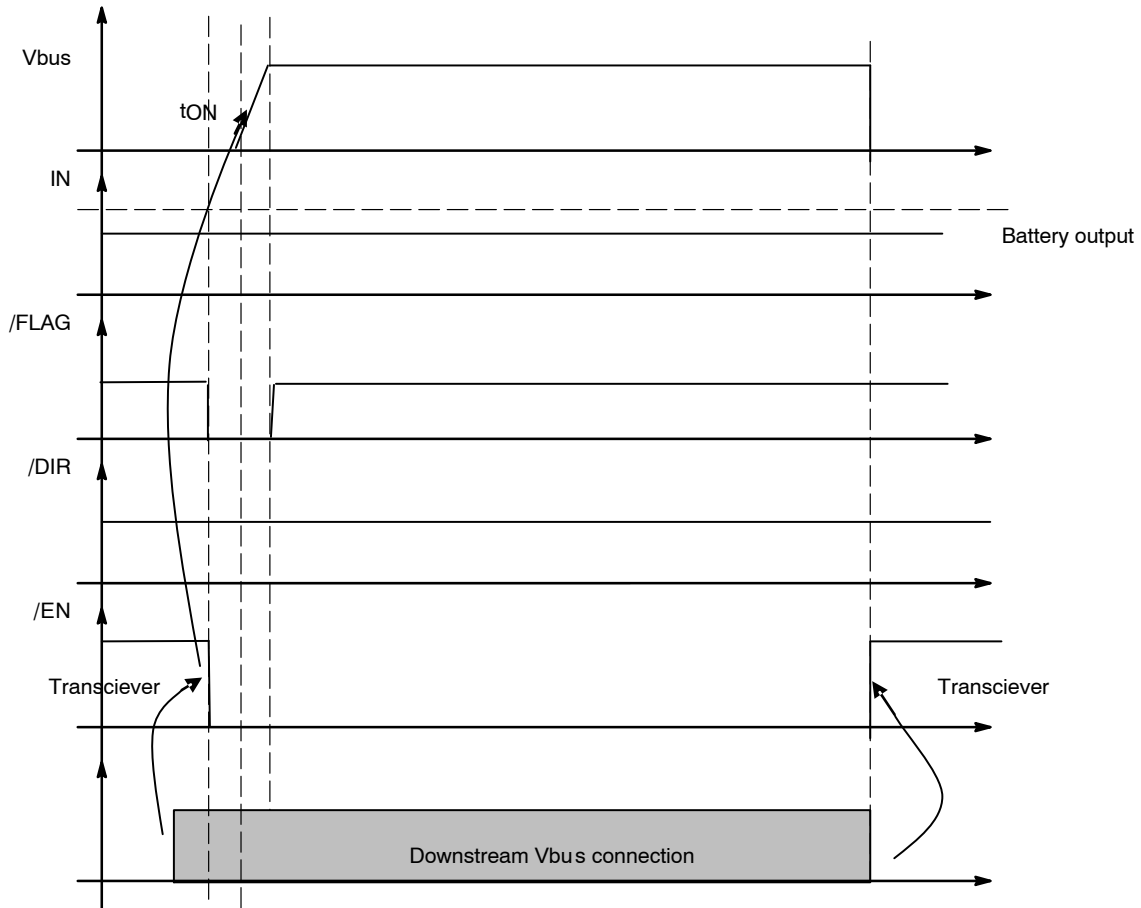


Figure 5. $\overline{\text{FLAG}}$ Status in Vbus Mode

Logic Inputs

To enable Charge operation (Charge Mode), the $\overline{\text{DIR}}$ pin shall be forced to low and $\overline{\text{EN}}$ to high. A high level on the

$\overline{\text{DIR}}$ pin disconnects IN pin from Vbus pin. $\overline{\text{DIR}}$ does not overdrive an OVLO or UVLO fault ($\overline{\text{FLAG}}$ status is still available).

Table 1. TABLE SELECTION OF CHARGE MODES

DIR	EN	MODE	Protection		
			OVP @ VBUS (+28 V, -28 V, OVLO 5.77 V)	OCP (IN to VBUS)	OCP (VBUS to IN)
0	0	NA	NA	NA	NA
0	1	Charge	Yes	NA	NA
1	0	VBUS	Yes	Yes	NA
1	1	Disable	Yes (out off)	NA	NA

Negative Voltage and Reverse Current

The device protects the system connected on IN pin from negative voltage occurring on Vbus pin, down to -28 V. When a negative voltage occurs, the IN pins are disconnected from Vbus pins. This negative protection is available in all modes

The thermal threshold has been set at 150°C. $\overline{\text{FLAG}}$ is then tied to low to inform the MCU.

As the thermal hysteresis is 30°C, the MOSFET will be closed as soon the device temperature falls down to 120°C.

If the fault event is still present, the temperature increase one more time and engages the thermal shutdown one more time until fault event disappeared.

Thermal Shutdown Protection

In case of internal overheating, the integrated thermal shutdown protection allows to open the internal MOSFET in order to instantaneously decrease the device temperature.

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PCB Recommendations

The under PAD1 of the NCP374 package shall be connected to an isolated PCB area to increase the heat transfer if necessary for an application standpoint.

In any case, the PAD1 shall be not connected to any other potential or GND than the isolated extra copper surface.

ORDERING INFORMATION

Device	Marking	Order Current Limit	Package	Shipping [†]
NCP374MU075TXG	NCP 374	750 mA	LLGA12 4x4 mm (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

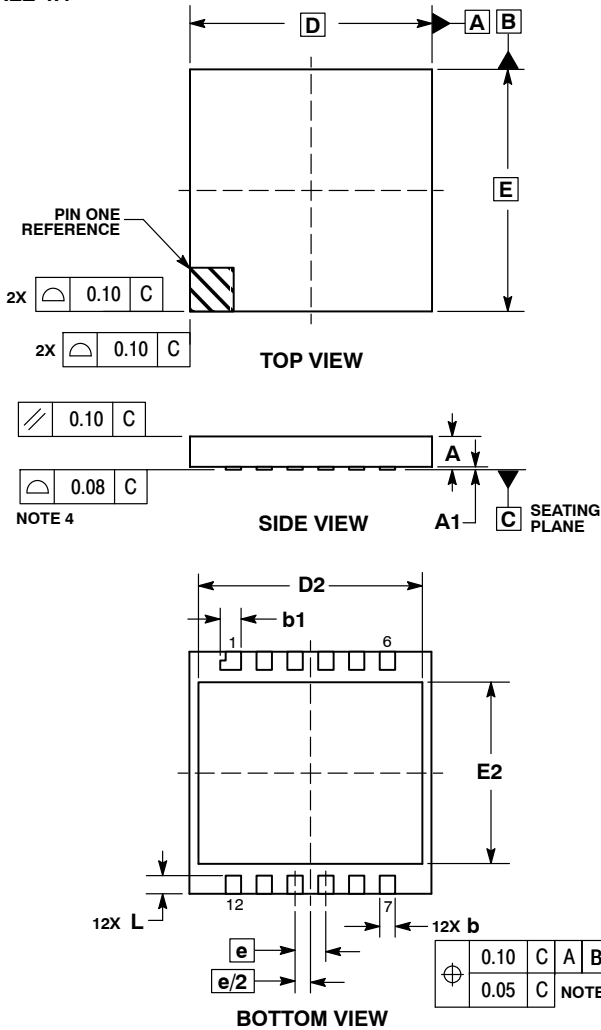
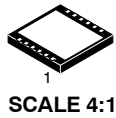
PACKAGE DIMENSIONS

ON Semiconductor®



TLLGA12 4x4, 0.5P
CASE 513AP
ISSUE O

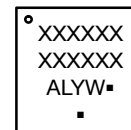
DATE 14 NOV 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.20	0.30
b1	0.35 REF	
D	4.00 BSC	
D2	3.65	3.75
E	4.00 BSC	
E2	2.95	3.05
e	0.50 BSC	
L	0.25	0.35

GENERIC MARKING DIAGRAM*

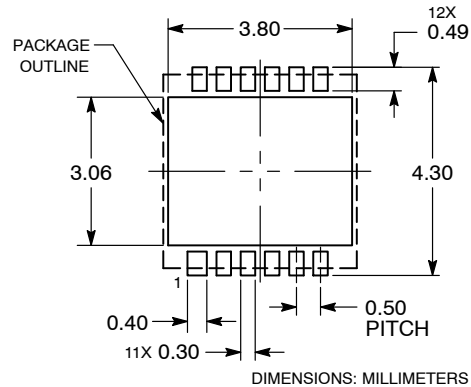


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(*Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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