

**MOSFET - Power,  
N-Channel, Shielded Gate,  
POWERTRENCH®  
100 V, 50 A, 10.6 mΩ**

**NTTFS010N10MCL**

**General Description**

This N-Channel POWETRENCH® MOSFET is produced using onsemi’s advanced POWETRENCH® process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

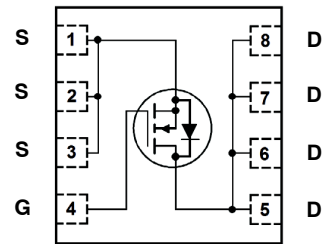
**Features**

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 10.6 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 15\text{ A}$
- Max  $r_{DS(on)}$  = 15.9 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 12\text{ A}$
- 50% Lower  $Q_{rr}$  than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

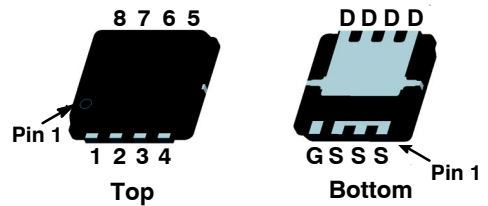
**Applications**

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive

**ELECTRICAL CONNECTION**

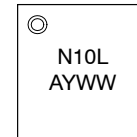


N-Channel MOSFET



WDFN8  
(3.3x3.3, 0.65 P)  
CASE 511DY

**MARKING DIAGRAM**



- N10L = Device Code
- A = Assembly Location
- Y = Year Code
- WW = Work Week Code

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.

# NTTFS010N10MCL

## MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	-Continuous $T_C = 25^\circ\text{C}$ (Note 5)	50
		-Continuous $T_C = 100^\circ\text{C}$ (Note 5)	32
		-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	10.7
		-Pulsed (Note 4)	250
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	73	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	52	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

## PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
NTTFS010N10MCLTAG	N10L	WDFN8 (3.3x3.3)	7"	12 mm	1500 Units

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		64		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 85 \mu\text{A}$	1.0	1.5	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 85 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-5.3		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$		9.1	10.6	m $\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 12 \text{ A}$		13.5	15.9	
		$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}, T_J = 125^\circ\text{C}$		15.3	17.8	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 15 \text{ A}$		54		S

### DYNAMIC CHARACTERISTICS

$C_{ISS}$	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1530	2150	pF
$C_{OSS}$	Output Capacitance			625	875	
$C_{RSS}$	Reverse Transfer Capacitance			10	18	
$R_G$	Gate Resistance		0.1	1.1	2.1	

# NTTFS010N10MCL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### SWITCHING CHARACTERISTICS

$t_{d(ON)}$	Turn – On Delay Time	$V_{DD} = 50\text{ V}, I_D = 15\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		9	19	ns
$t_{rd(ON)}$	Rise Time			3	10	
$t_{d(OFF)}$	Turn – Off Delay Time			28	45	
$t_f$	Fall Time			5	10	
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 50\text{ V}$ $I_D = 15\text{ A}$	22	30	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$		10		
$Q_{gs}$	Gate to Source Charge			4		
$Q_{gd}$	Gate to Drain “Miller” Charge			3		
$Q_{oss}$	Output Charge	$V_{DD} = 50\text{ V}, V_{GS} = 0\text{ V}$		41		
$Q_{sync}$	Total Gate Charge Sync	$V_{DS} = 0\text{ V}, V_{GS} = 0\text{ to }10\text{ V}$	19		nC	

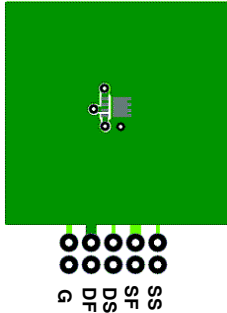
### DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)	0.7	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 15\text{ A}$ (Note 2)	0.8	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 8\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	22	36	ns
$Q_{rr}$	Reverse Recovery Charge		35	56	nC
$t_{rr}$	Reverse Recovery Time	$I_F = 8\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$	17	30	ns
$Q_{rr}$	Reverse Recovery Charge		79	126	nC

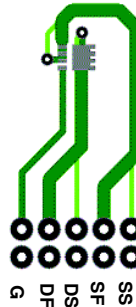
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



- 53°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



- 125°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.
- $E_{AS}$  of 73 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 3\text{ mH}$ ,  $I_{AS} = 7\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.5\text{ mH}$ ,  $I_{AS} = 13\text{ A}$ .
- Pulsed  $I_D$  please refer to Figure 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

# NTTFS010N10MCL

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

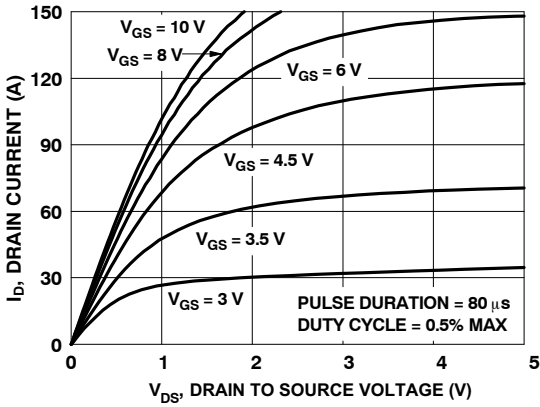


Figure 1. On Region Characteristics

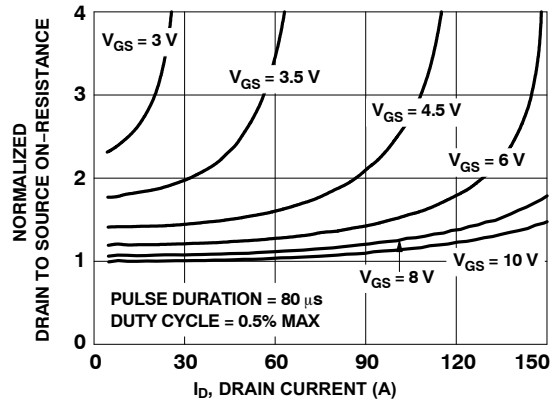


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

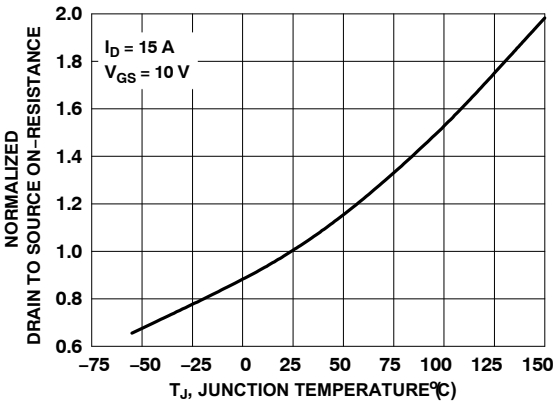


Figure 3. Normalized On Resistance vs. Junction Temperature

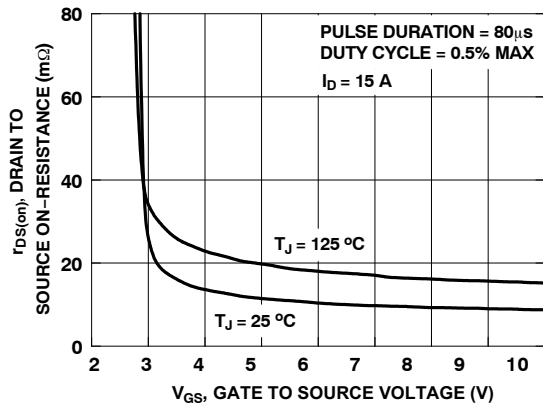


Figure 4. On-Resistance vs. Gate to Source Voltage

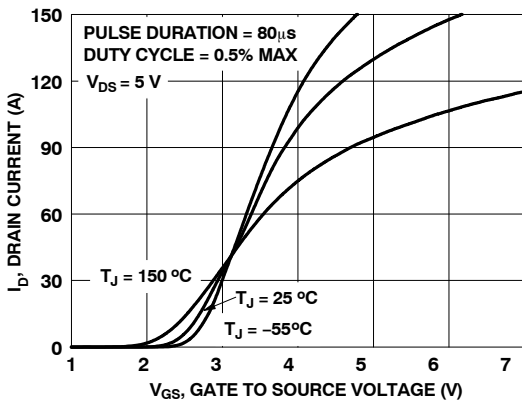


Figure 5. Transfer Characteristics

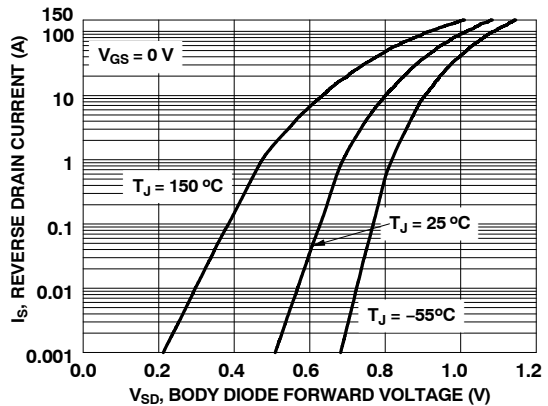


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# NTTFS010N10MCL

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

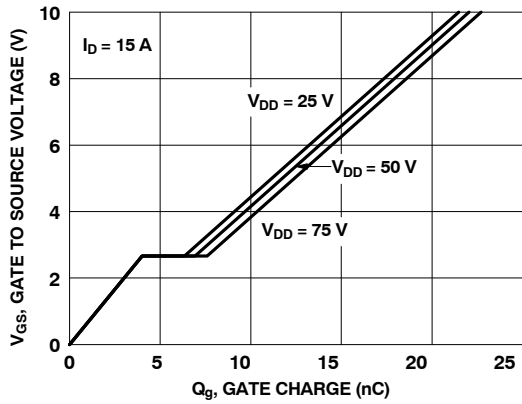


Figure 7. Gate Charge Characteristics

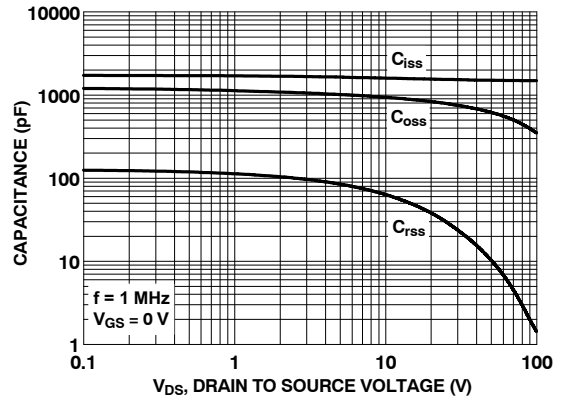


Figure 8. Capacitance vs. Drain to Source Voltage

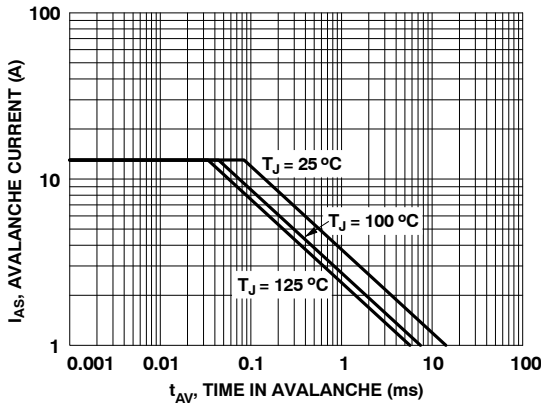


Figure 9. Unclamped Inductive Switching Capability

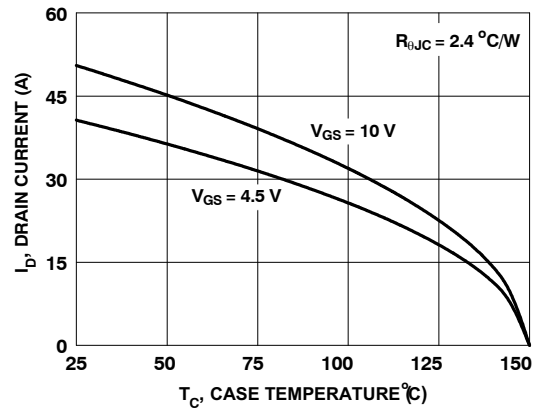


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

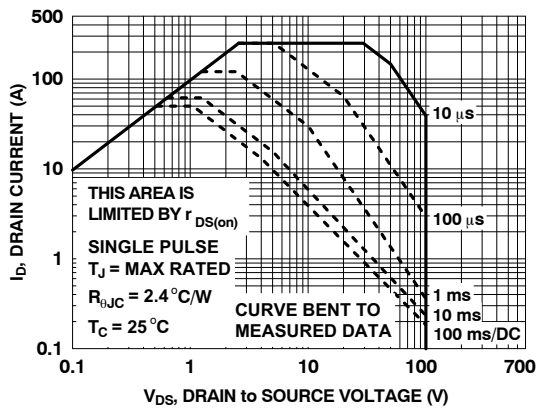


Figure 11. Forward Bias Safe Operating Area

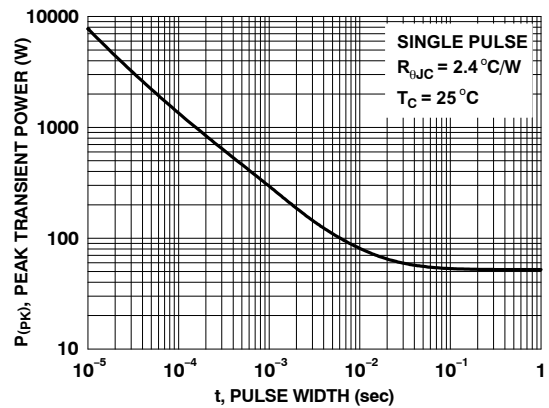


Figure 12. Single Pulse Maximum Power Dissipation

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## TYPICAL CHARACTERISTICS (continued)

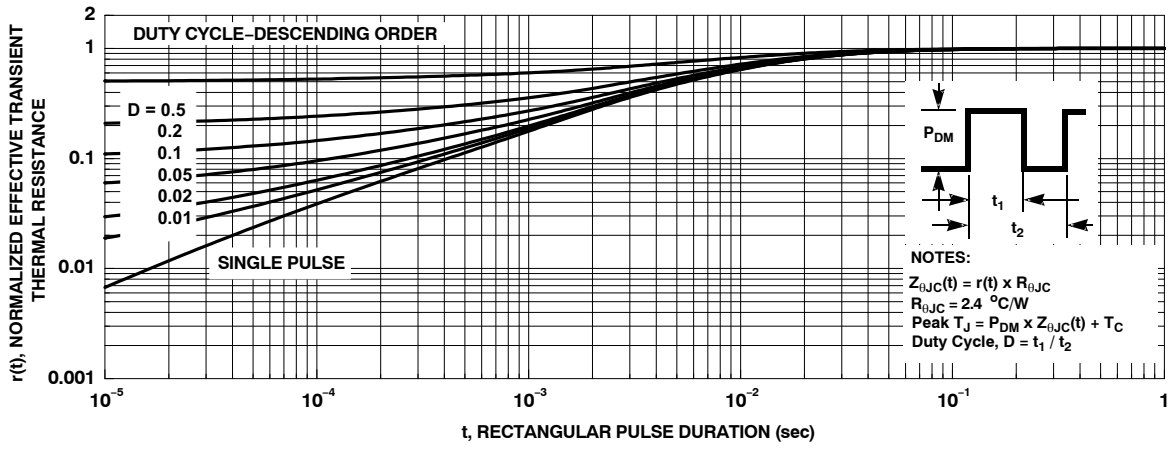


Figure 13. Junction-to-Case Transient Thermal Response Curve

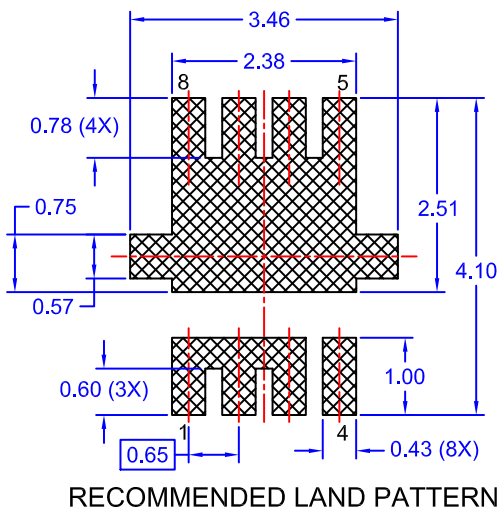
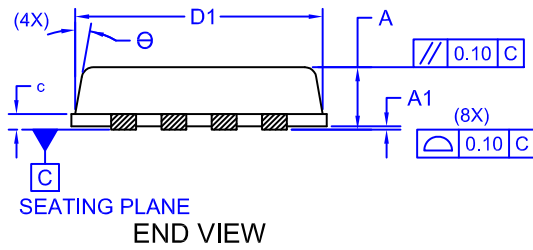
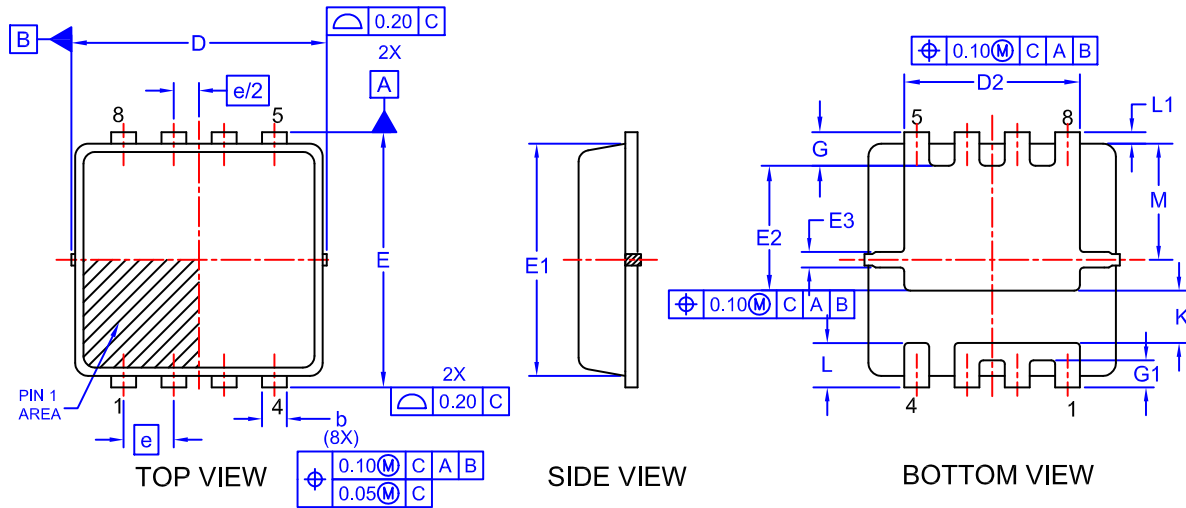
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



WDFN8 3.3x3.3, 0.65P  
CASE 511DY  
ISSUE A

DATE 21 AUG 2018

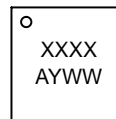


**NOTES:**

1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS D1 & E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
M	1.35	1.50	1.60
$\theta$	0	-	12

**GENERIC MARKING DIAGRAM\***



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year Code
- WW = Work Week Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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