PSMN014-40HLD

N-channel 40 V, 13.6 mOhm, logic level MOSFET in LFPAK56D using NextPowerS3 technology

26 September 2022 **Product data sheet**

1. General description

Dual logic level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using NextPowerS3 technology.

2. Features and benefits

- Dual MOSFET
- Repetitive avalanche rated
- High reliability LFPAK56D package
- Copper-clip, solder die attach
- Qualified to 175 °C

3. Applications

- Brushless DC motor control
- DC-to-DC converters
- High-performance synchronous rectification
- High performance and high efficiency server power supply

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	42	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	46	W
T_j	junction temperature			-55	-	175	°C
Static characteristics FET1 and FET2							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C		7.9	11.4	13.6	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 105 °C		10.9	16	20.4	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	I_D = 10 A; V_{DS} = 32 V; V_{GS} = 5 V; T_j = 25 °C		-	1.8	4.2	nC
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C		-	13	19.4	nC
Avalanche Ruggedness FET1 and FET2							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 39.9 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; Fig. 4	[2] [3]	-	-	10.6	mJ

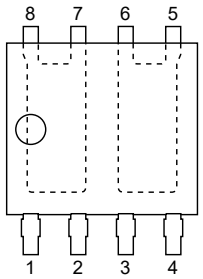
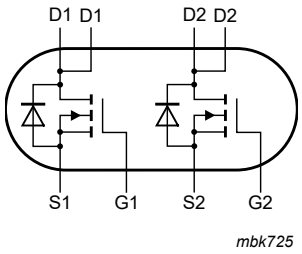
nexperia

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode FET1 and FET2							
Q_r	recovered charge	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C	[4]	-	16.2	-	nC

[1] 42A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.
[4] Includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 **LFPAK56D; Dual LFPAK (SOT1205)**	
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN014-40HLD	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN014-40HLD	14DS40H

8. Limiting values

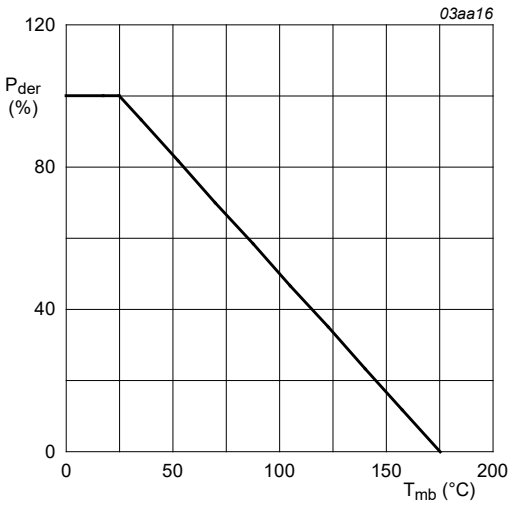
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{GS}	gate-source voltage	DC; T_j = 25 °C		-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	46	W

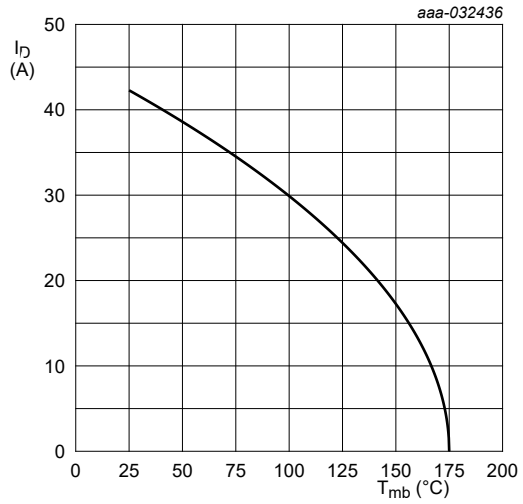
Symbol	Parameter	Conditions		Min	Max	Unit
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	42	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	30	A
I_{DM}	peak drain current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C; Fig. 3		-	169	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I_S	source current	T_{mb} = 25 °C		-	42	A
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	169	A
Avalanche Ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 39.9 A; $V_{sup} \leq$ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; Fig. 4	[2] [3]	-	10.6	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} = 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 4	[4]	-	39.9	A

[1] 42A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.
[4] Protected by 100% test



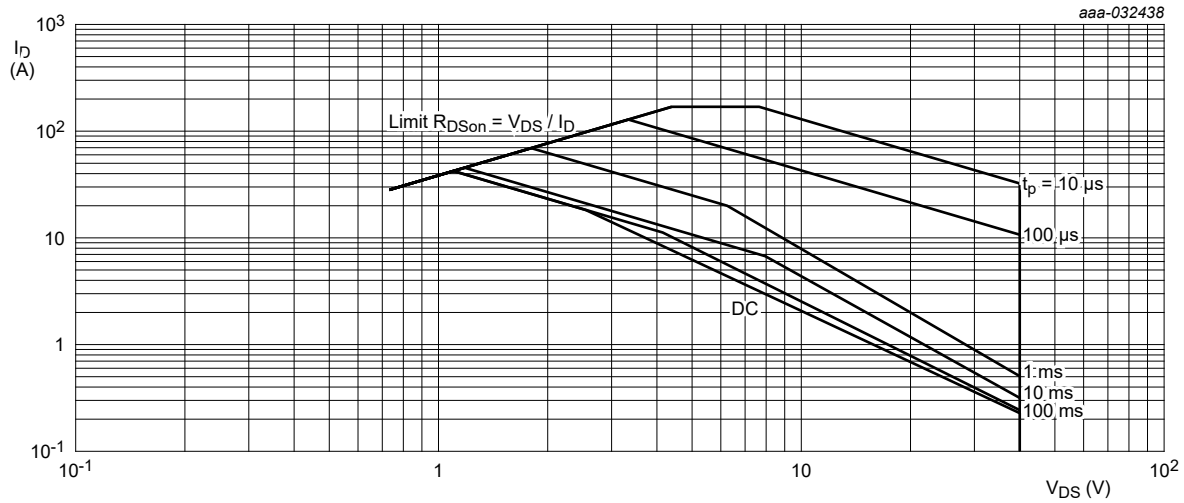
$$P_{der} = \frac{P_{tot}}{P_{tot(25\,°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



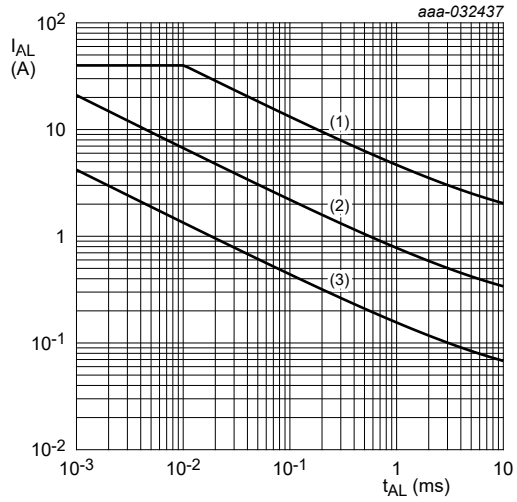
42 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
$V_{GS} \geq$ 10 V

Fig. 2. Continuous drain current as a function of mounting base temperature, FET1 and FET2



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain current as a function of drain-source voltage, FET1 and FET2



(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	3	3.23	K/W

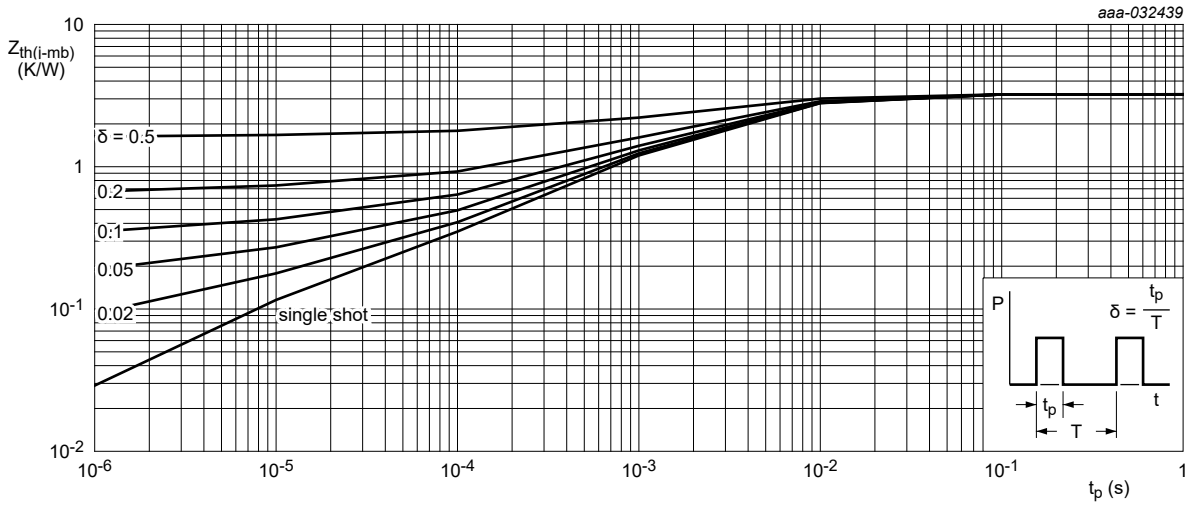


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

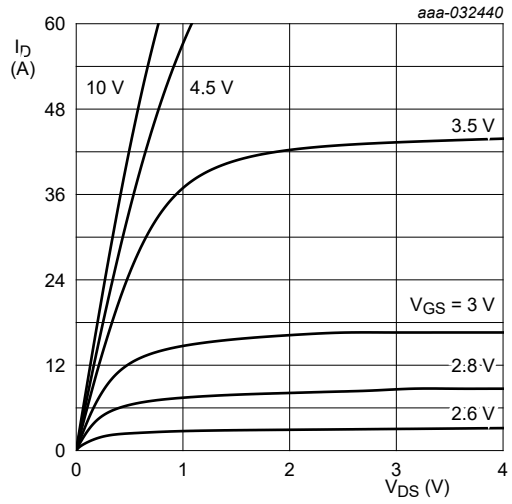
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	43	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C		-	40.5	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10		1.5	1.85	2.2	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 10		0.7	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 10		-	-	2.6	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.01	5	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 °C		-	0.14	10	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	26	500	µA
I_{GSS}	gate leakage current	V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C		7.9	11.4	13.6	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 105 °C		10.9	16	20.4	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 125 °C		12	17.4	21.9	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 175 °C		14.5	20.9	26.4	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 25 °C		9.8	14.1	16.9	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 105 °C		13.5	20	25.4	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 125 °C		14.8	21.6	27.2	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 175 °C		18	26.6	32.8	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.7	1.8	4.2	Ω

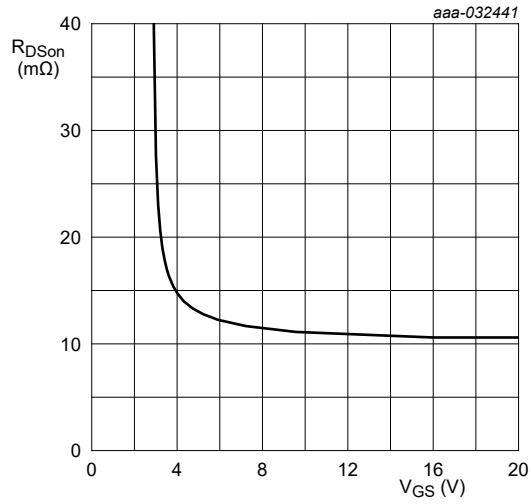
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics FET1 and FET2							
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C		-	13	19.4	nC
		I_D = 10 A; V_{DS} = 32 V; V_{GS} = 5 V; T_j = 25 °C		-	6.8	10.2	nC
Q_{GS}	gate-source charge			-	2.3	3.8	nC
Q_{GD}	gate-drain charge			-	1.8	4.2	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 11		-	848	1160	pF
C_{oss}	output capacitance			-	280	420	pF
C_{rss}	reverse transfer capacitance			-	39	84	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 32 V; R_L = 3.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	6.5	-	ns
t_r	rise time			-	9.7	-	ns
$t_{d(off)}$	turn-off delay time			-	10.1	-	ns
t_f	fall time			-	7.8	-	ns
Source-drain diode FET1 and FET2							
V_{SD}	source-drain voltage	I_S = 10 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 12		-	0.81	1	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C		-	21.5	-	ns
Q_r	recovered charge		[1]	-	16.2	-	nC

[1] Includes capacitive recovery



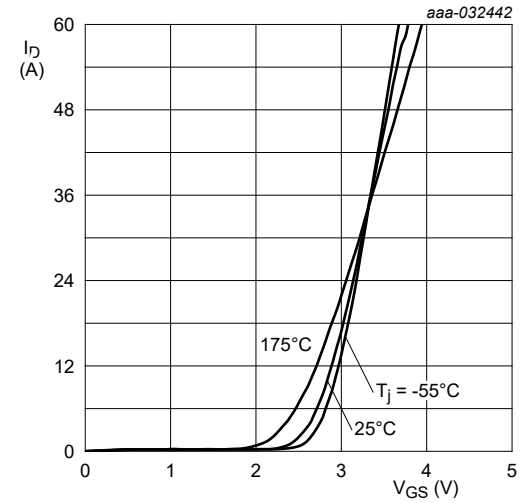
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2



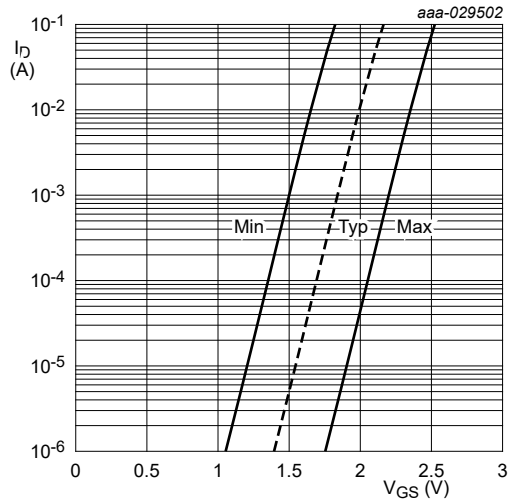
T_j = 25 °C; I_D = 10 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values. FET1 and FET2



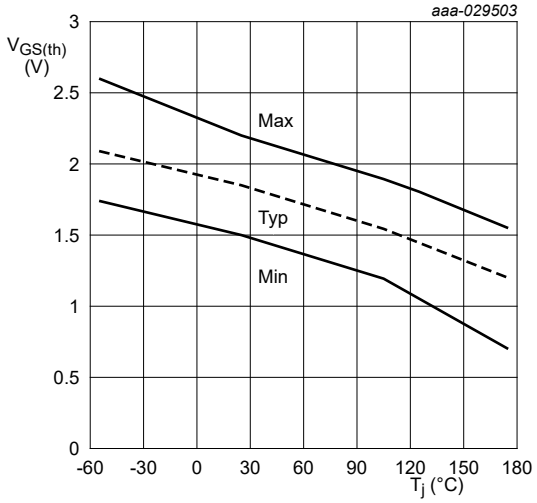
V_{DS} = 8 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2



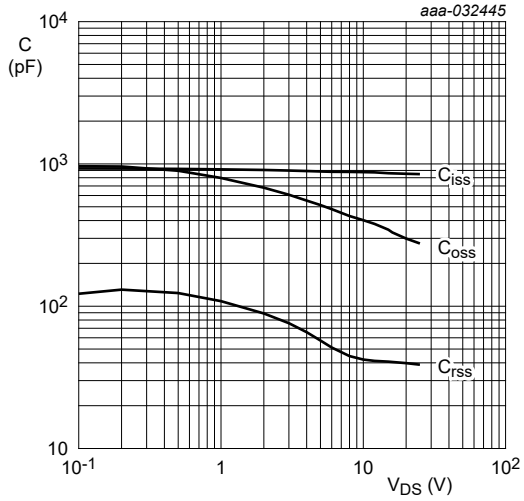
T_j = 25 °C; V_{DS} = 5 V

Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2



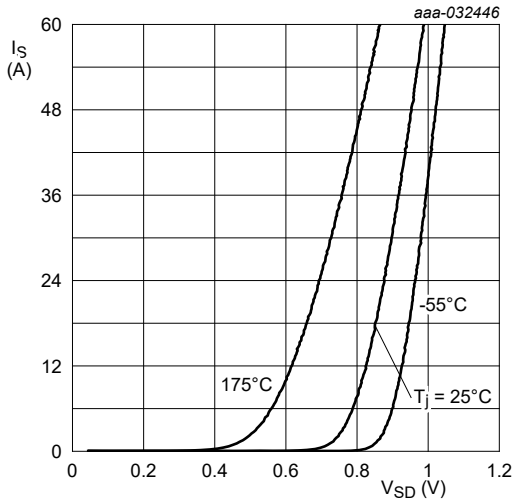
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2



V_{GS} = 0 V; f = 1 MHz

Fig. 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

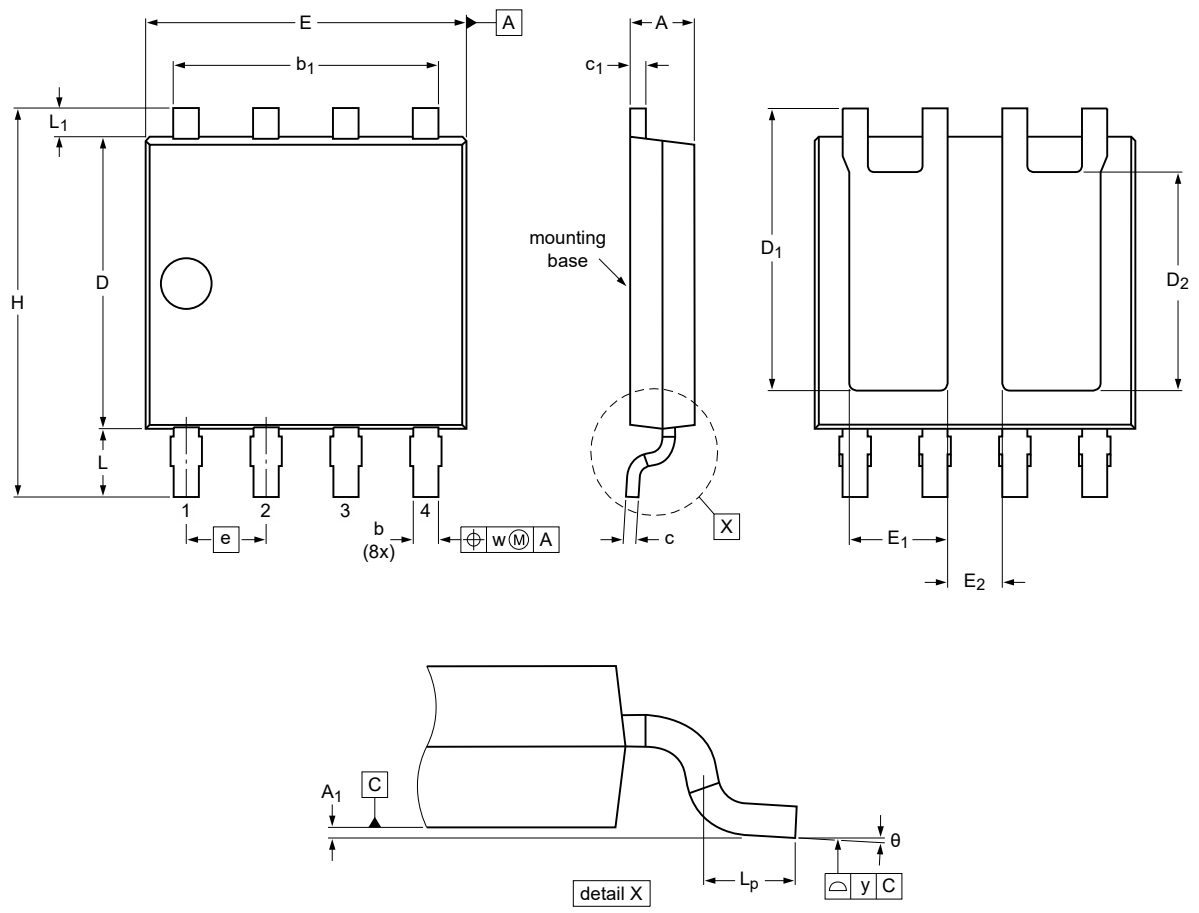


V_{GS} = 0 V

Fig. 12. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values FET1 and FET2

11. Package outline

Plastic single ended surface mounted package LFPAK56D; 8 leads **SOT1205**



Dimensions

Unit		A	A_1	b	b_1	c	c_1	$D^{(1)}$	$D_1{}^{(1)}$	D_2 (ref)	$E^{(1)}$	$E_1{}^{(1)}$	E_2	e	H	L	L_1	L_p	w	y	θ
mm	max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.55	3.5	5.30	1.8	0.85		6.2	1.3	0.55	0.85			8°
	nom													1.27					0.25	0.1	
	min	1.02	0.0	0.35	4.1	0.19	0.24	4.45	4.35	3.4	4.95	1.6	0.60		5.9	0.8	0.30	0.40			0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1205						~~14-08-21~~ 14-10-28

Fig. 13. Package outline LFPAK56D; Dual LFPAK (SOT1205)

12. Soldering

Footprint information for reflow soldering of LFPAK56D package **SOT1205**

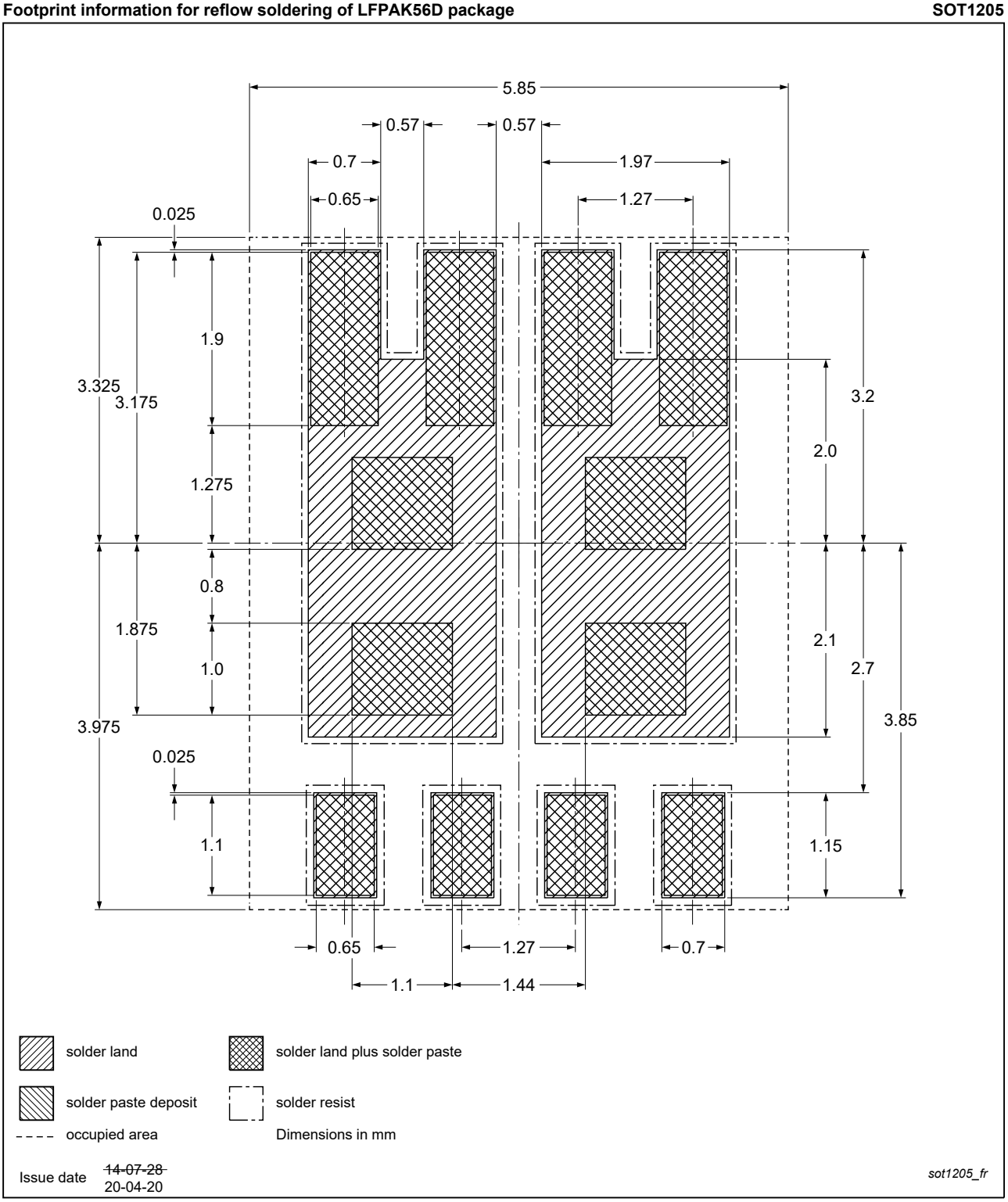


Fig. 14. Reflow soldering footprint for LFPAK56D; Dual LFPAK (SOT1205)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 26 September 2022