TX 98-4

ASK Transmitter

Data Sheet

Revision 1.0, 2010-04-23

Wireless Sense & Control

Edition 2010-04-23

Published by
Infineon Technologies AG
81726 Munich, Germany

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TX 98-4 ASK Transmitter

Revision History: 2010-04-23, Revision 1.0

Previous Revision: none

Page	Subjects (major changes since last revision)

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Last Trademarks Update 2009-10-19

Table of Contents

1 Product Description

1.1 Overview

The TX 98-4 is a single chip ASK transmitter for operation in the frequency band from 433 to 435 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additional features are a power down mode and a divided clock output.

1.2 Features

- Frequency range 433 ... 435 MHz
- Low supply current
- Power down mode
- High efficiency power amplifier (typically 10 dBm)
- Fully integrated frequency synthesizer
- VCO without external components
- ASK modulation
- Voltage supply range 2.1... 4 V
- Low external component count
- Divided clock output for µC
- Temperature range -40... +85°C
- Crystal oscillator 13.56 MHz

1.3 Application

TX 98-4 is suitable for any kind of remote control system, especially for low data rate wireless applications where low current consumption is important and where the line-of-sight limitation is driving the infra-red to RF replacement.

Main applications:

- Home Automation
  - Lighting Control
  - Curtain, Roller Blind Control
  - Air Condition Control
- Garage Door Openers
- Wireless Toys
- Remote Keyless Entry Systems

TX 98-4 is defined and qualified to meet low-cost consumer product requirements.

1.4 Ordering Information

Table 1 Order Information

Type	Ordering Code	Package[1)]
TX 98-4	SP000743714	**PG-TSSOP-10**

1) *Available on tape and reel*

2 Functional Description

2.1 Pin Configuration

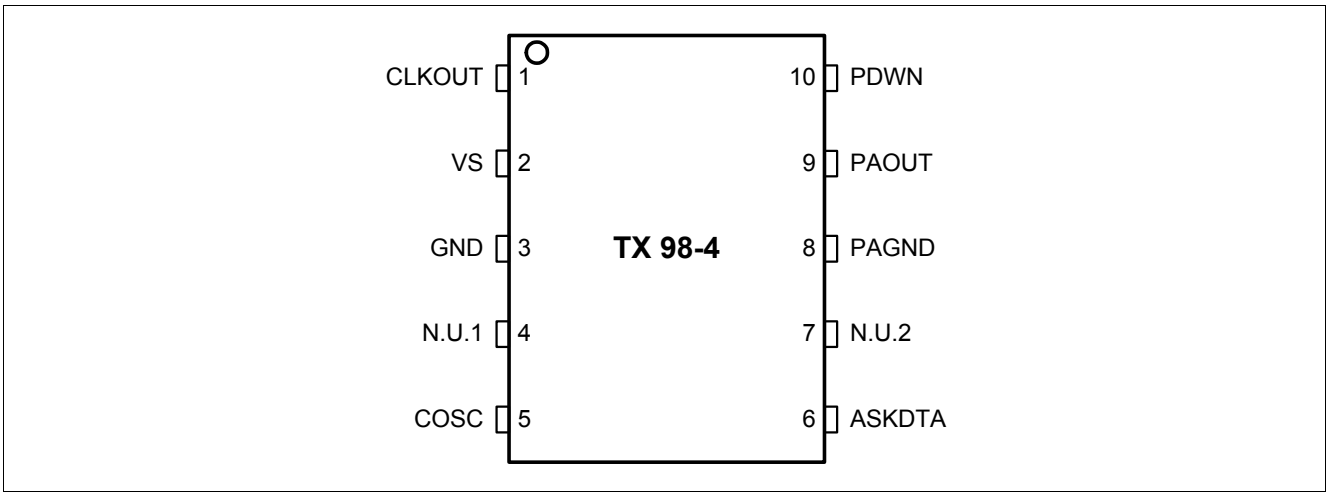


Figure 1 IC Pin Configuration

2.2 Pin Definition and Functions

Table 2 Pin Definition and Functions - Overview

Pin No.	Symbol	Function
1	CLKOUT	Clock Driver Output (847.5 kHz)
2	VS	Voltage Supply
3	GND	Ground
4	N.U.1	Not used 1
5	COSC	Crystal Oscillator Input (13.56 MHz)
6	ASKDTA	Amplitude Shift Keying Data Input
7	N.U.2	Not used 2
8	PAGND	Power Amplifier Ground
9	PAOUT	Power Amplifier Output (434 MHz)
10	PDWN	Power Down Mode Control

Table 3 Pin Definition and Function

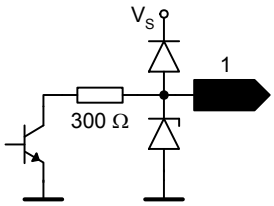
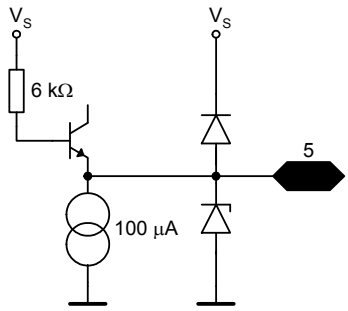
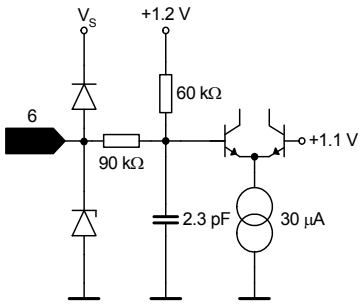
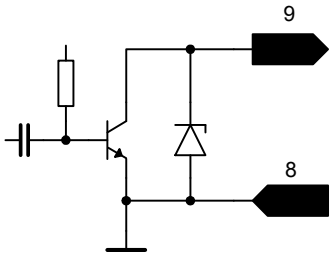
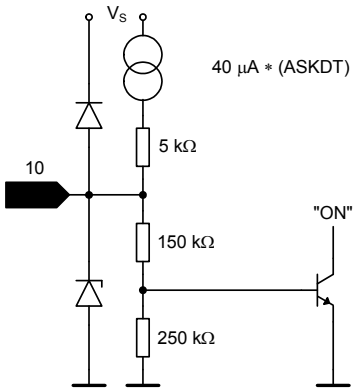
Ball No.	Name	Pin Type	Buffer Type	Function
1	CLKOUT			**Clock output to supply an external device** An external pull-up resistor has to be added in accordance to the driving requirements of the external device. The clock frequency is 847.5 kHz.
2	VS			**This pin is the positive supply of the transmitter electronics** An RF bypass capacitor should be connected directly to this pin and returned to GND (pin 3) as short as possible.
3	GND			**General ground connection**
4	N.U.1			**This pin must be left open**
5	COSC			**This pin is connected to the reference oscillator circuit** The reference oscillator is working as a negative impedance converter. It presents a negative resistance in series to an inductance at the COSC pin.
6	ASKDTA			**Digital amplitude modulation can be imparted to the Power Amplifier through this pin** A logic high (ASKDTA > 1.5 V or open) enables the Power Amplifier. A logic low (ASKDTA < 0.5 V) disables the Power Amplifier.
7	N.U.2			**This pin must be left open**

Table 3 Pin Definition and Function (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
8	PAGND			**Ground connection of the power amplifier** The RF ground return path of the power amplifier output PAOUT (pin 9) has to be concentrated to this pin.
9	PAOUT			**RF output pin of the transmitter** A DC path to the positive supply VS has to be supplied by the antenna matching network.
10	PDWN			**Disable pin for the complete transmitter circuit** A logic low (PDWN < 0.7 V) turns off all transmitter functions. A logic high (PDWN > 1.5 V) gives access to all transmitter functions.

2.3 Functional Block Diagram

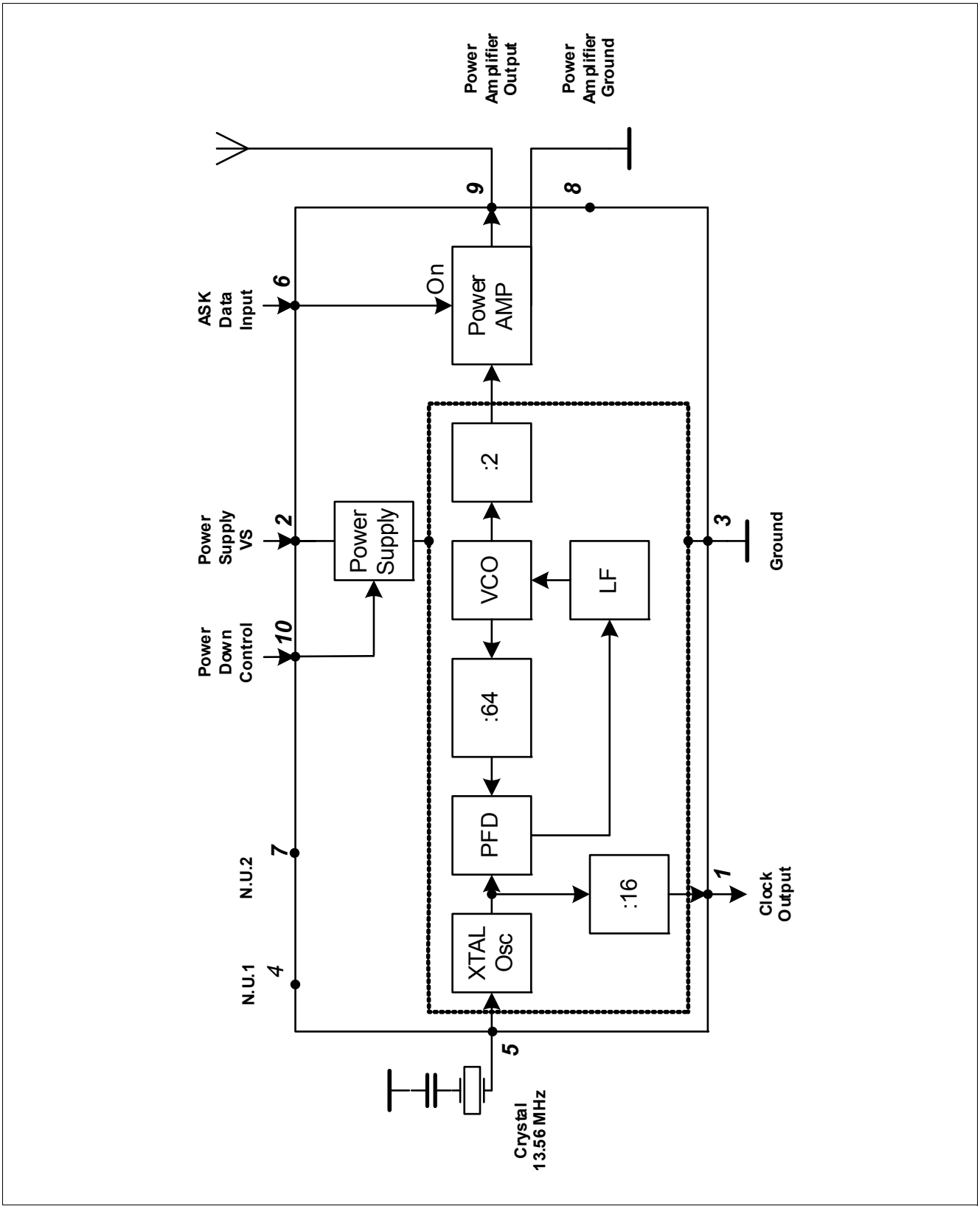


Figure 2 Functional Block Diagram

2.4 Functional Block Description

2.4.1 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a Voltage Controlled Oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter. It is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 868 MHz. The oscillator signal is fed both, to the synthesizer divider chain and (via 1:2 divider) to the power amplifier. The overall division ratio of the asynchronous divider chain is 64. The phase detector is a Type IV PD with charge pump. The passive loop filter is realized on chip.

2.4.2 Crystal Oscillator

The crystal oscillator operates at 13.56 MHz.

The crystal frequency is divided by 16. The resulting 847.5 kHz are available at the clock output CLKOUT (pin1) to drive the clock input of a micro controller.

2.4.3 Power Amplifier

The VCO frequency is divided by 2 and fed to the Power Amplifier.

The Power Amplifier can be switched on and off by the signal at ASKDTA (pin 6).

Table 4 ASKDTA - Power Amplifier

ASKDTA (pin6)	Power Amplifier
Low[1)]	OFF
Open[2)], High[3)]	ON

1) Low: Voltage at pin < 0.5 V

2) Open: Pin open

3) High: Voltage at pin > 1.5 V

The Power Amplifier has an Open Collector output at PAOUT (pin 9) and requires an external pull-up coil to provide bias. The coil is part of the tuning and matching LC circuitry to get best performance with the external loop antenna. To achieve the best power amplifier efficiency, the high frequency voltage swing at PAOUT (pin 9) should be twice the supply voltage.

The power amplifier has its own ground pin PAGND (pin 8) in order to reduce the amount of coupling to the other circuits.

2.4.4 Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE.

2.4.4.1 Power Down Mode

In the POWER DOWN MODE the complete chip is switched off.

The current consumption is typically 0.3 nA @ 3 V and 25°C.

This current doubles every 8°C. The values for higher temperatures is typically 14 nA @ 85°C.

2.4.4.2 PLL Enable Mode

In the PLL ENABLE MODE the PLL is switched on but the power amplifier is turned off to avoid undesired power radiation during the time the PLL needs to settle. The turn on time of the PLL is determined mainly by the turn on time of the crystal oscillator and is less than 1 msec when the specified crystal is used.

The current consumption is typically 4mA.

2.4.4.3 Transmit Mode

In the TRANSMIT MODE the PLL is switched on and the power amplifier is turned on too.

The current consumption of the IC is typically 14.2 mA when using a proper transforming network at PAOUT, see **Figure 3**.

2.4.4.4 Power mode control

The bias circuitry is powered up via a voltage V > 1.5 V at the pin PDWN (pin10).

When the bias circuitry is powered up, the pin ASKDTA is pulled up internally.

Forcing the voltage at the pins low overrides the internally set state.

The principle schematic of the power mode control circuitry is shown in **Figure 3**

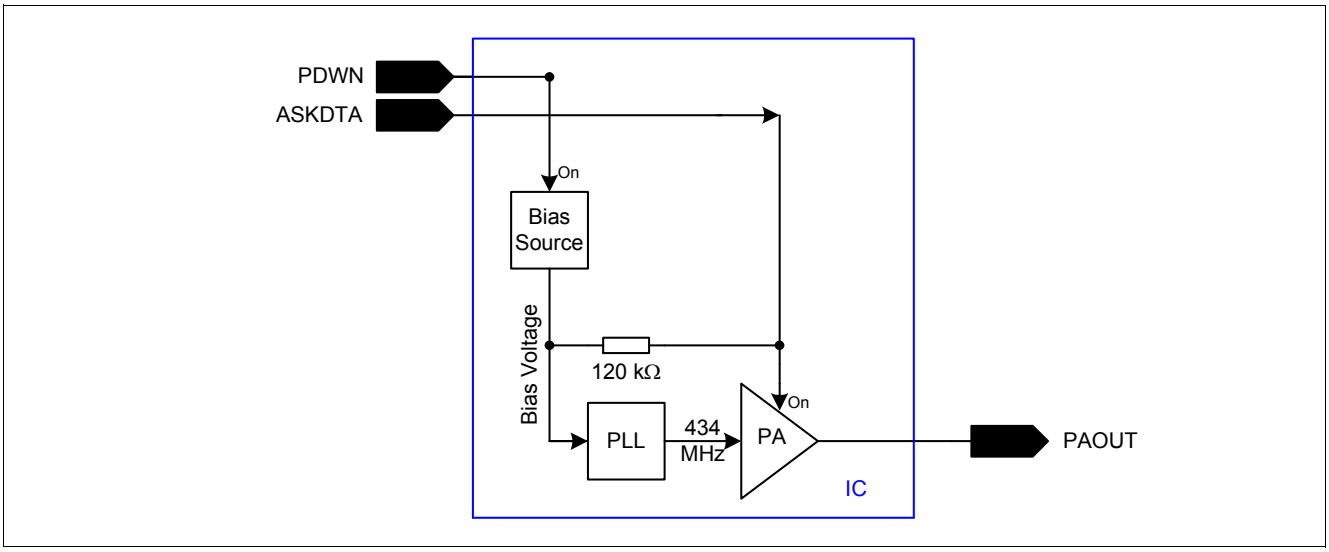


Figure 3 Power mode control circuitry

Table 5 provides a listing of how to get into the different power modes

Table 5 Power Modes

PDWN	ASKDTA	MODE
Low[1)]	Low, Open	POWER DOWN
Open[2)]	Low	POWER DOWN
High[3)]	Low	PLL ENABLE
Open	High	TRANSMIT
High	Open, High	TRANSMIT

1) Low: Voltage at pin < 0.7 V (PDWN), Voltage at pin < 0.5 V (ASKDTA)
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

Other combinations of the control pins PDWN and ASKDTA are not recommended.

To avoid spurious radiation it is strongly recommended to switch not directly from PDWN-mode to TRANSMIT-mode, but to PLL-ENABLE-mode first!

2.4.5 Recommended Timing Diagrams for ASK-Modulation

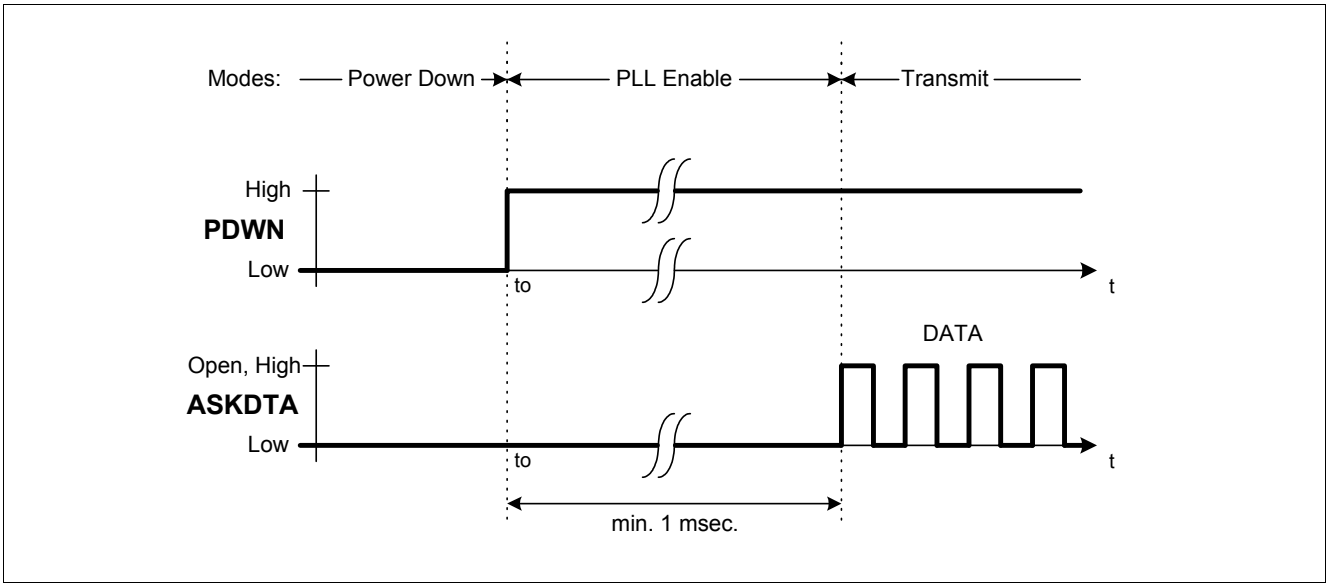


Figure 4 ASK Modulation

3 Application

3.1 Application Hints on the Crystal Oscillator

The crystal oscillator achieves a turn on time less than 1 msec when the specified crystal is used. To achieve this, a NIC oscillator type is implemented in the TX 98-4. The input impedance of this oscillator is a negative resistance in series to an inductance. Therefore the load capacitance of the crystal CL (specified by the crystal supplier) is transformed to the capacitance Cv.

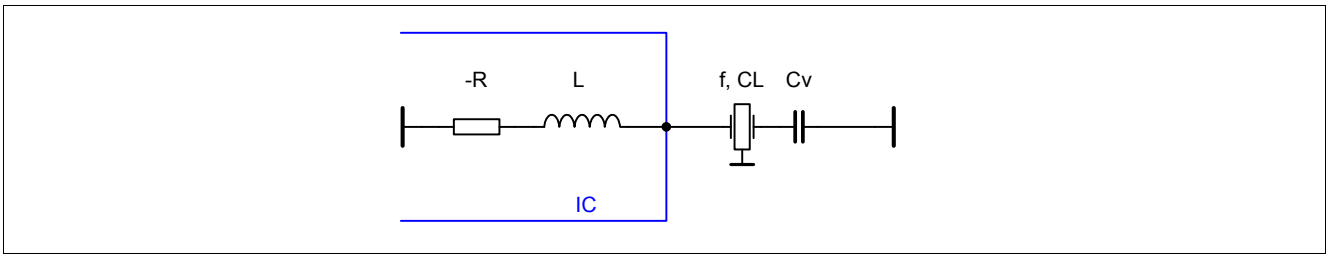


Figure 5 Application Hints

$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L} \tag{1}$$

CL Crystal load capacitance for nominal frequency

ω Angular frequency

L Inductance of the crystal oscillator

Example

The inductance L at 13.56 MHz is about 4.6 µH. Assuming a crystal frequency of 13.56 MHz and a crystal load capacitance of CL = 12 pF, the value of Cv is calculated to ~ 8,6 pF.

$$C\,v \;=\; \frac{1}{\frac{1}{C\,L} + \;\omega\;^{2}\,L} \tag{2}$$

3.2 Design Hints on the Clock Output (CLKOUT)

The CLKOUT pin is an open collector output. An external pull up resistor (RL) should be connected between this pin and the positive supply voltage. The value of RL is depending on the clock frequency and the load capacitance CLD (PCB board plus input capacitance of the micro controller). RL can be calculated to:

$$RL = \frac{1}{fCLKOUT * 8 * CLD} \tag{3}$$

Table 6 Clock Output fCLKOUT=847.5 kHz

CL[pF]	RL[kOhm]
5	27
10	12
20	6.8

Note: To achieve a low current consumption and a low spurious radiation, the largest possible RL should be chosen.

Even harmonics of the signal at CLKOUT can interact with the crystal oscillator input COSC preventing the start-up of oscillation. Care must be taken in layout by sufficient separation of the signal lines to ensure sufficiently small coupling.

3.3 Application Hints on the Power-Amplifier

The power amplifier operates in a high efficient class C mode. This mode is characterized by a pulsed operation of the power amplifier transistor at a current flow angle of Θ<<π. A frequency selective network at the amplifier output passes the fundamental frequency component of the pulse spectrum of the collector current to the load. The load and its resonance transformation to the collector of the power amplifier can be generalized by the equivalent circuit of **Figure 6**. The tank circuit L//C//RL in parallel to the output impedance of the transistor should be in resonance at the operating frequency of the transmitter.

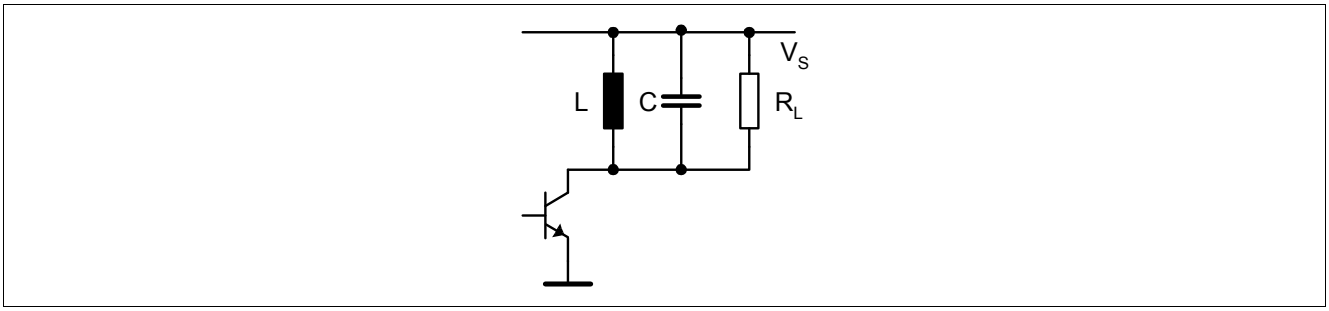


Figure 6 Equivalent power amplifier tank circuit

The optimum load at the collector of the power amplifier for “critical” operation under idealized conditions at resonance is:

$$R_{LC} = \frac{V_S^2}{2 * P_O} \tag{4}$$

The theoretical value of R_{LC} for an RF output power of P_o= 10 dBm (10 mW) is:

$$R_{LC} = \frac{3^2}{2 * 0.01} = 450\Omega \tag{5}$$

“Critical” operation is characterized by the RF peak voltage swing at the collector of the PA transistor to just reach the supply voltage V_S.

The high degree of efficiency under “critical” operating conditions can be explained by the low power losses at the transistor. During the conducting phase of the transistor, its collector voltage is very small. This way the power loss of the transistor, equal to $i_C * u_{CE}$ is minimized. This is particularly true for small current flow angles of Θ<<π.
In practice the RF-saturation voltage of the PA transistor and other parasitic’s reduce the “critical” R_{LC}.

The output power P_o is reduced by operating in an “overcritical” mode characterized by $R_L > R_{LC}$.
The power efficiency (and the bandwidth) increase when operating at a slightly higher R_L, as shown in **Figure 7**.
The collector efficiency E is defined as:

$$E = \frac{P_O}{V_S I_C} \tag{6}$$

The diagram of Figure 7 was measured directly at the PA-output at V_S = 3 V. Losses in the matching circuitry decrease the output power by about 1.5 dB. As can be seen from the diagram, 250 Ω is the optimum impedance for operation at 3 V. For an approximation of R_{OPT} and P_{OUT} at other supply voltages those two formulas can be used:

$$R_{OPT} \sim V_S \tag{7}$$

and

$$P_{OUT} \sim R_{OPT} \tag{8}$$

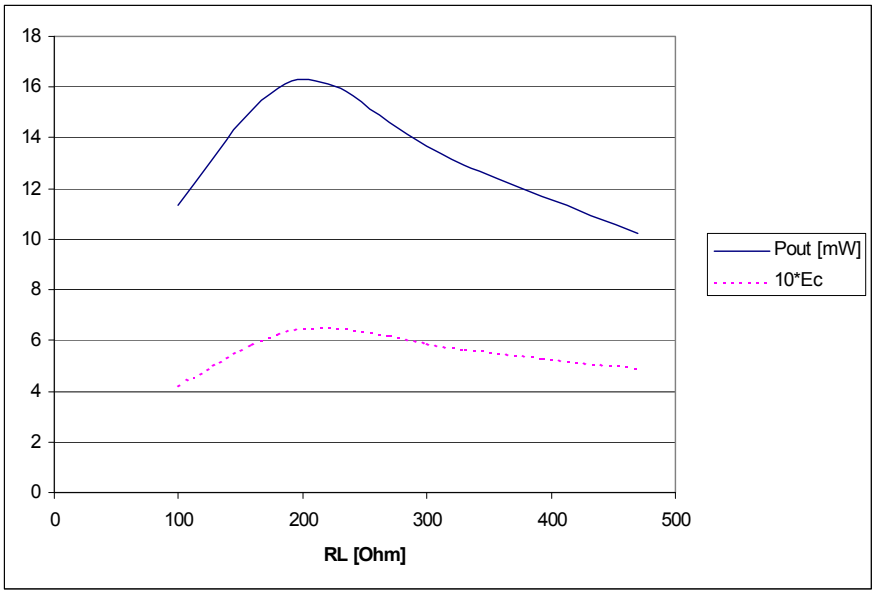


Figure 7 Output power P_o (mW) and collector efficiency E vs. load resistor R_L

The DC collector current I_c of the power amplifier and the RF output power P_o vary with the load resistor R_L. This is typical for overcritical operation of class C amplifiers. The collector current will show a characteristic dip at the resonance frequency for this type of “overcritical” operation. The depth of this dip will increase with higher values of R_L.

4 Reference

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irrevisible damage to the integrated circuit.

Table 7 Absolute Maximum Ratings, T_{amb} = -40°C … +85°C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction Temperature	T_J	-40		+125	°C	
Storage Temperature	T_s	-40		+150	°C	
Thermal Resistance	R_{thJA}			220	K/W	
Supply voltage	V_S	-0.3		+4.0	V	
Voltage at any pin excluding pin 9	V_{pins}	-0.3		V_S + 0.3	V	
Voltage at pin 9	V_{pin9}	-0.3		2 * V_S	V	No ESD-Diode to V_S
ESD integrity, all pins	V_{ESD}	-1		+1	kV	JEDEC Standard JESD22-A114-B
ESD integrity, all pins excluding pin 9	V_{ESD}	-2.5		+2.5	kV	JEDEC Standard JESD22-A114-B

Note: All voltages referred to ground (pins) unless stated otherwise. Pins 3 and 8 are grounded.

4.2 Operating Ratings

Within the operational range the IC operates as described in the circuit description.

Table 8 Operating Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_S	2.1		4.0	V	
Ambient temperature	T_A	-40		85	°C	

4.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature. Typical characteristics are the median of the production. The device parameters are either verified by design and/or characterization or by production test.

4.3.1 AC/DC Characteristic at 3 V, 25°C

Table 9 Supply Voltage V_S=3V, Ambient temperature T_{amb}=25°C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Current consumption						
Power Down mode	$I_{S\ PDWN}$		0.3	100	nA	V (Pins 10, 6 and 7) < 0.2 V
PLL Enable mode	$I_{S\ PLL\_EN}$		4	5.5	mA	
Transmit mode 434 MHz	$I_{S\ TRANSM}$		14.2	18	mA	
Output frequency						
Output frequency	f_{OUT}	427	434.5	442	MHz	f_{OUT} = 32 * f_{COSC}
Clock Driver Output (Pin 1)						
Output current (High)	I_{CLKOUT}			5	µA	V_{CLKOUT} = V_S
Saturation Voltage (Low)[1]	V_{SATL}			0.56	V	I_{CLKOUT} = 1 mA
Crystal Oscillator Input (Pin 5)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	Ω	f = 13.56 MHz
Input inductance of the COSC pin			4.6		µH	f = 13.56 MHz
ASK Modulation Data Input (Pin 6)						
ASK Transmit disabled	V_{ASKDTA}	0		0.5	V	
ASK Transmit enabled	V_{ASKDTA}	1.5		VS	V	
Input bias current ASKDTA	I_{ASKDTA}			30	µA	V_{ASKDTA} = V_S
Input bias current ASKDTA	I_{ASKDTA}	-20			µA	V_{ASKDTA} = 0 V
ASK data rate	f_{ASKDTA}			20	kHz	
Power Amplifier Output (Pin 9)						
Output Power[2] at 434 MHz transformed to 50 Ohm	P_{OUT434}	7	10	13	dBm	
Power Down Mode Control (Pin 10)						
Power Down mode	V_{PDWN}	0		0.7	V	V_{ASKDTA} < 0.2 V
PLL Enable mode	V_{PDWN}	1.5		VS	V	V_{ASKDTA} < 0.5 V
Transmit mode	V_{PDWN}	1.5		VS	V	V_{ASKDTA} > 1.5 V
Input bias current PDWN	I_{PDWN}			30	µA	V_{PDWN} = V_S

1) Derating linearly to a saturation voltage of max. 140 mV at ICLKOUT = 0 mA

2) Power amplifier in overcritical C-operation. Matching circuitry as used in the 50 Ohm-Output Test board at the specified frequency. Tolerances of the passive elements not taken into account.

5 Package Outlines

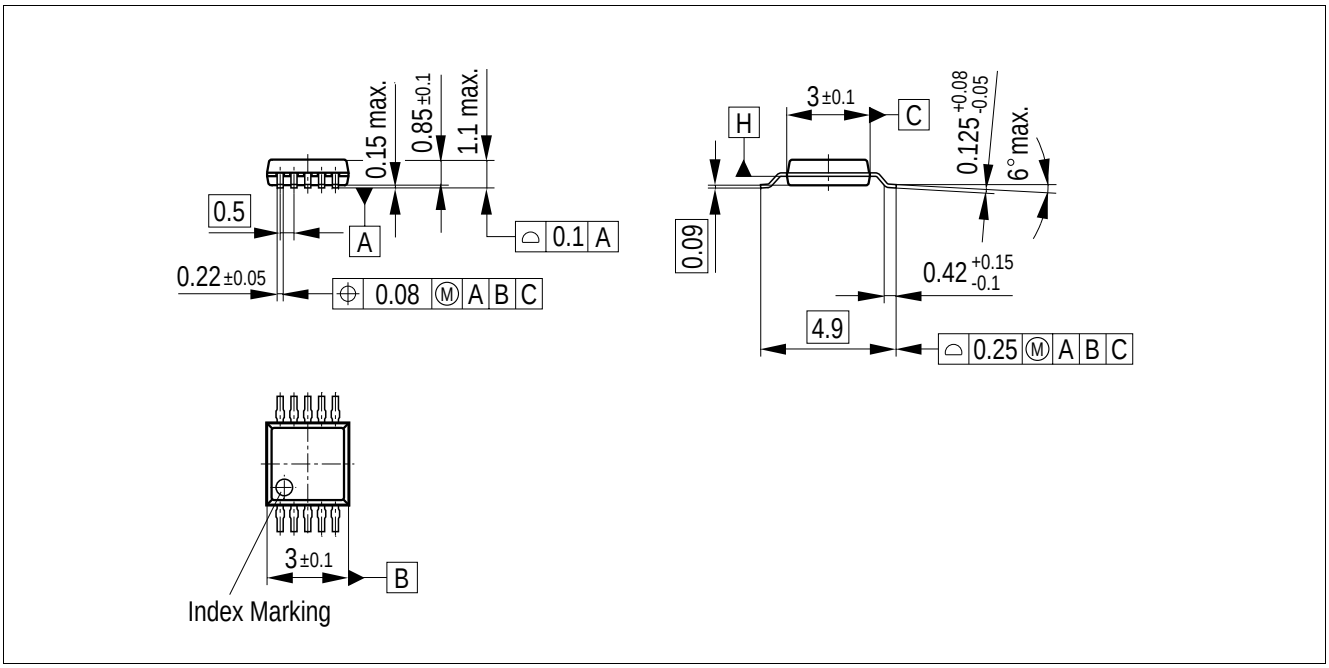


Figure 8 PG-TSSOP-10

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.*
2. *SMD = Surface Mounted Devic*

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