



Product Change Notification / SYST-17UVLR884

Date:

20-Dec-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

Data Sheet - ATtiny1624/1626/1627 Data Sheet Document Revision

Affected CPNs:

[SYST-17UVLR884_Affected_CPN_12202021.pdf](#)

[SYST-17UVLR884_Affected_CPN_12202021.csv](#)

Notification Text:

SYST-17UVLR884

Microchip has released a new Product Documents for the ATtiny1624/1626/1627 Data Sheet of devices. If you are using one of these devices please read the document located at [ATtiny1624/1626/1627 Data Sheet](#).

Notification Status: Final

Description of Change:

Document

- Data sheet status changed to "Completed": final limits added to the Electrical Characteristics, Typical Characteristics expanded, and package top markings added
- Number of available AC input pins corrected for ATtiny1624, ATtiny1626 in Table 2. Peripheral Overview
- Editorial updates throughout the document

CPU

- RAMPZ description updated
- EICALL not present/required in the tiny 2-family Fuses Reserved bits are written to '1', so the factory default values are:
 - OSCCFG: 0x7E
 - SYSCFG0: 0xF6
 - SYSCFG1: 0xFF

NVMCTRL

- Table 10-1. Setting Up Flash Sections: When BOOTEND = 0, the value of APPEND is ignored, and the entire Flash is BOOT section.
- Register CTRLB has Configuration Change Protection

RSTCTRL

Figures and timing diagrams improved:

- Block Diagram: improved
- MCU Start-Up
- Brown-Out Detector Reset
- Software Reset

CPUINT

Description of the IVSEL bit in the CTRLA register improved: When the entire Flash is configured as BOOT section, the IVSEL bit in the CTRLA register is ignored.

PORT

Slew rate limitation functionality added: Slew Rate Limit Enable (SLR) bit in the Port Control (PORTCTRL) register.

TCA

- Split mode interrupts added to Interrupt Vector Table
- Timing diagram for Split mode added
- Block diagram: The path from CNT register to CMPnBUF register removed
- In TCA Frequency mode, the timer frequency is controlled by CMP0, not CMPn

TCB

- 32-bit input capture is working for all input capture modes
- In Single-Shot mode, when the EDGE bit in the EVCTRL register is '1', both positive and negative edges will start the counter

RTC

It is no longer required to check the Synchronization Busy bits in the STATUS and PITSTATUS registers after startup

USART

- Description of the TX buffer added
- Description of the IREI bit in the EVCTRL register corrected

TWI

- FLUSH and BUSSTATE description updated
- CTRLA.SDASETUP is used in client mode to select the clock hold time to ensure minimum setup time

ADC

- Description of COMMAND.START bit field improved
- PGA initialization time is 20 μ s
- Group configuration names aligned with header files for PGACTRL.PGABIASSEL and MUXNEG.MUXNEG

UPDI

Value of STATUSA.UPDIREV corrected to '0100'

Electrical Characteristics

- Table 33-5: Typical values altered and min./max. values added
- Table 33-6: Completed
- Table 33-7: ADC updated
- Table 33-12: Note added
- Table 33-13: Note added
- Table 33-22: Symbol column updated
- Table 33-23: Value set reduced and updated
- ADC Table 33-26: values updated
- ADC Table 33-27: Values updated
- ADC Table 33-28: Values updated
- TEMPSENSE Table 33-29: Accuracy value updated
- 33.18. AC: Typical values altered and min./max. values added in all tables Typical Characteristics Plots added

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 20 Dec 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[ATtiny1624/1626/1627 Data Sheet](#)

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Affected Catalog Part Numbers (CPN)

ATTINY1624-SSF
ATTINY1624-SSFR
ATTINY1624-SSU
ATTINY1624-SSUR
ATTINY1624-XF
ATTINY1624-XFR
ATTINY1624-XU
ATTINY1624-XUR
ATTINY1626-MF
ATTINY1626-MFR
ATTINY1626-MU
ATTINY1626-MUR
ATTINY1626-SF
ATTINY1626-SFR
ATTINY1626-SU
ATTINY1626-SUR
ATTINY1626-XF
ATTINY1626-XFR
ATTINY1626-XU
ATTINY1626-XUR
ATTINY1627-MF
ATTINY1627-MFR
ATTINY1627-MU
ATTINY1627-MUR