Silicon carbide Power MOSFET 650 V, 55 mΩ typ., 40 A in a PowerFLAT 8x8 HV package

PowerFLAT 8x8 HV

Drain(5)

Gate(1)

Driver source(2)

Power source(3, 4)

NG1DS2PS34D5
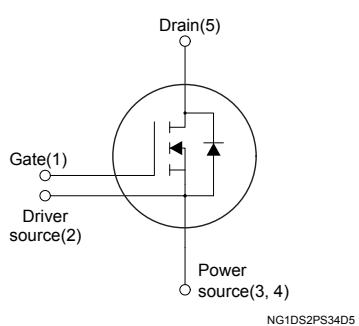
Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
SCTL35N65G2V	650 V	67 mΩ	40 A

- Very fast and robust intrinsic body diode
- Low capacitances
- Source sensing pin for increased efficiency

Applications

- Switching mode power supply
- DC-DC converters
- Industrial motor control

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2nd generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

STPOWER

Product status link
SCTL35N65G2V

Product summary	
Order code	SCTL35N65G2V
Marking	35N65G2V
Package	PowerFLAT 8x8 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operating range)	-5 to 20	
$I_D^{(1)}$	Drain current (continuous) at T_C = 25 °C	40	A
	Drain current (continuous) at T_C = 100 °C	40	
$I_{DM}^{(2)}$	Drain current (pulsed)	160	A
P_{TOT}	Total power dissipation at T_C = 25 °C	417	W
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		°C

1. *Value limited by package.*
2. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.36	°C/W
$R_{thJB}^{(1)}$	Thermal resistance, junction-to-board	45	°C/W

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			5	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = -10 to 22 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	1.8	3.2	5.0	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 20 V, I_D = 20 A		45	67	mΩ
		V_{GS} = 18 V, I_D = 20 A		55		
		V_{GS} = 20 V, I_D = 20 A, T_J = 175 °C		58		

Table 4. Dynamic, based on HiP247 package option

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 400 V, f = 1 MHz	-	1370	-	pF
C_{oss}	Output capacitance		-	125	-	pF
C_{rss}	Reverse transfer capacitance		-	30	-	pF
R_g	Gate input resistance	f = 1 MHz, I_D = 0 A	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 20 A, V_{GS} = 0 to 20 V	-	73	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	27	-	nC

Table 5. Switching energy (inductive load), based on HiP247 package option

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	V_{DD} = 400 V, I_D = 20 A,	-	100	-	µJ
E_{off}	Turn-off switching energy	R_G = 4.7 Ω, V_{GS} = -5 to 20 V	-	35	-	µJ

Table 6. Switching times, based on HiP247 package option

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 20 A,	-	16	-	ns
t_f	Fall time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time	R_G = 4.7 Ω, V_{GS} = -5 to 20 V	-	35	-	ns
t_r	Rise time		-	9	-	ns

Table 7. **Reverse diode characteristics, based on HiP247 package option**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	V_{GS} = 0 V, I_F = 20 A,	-	3.3	-	V
t_{rr}	Reverse recovery time		-	18	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 400 V, I_F = 20 A, di/dt = 1000 A/µs	-	85	-	nC
I_{RRM}	Reverse recovery current		-	7	-	A

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area
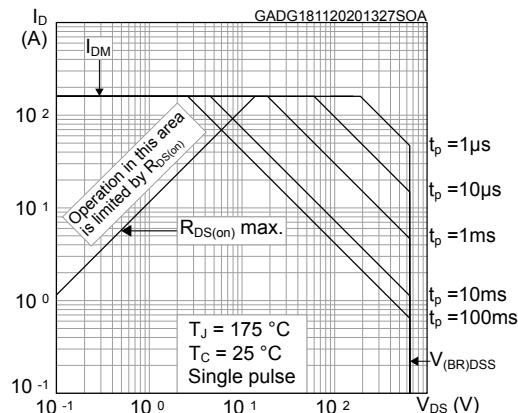
Figure 2. Thermal impedance
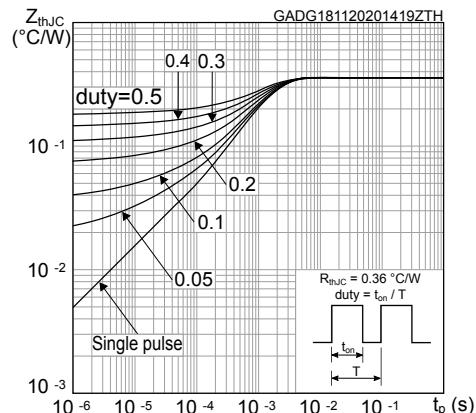
Figure 3. Output characteristics (T_J = 25 °C), based on HiP247 package option
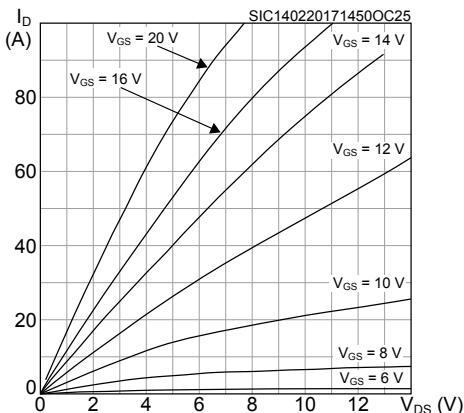
Figure 4. Output characteristics (T_J = 175 °C), based on HiP247 package option
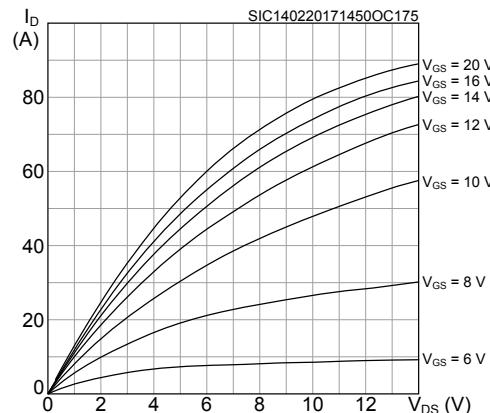
**Figure 5. Transfer characteristics, based on HiP247 package option**
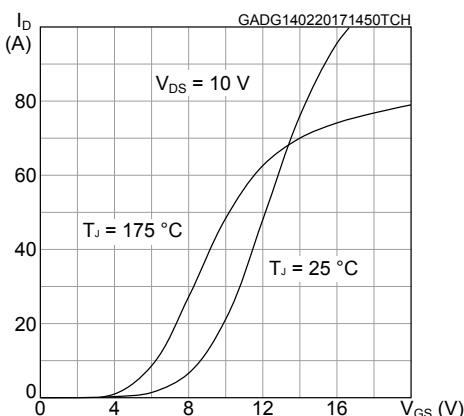
**Figure 6. Gate charge vs gate-source voltage, based on HiP247 package option**
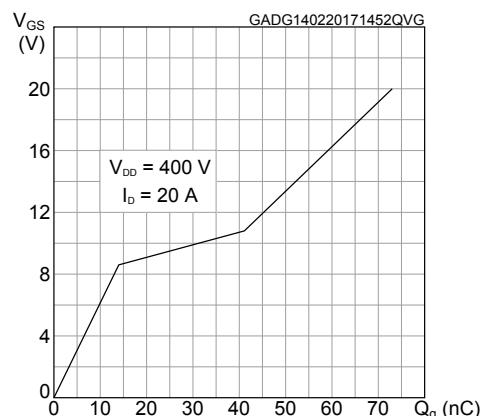
**Figure 7. Capacitance variations, based on HiP247 package option**

GADG140220171452CVR

C (pF)

C_{ISS}

C_{OSS}

C_{RSS}

f = 1 MHz

10^3

10^2

10^1

10^{-1} 10^0 10^1 10^2 V_{DS} (V)
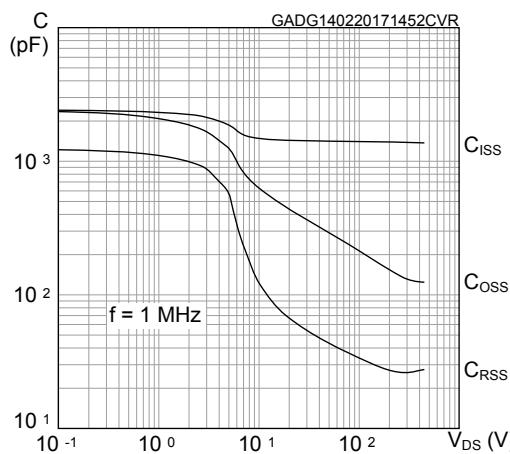
Figure 8. Switching energy vs drain current, based on HiP247 package option

SIC140220171454SLC

E (µJ)

V_{DD} = 400 V,
R_G = 4.7 Ω,
V_{GS} = -5 to 20 V

E_{tot}

E_{on}

E_{off}

1000

800

600

400

200

0

0 20 40 60 I_D (A)
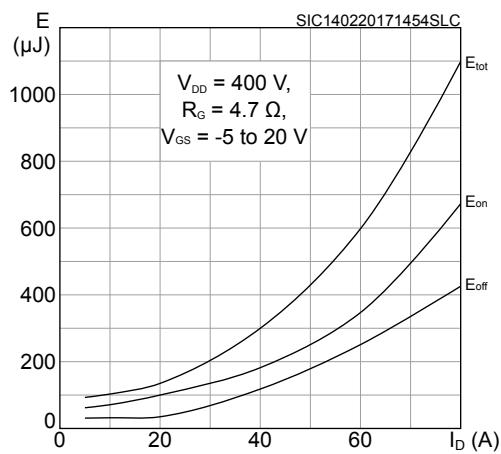
Figure 9. Switching energy vs junction temperature, based on HiP247 package option

SIC140220171455SLT

E (µJ)

140

120

100

80

60

40

20

0

E_{tot}

E_{on}

V_{DD} = 400 V, R_G = 4.7 Ω,
I_D = 20 A, V_{GS} = -5 to 20 V

E_{off}

0 50 100 150 T_J (°C)
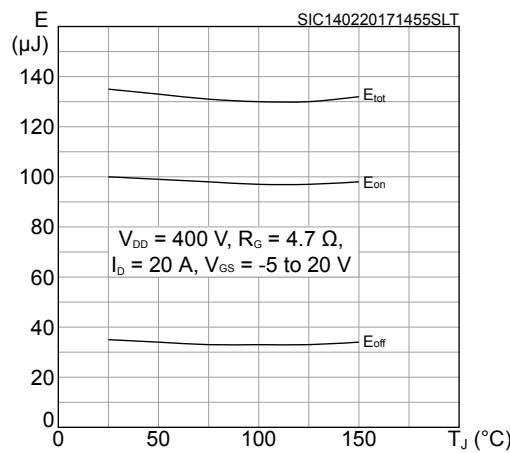
Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

$V_{(BR)DSS}$ (norm.)

GADG140220171455BDV

I_D = 1 mA

1.06

1.04

1.02

1.00

0.98

0.96

0.94

-75 -25 25 75 125 175 T_J (°C)
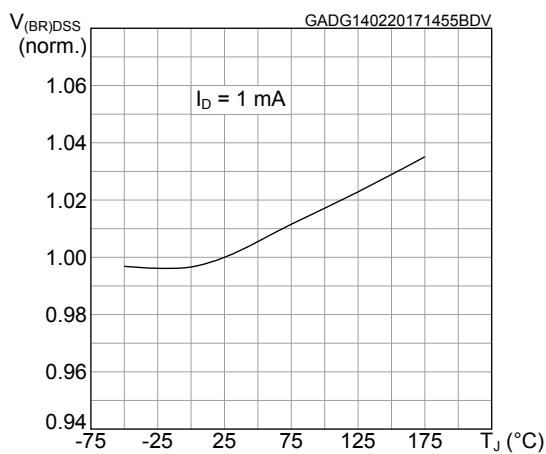
Figure 11. Normalized gate threshold voltage vs temperature

$V_{GS(th)}$ (norm.)

GADG140220171458VTH

I_D = 1 mA

1.4

1.2

1.0

0.8

0.6

0.4

-75 -25 25 75 125 175 T_J (°C)
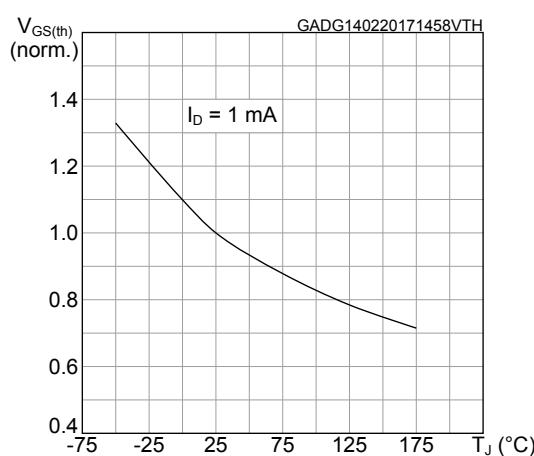
Figure 12. Normalized on-resistance vs temperature

$R_{DS(on)}$ (norm.)

GADG140220171458RON

V_{GS} = 20 V

2.0

1.5

1.0

0.5

0.0

-75 -25 25 75 125 175 T_J (°C)
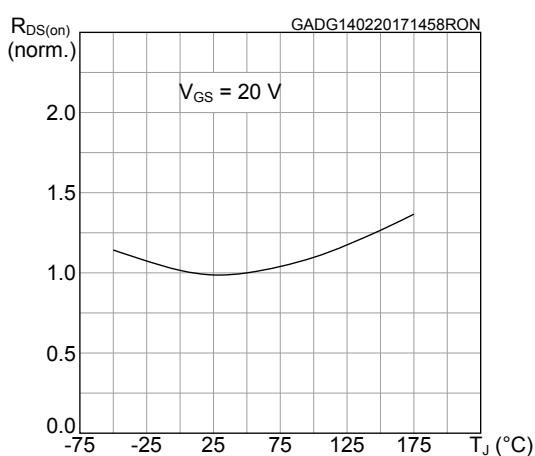
Figure 13. Reverse conduction characteristics (T$_J$ = 25 °C), based on HiP247 package option
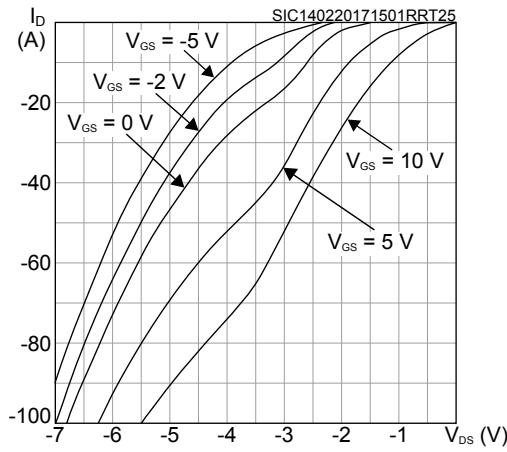
**Figure 14. Reverse conduction characteristics (T$_J$ = 175 °C), based on HiP247 package option**
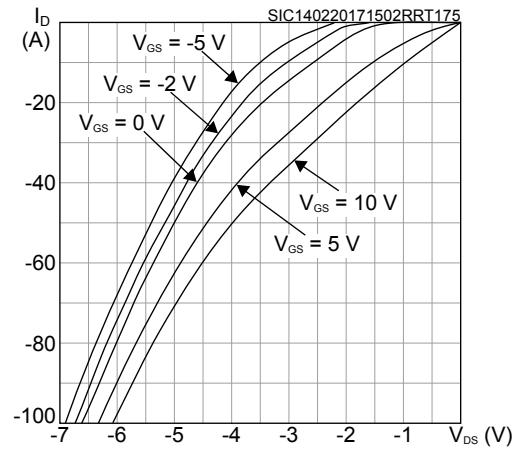
3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 PowerFLAT 8x8 HV type A package information

Figure 15. **PowerFLAT 8x8 HV type A package outline**
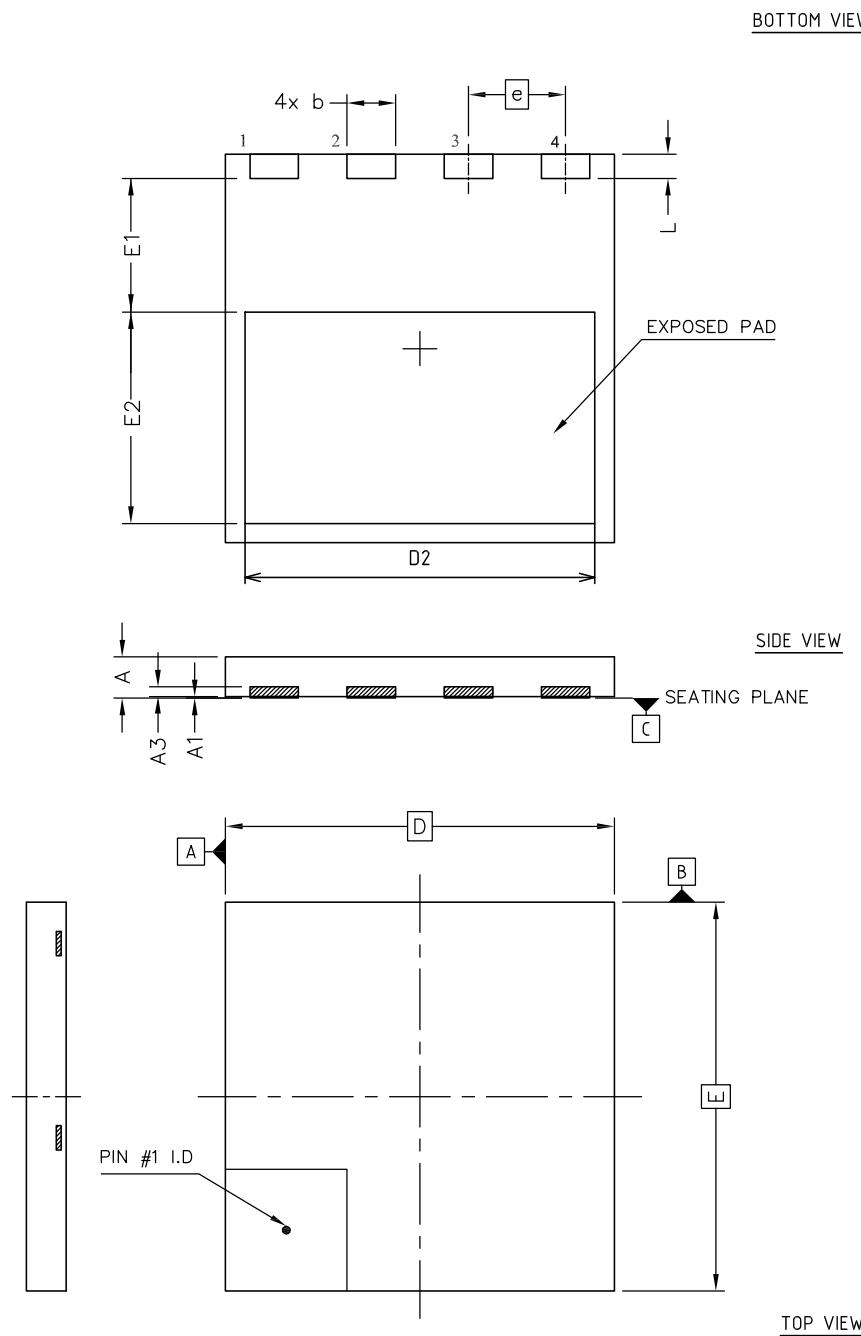
8222871_Rev_4

Table 8. PowerFLAT 8x8 HV type A mechanical data

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e	2.00 BSC		
L	0.40	0.50	0.60

Figure 16. PowerFLAT 8x8 HV footprint
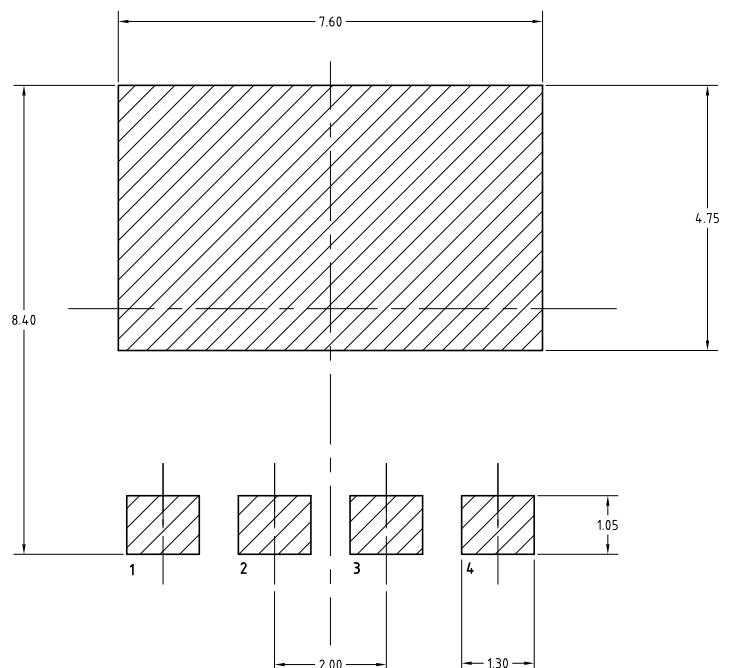

8222871_REV_4_footprint

Note: *All dimensions are in millimeters.*

## 3.2 PowerFLAT 8x8 HV packing information

Figure 17. PowerFLAT 8x8 HV tape

8229819_Tape_revA
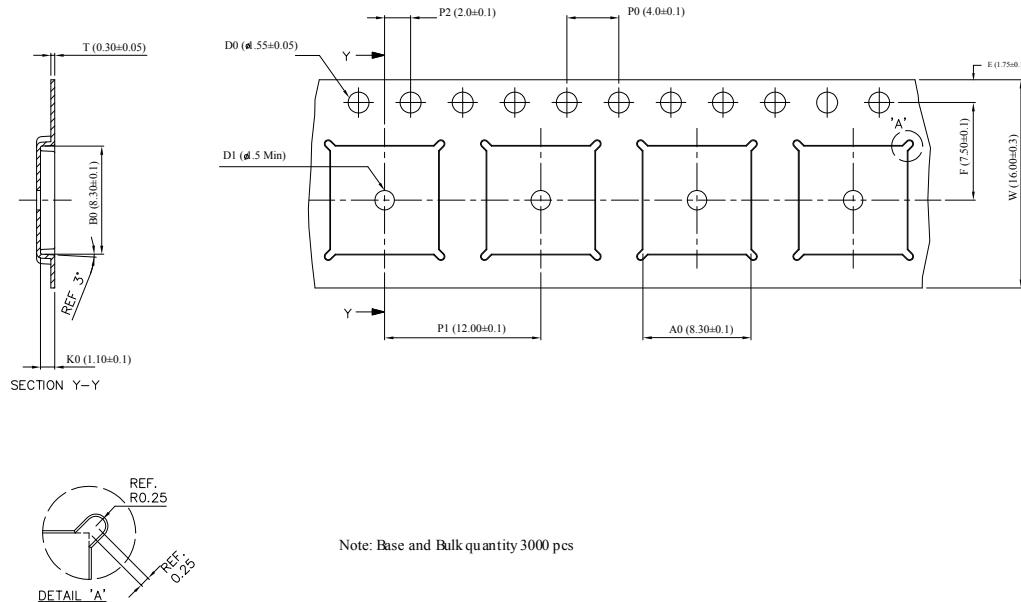
Note: *All dimensions are in millimeters.*

Figure 18. PowerFLAT 8x8 HV package orientation in carrier tape
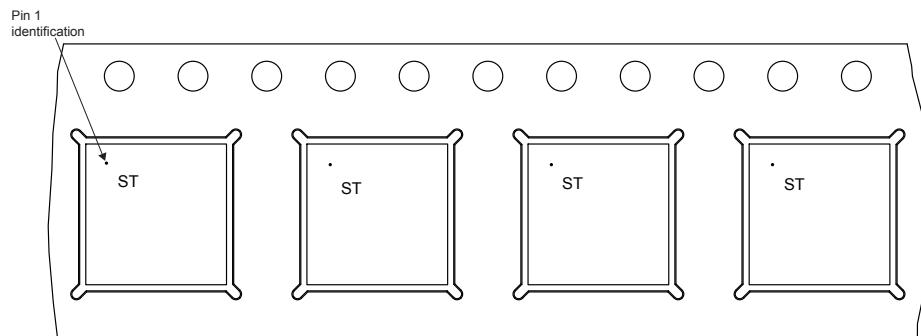
Figure 19. PowerFLAT 8x8 HV reel
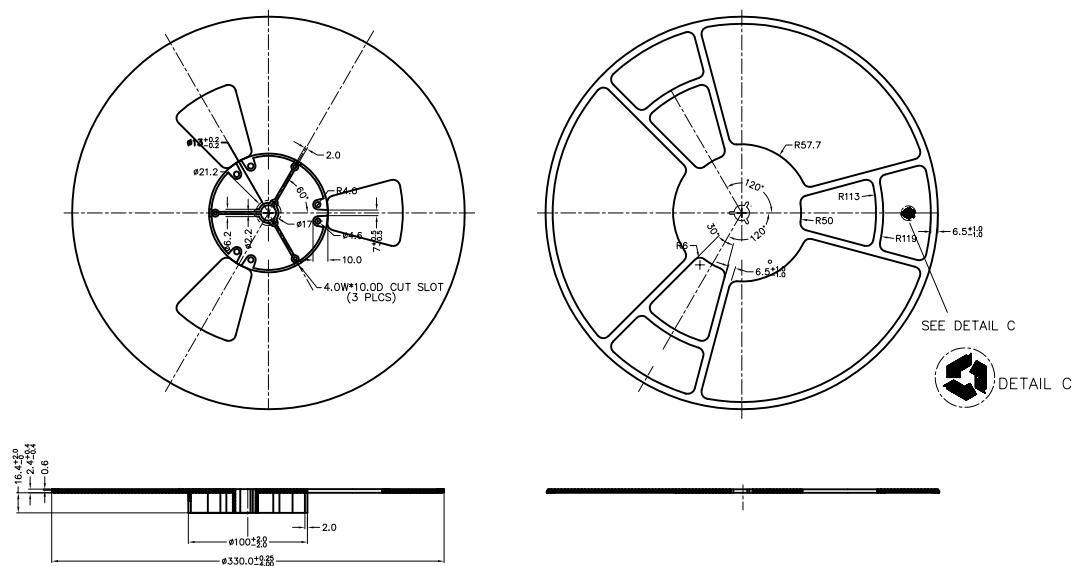
8229819_Reel_revA

Note: All dimensions are in millimeters.

Revision history

Table 9. Document revision history

Date	Version	Changes
02-Dec-2020	1	First release.

Contents

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