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# FDI030N06

## N-Channel PowerTrench® MOSFET

60 V, 193 A, 3.2 mΩ

### Features

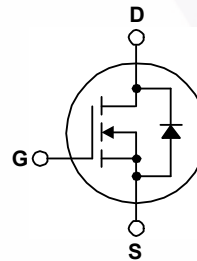
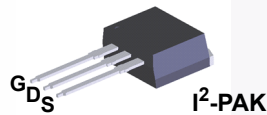
- $R_{DS(on)} = 2.6 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 75 \text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Renewable System



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise note.

Symbol	Parameter	FDI030N06	Unit
$V_{DSS}$	Drain to Source Voltage	60	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ , Silicon Limited)	193*
		- Continuous ( $T_C = 100^\circ\text{C}$ , Silicon Limited)	136*
		- Continuous ( $T_C = 25^\circ\text{C}$ , Package Limited)	120
$I_{DM}$	Drain Current	- Pulsed (Note 1)	772 A
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	1434 mJ
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	6 V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	231 W
		- Derate Above $25^\circ\text{C}$	1.54 W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

### Thermal Characteristics

Symbol	Parameter	FDI030N06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.65	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDI030N06	FDI030N06	I <sup>2</sup> -PAK	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0 \text{ V}$ , $T_C = 25^\circ\text{C}$	60	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1 \text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.05	-	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}$ , $V_{GS} = 0 \text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 48 \text{ V}$ , $T_C = 150^\circ\text{C}$	-	-	500	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 75 \text{ A}$	-	2.6	3.2	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{ V}$ , $I_D = 75 \text{ A}$	-	154	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$	-	7380	9815	pF
$C_{oss}$	Output Capacitance		-	1095	1455	pF
$C_{rss}$	Reverse Transfer Capacitance		-	415	625	pF
$Q_{g(tot)}$	Total Gate Charge at 10V		$V_{DS} = 48 \text{ V}$ , $I_D = 75 \text{ A}$ , $V_{GS} = 10 \text{ V}$	-	116	151
$Q_{gs}$	Gate to Source Gate Charge	(Note 4)	-	40	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	35	-	nC

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30 \text{ V}$ , $I_D = 75 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_G = 4.7 \Omega$	-	39	87	ns
$t_r$	Turn-On Rise Time		-	178	366	ns
$t_{d(off)}$	Turn-Off Delay Time		-	54	118	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	33	76

### Drain-Source Diode Characteristics

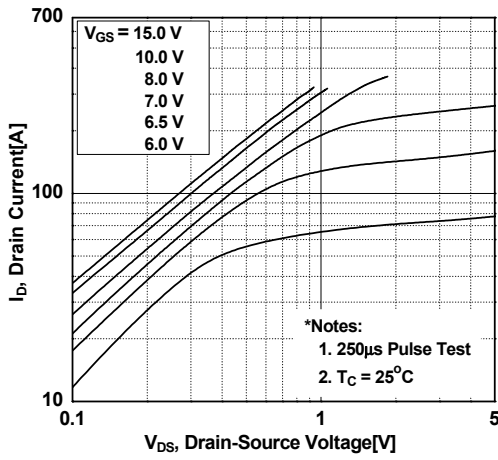
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	193	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	772	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 75 \text{ A}$	-	-	1.3	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 75 \text{ A}$ , $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	46	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	50	-	nC

#### Notes:

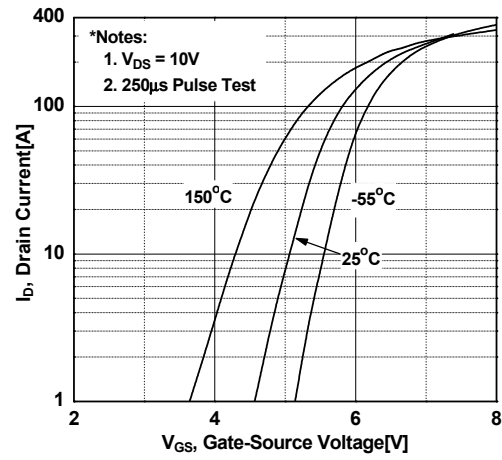
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $L = 0.51 \text{ mH}$ ,  $I_{AS} = 75 \text{ A}$ ,  $V_{DD} = 50 \text{ V}$ ,  $R_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 75 \text{ A}$ ,  $di/dt \leq 450 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

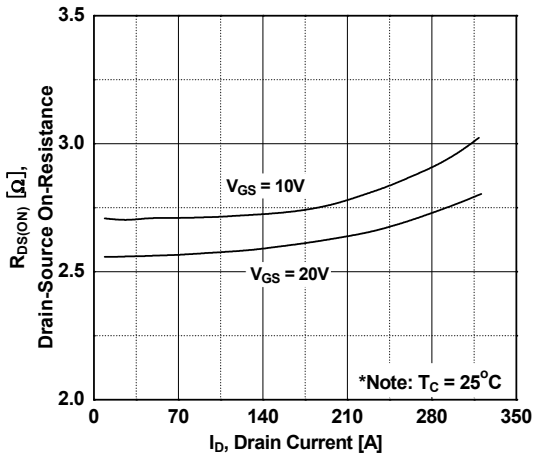
**Figure 1. On-Region Characteristics**



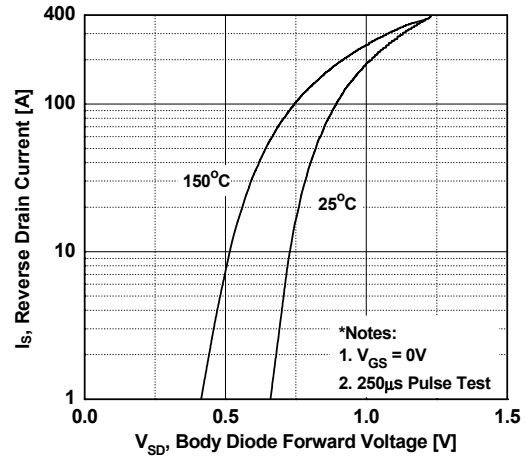
**Figure 2. Transfer Characteristics**



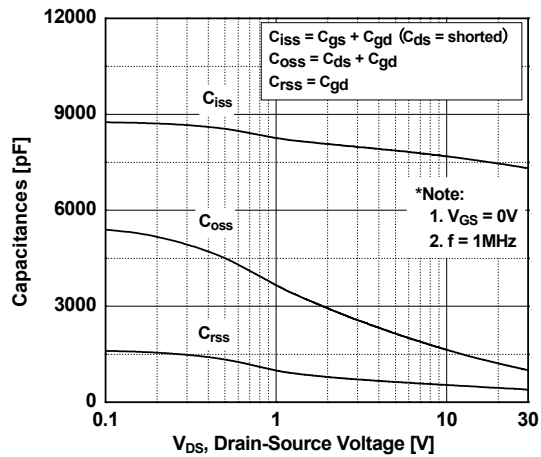
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



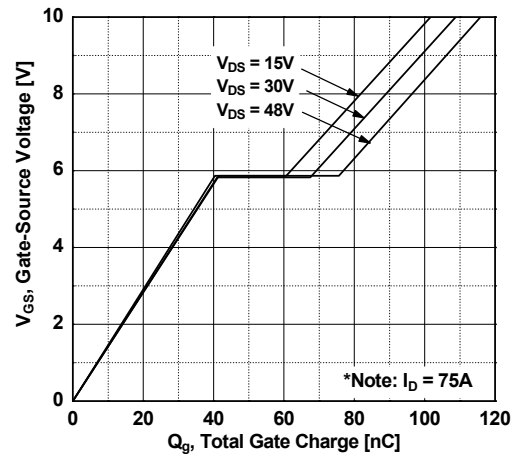
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

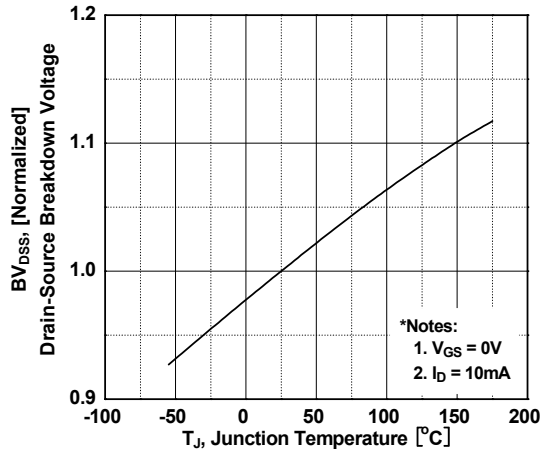


**Figure 6. Gate Charge Characteristics**

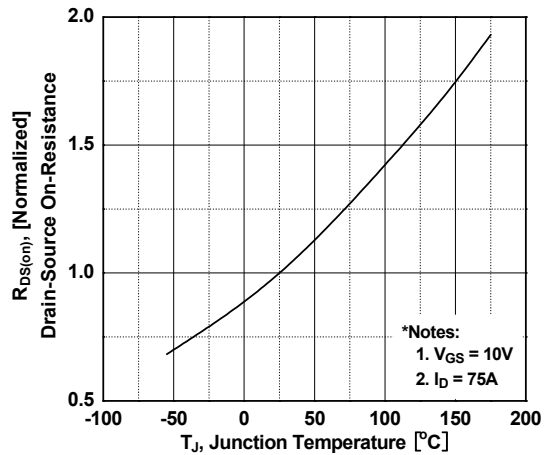


**Typical Performance Characteristics** (Continued)

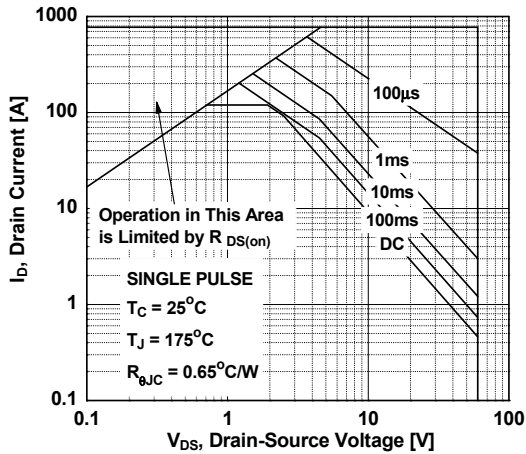
**Figure 7. Breakdown Voltage Variation vs. Temperature**



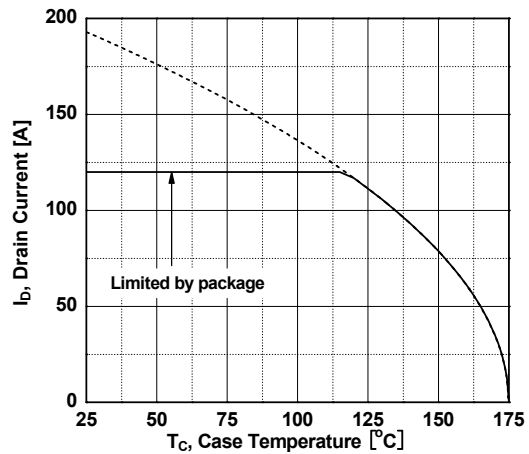
**Figure 8. On-Resistance Variation vs. Temperature**



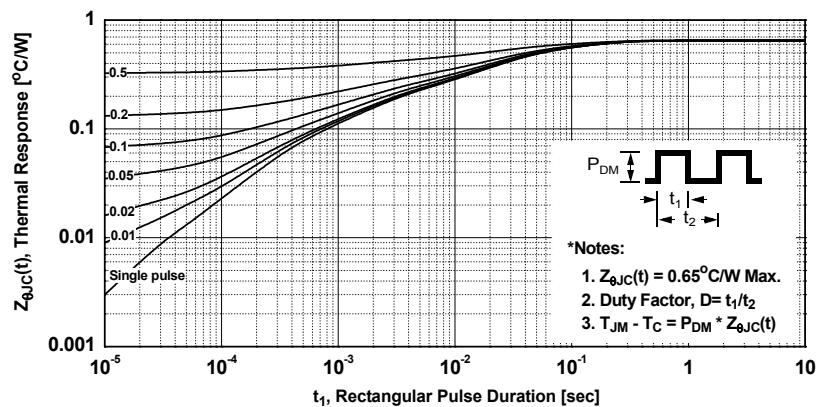
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**





**Figure 12. Gate Charge Test Circuit & Waveform**



**Figure 13. Resistive Switching Test Circuit & Waveforms**

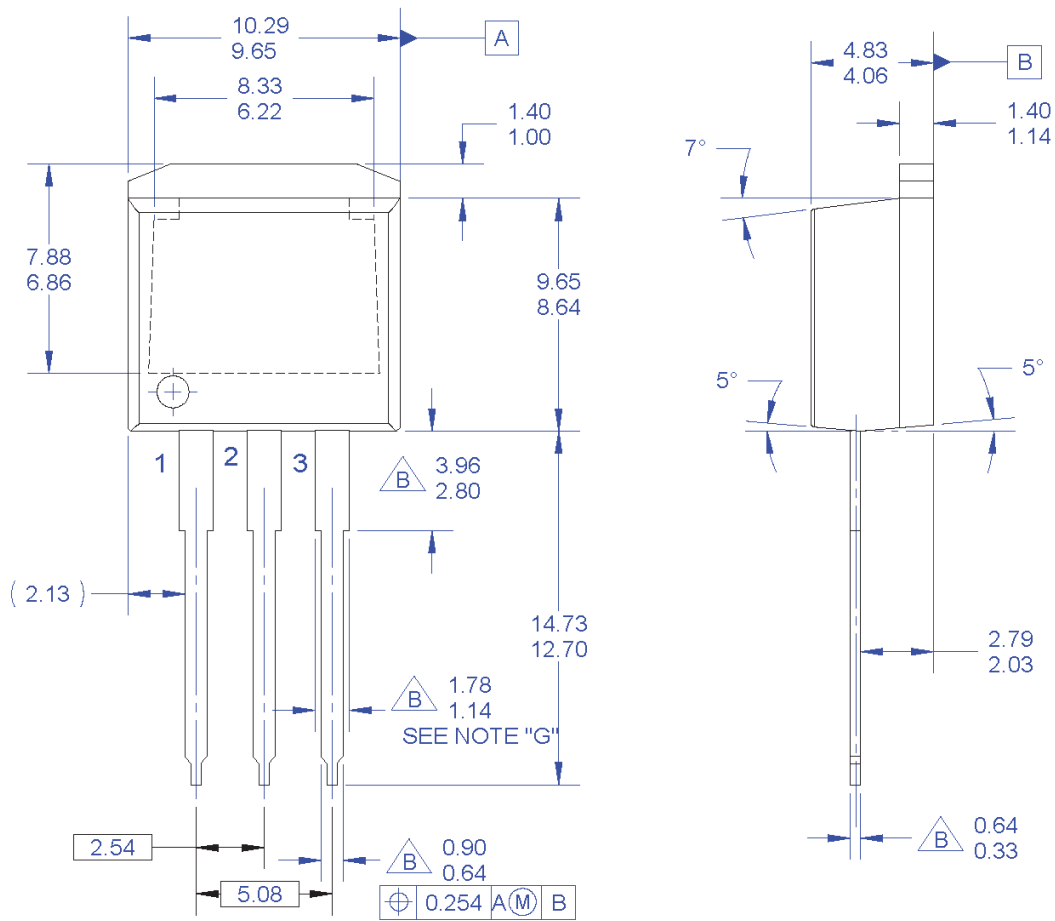


**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**



Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**NOTES:**

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- $\Delta$  B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

**Figure 16. TO262 (I<sup>2</sup>PAK), Molded, 3-Lead, Jedec Variation AA**

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