EVM User's Guide: TRF1208-AFE7950EVM

TRF1208-AFE7950-EVM Evaluation Module

ABSTRACT

The evaluation module TRF1208-AFE7950-EVM is used to evaluate the performance of TI's AFE79xx family of integrated RF sampling transceivers with TI's TRF1208 differential amplifier. The AFE79xx devices support up to 4 transmit, 4 receive, and 2 feedback channels (4T4R2F) and integrates phase-locked loop (PLL) and voltage-controlled oscillator (VCO) for generating data-converter clocks. The AFE79xx device integrates 8 JESD204B- and JESD204C-compatible serializer or deserializer (SerDes) transceivers capable of running up to 29.5 Gbps to transmit and receive digital data through the onboard FPGA mezzanine card (FMC) connector.

TRF1208 device is a fully differential amplifier that either drives the ADC of receive paths (in S2D configuration) or are driven by the DAC of the transmit path (in D2S configuration). The EVM includes the LMK04828 clock generator to provide reference clocks and SYSREF to the analog front end (AFE) and capture card (field-programmable gate array, FPGA). The evaluation module (EVM) works off a single 5.5-V input and includes complete power management circuitry. External clocking options include support for feeding the reference clock (for the on-chip PLL). The design interfaces with the TI pattern and capture card solution (TSW14J56 and TSW14J57), as well as many FPGA development kits.

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1 EVM Overview

The TRF1208-AFE7950-EVM includes a clocking and power solution, and runs off a single 5.5-V supply. As Figure 1-1 shows, the RF inputs and outputs using SMA connectors are on the top side of the EVM. A reference clock (for example, 10 MHz) to lock the onboard voltage-controlled crystal oscillator (VCXO) with the LMK04828, PLL-1 can be provided to the connector named LMK CLKIN (SMA J15). [1]

SMA J13 (REF_CLK_HIGH) or SMA J14 (REF_CLK_LOW) can be used to feed an external reference clock to lock the PLLs in the AFE79xx. The USB connector and the 5.5-V connector are on the right side of the board.

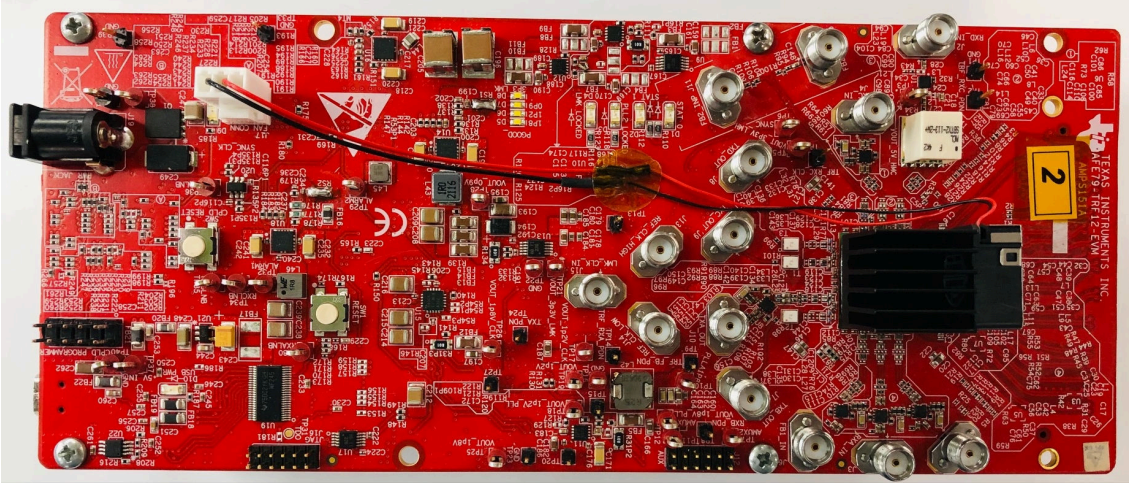

Figure 1-1. TRF1208-AFE7950-EVM Top View

Figure 1-2 shows the bottom view of the TRF1208-AFE7950-EVM.

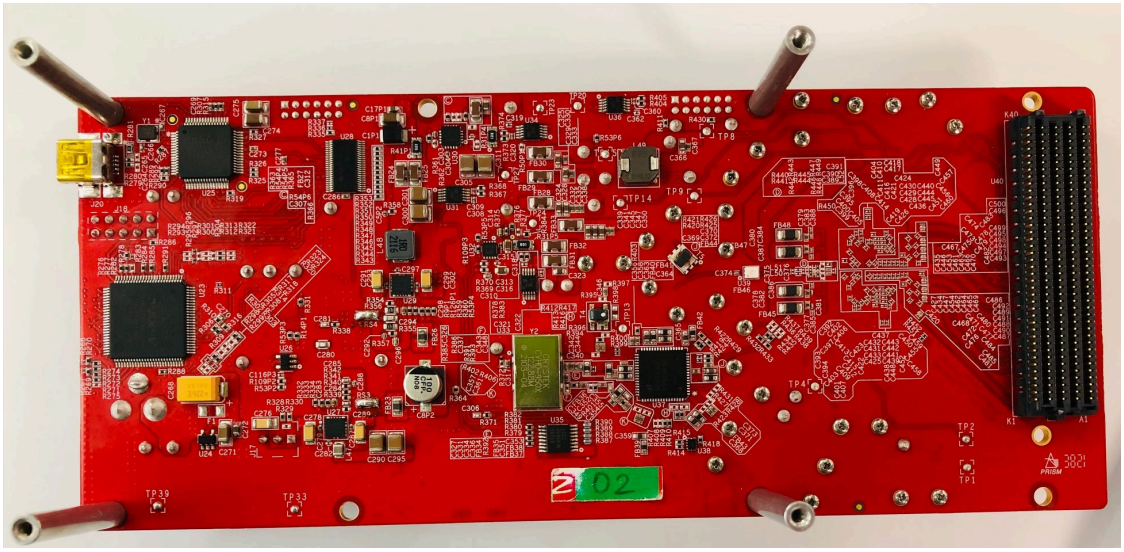

Figure 1-2. TRF1208-AFE7950-EVM Bottom View

[1] Typically, lab equipment has a 10-MHz oscillator output to synchronize multiple lab systems. The onboard LMK04828 can accept the 10 MHz from external lab equipment to ensure synchronization and coherency of the data capture and generation to the TRF1208-AFE7950-EVM.

The capture card that is used with the TRF1208-AFE7950-EVM is typically the TSW14J56 or TSW14J57. The TSW14J56 supports a SerDes speed of up to 12.5 Gbps and the TSW14J57 goes as high as 15 Gbps. The choice of the TSW14J56 or TSW14J57 EVM depends on the AFE79xx JESD204 configuration and the associated SerDes rate.

1.1 Hardware

Two bench power supplies are required to power the TRF1208-AFE7950-EVM and TSW14J5x EVM. A PC to program the EVM and capture card is required. For more information, see Section 1.1.1. All lab equipment requirements (such as signal source, signal analyzer, and so forth) are left to the users' discretion.

Note

Typically, the bench power supply with a rating of 5.5 V is used to power the TRF1208-AFE7950-EVM. The nominal EVM power supply voltage is 5 V. The additional 0.5-V overhead is added to compensate for the power cable loss as the TRF1208-AFE7950-EVM and TSW14J56/TSW14J57 are configured to full operating mode to accommodate the voltage drop associated with power cable loss.

1.1.1 Recommended Test Environment

The recommended test environment for the TRF1208-AFE7950-EVM are as follows:

- Power supply at 5.5 V, 4 A maximum for the TRF1208-AFE7950-EVM
- Power supply at 5.5 V, 3 A maximum for the TSW14J56 EVM
- Power supply at 12 V, 3 A maximum for the TSW14J57 EVM (optional evaluation)
- A PC that supports USB 3.0 for fast file transfer from ADC capture and DAC pattern loading
- High-quality RF signal generator that supports RF frequency of interest for evaluation. The example set-up uses Keysight PSG series of signal generator.
- High-quality RF spectrum analyzer that supports RF frequency of interest for evaluation. The example set-up uses Rohde & Schwarz FSQ-26 series of spectrum analyzer.

1.1.2 Required Hardware

The required hardware for the TRF1208-AFE7950-EVM are as follows:

- TSW14J56 EVM (optional: TSW14J57 EVM)
- TRF1208-AFE7950-EVM
- USB 3.0 cable
- USB 2.0 Mini-B cable
- Two power supply cables

1.2 Required Software

The software used to configure the TRF1208-AFE7950-EVM is called *Latte*. The latest version of Latte is available for download from TI's MySecure website. The software can be request after signing into myTI at this link. The installer file is called *AFE79xx_EVM_GUI_v1p4p4p1*.

The HSDC Pro software controls the TSW14J5x, and can be downloaded from www.ti.com/tool/dataconverterpro-sw. HSDC Pro version 5.0 or higher is required.

1.2.1 Software Installation Sequence

1. Install High-Speed Data Converter Pro software. Follow all the instructions within the installer execution process. Note the directory to which the High-Speed Data Converter Pro software is installed.

   Note

   The default HSDC PRO software directory is in:

   C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro

2. Install AFE79xxEVM_GUIv1p4p4p1.exe. Follow all the instructions within the installer execution process. As shown in Figure 1-3, the installer will install the following:
   - Latte 5.2.3
   - AFE79xx Latte Library v1.44

Note

Both the base Latte software and the AFE79xx Latte Library will be updated as needed throughout the product development process.

- National Instruments LabVIEW™ Runtime Engine 2014
- Associated HSDC PRO INI Files required for TRF1208-AFE7950-EVM.

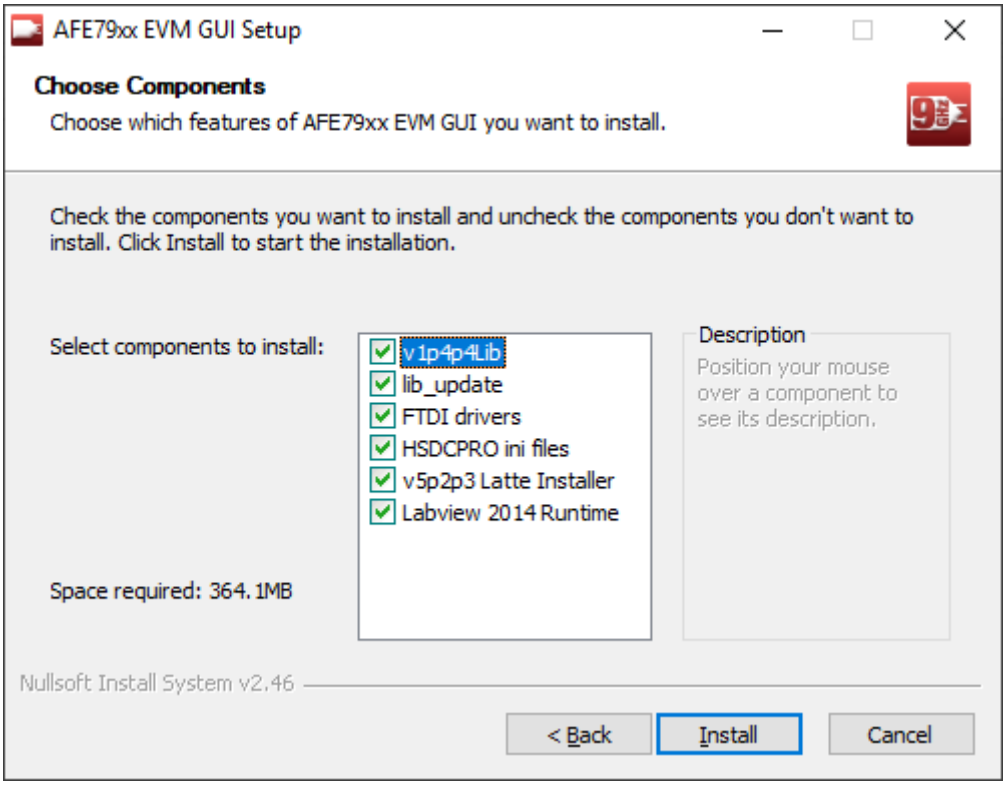

Figure 1-3. Latte Installer Options

3. Note that the Default Latte Software Directory is installed at C:\Users\"User ID"\Documents\Texas Instruments\Latte.

Note

Replace the “User ID” with the proper Windows login ID.

1.2.2 Software Installation Checks

After installing Latte, the AFE79xx.ini files appear in the respective folders in the HSDC Pro directory. Verify these files were properly installed by inspecting the relevant directories. The .ini files to look for are AFE79xx_1x2FB_44210.ini, AFE79xx_2x2RX_24410.ini, and AFE79xx_2x2TX_44210.ini.

For the TSW14J56, see the directories that follow:

- C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J56revD Details\ADC files
- C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J56revD Details\DAC files

For the TSW14J57, see directories that follow:

- C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J57revE Details\ADC files
- C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J57revE Details\DAC files

1.3 Signal Chain of the EVM Board

Figure 1-4 shows the signal chain of the board.

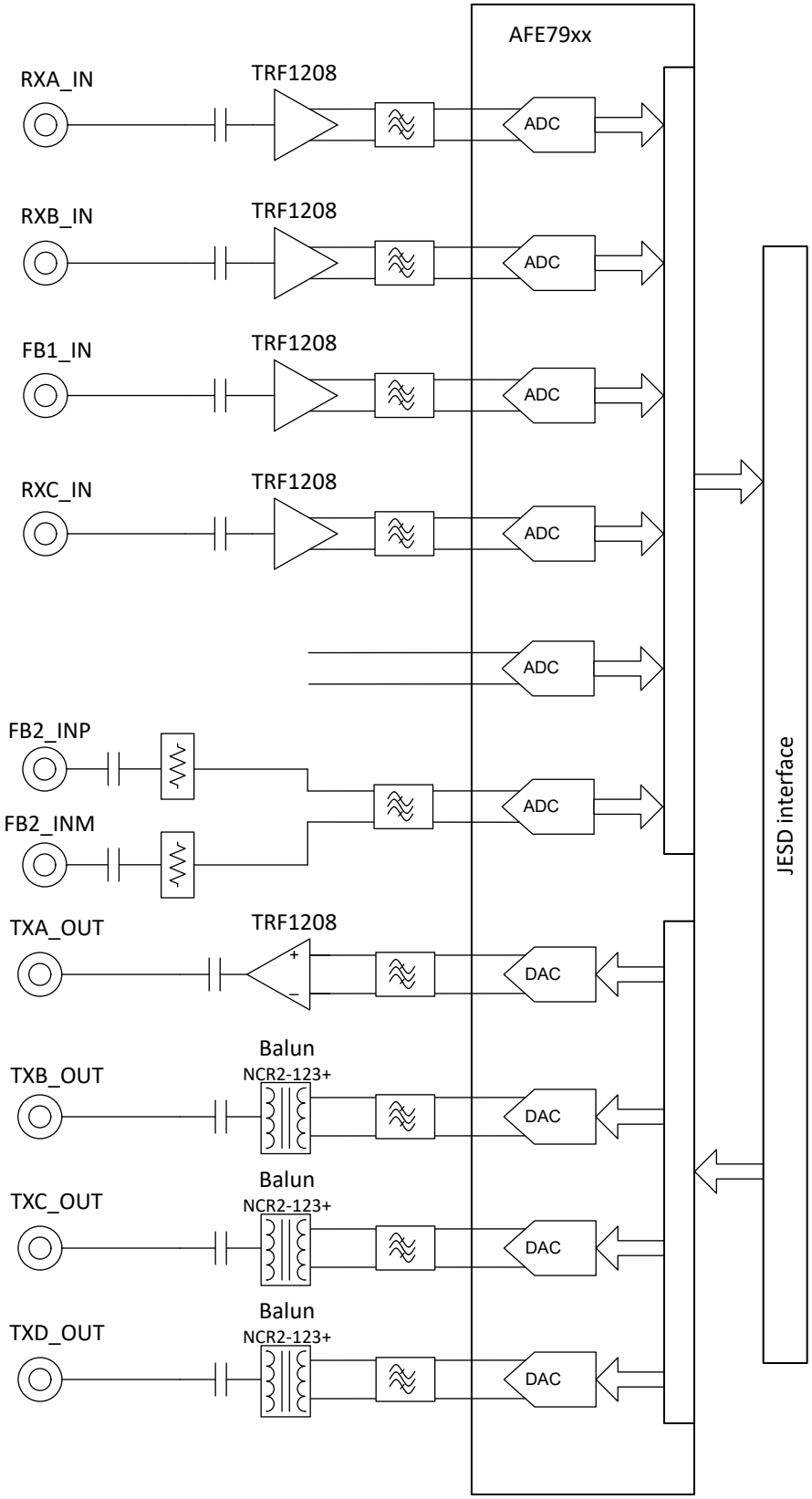

Figure 1-4. AFE79 + TRF1208 EVM Block Diagram

2 Hardware Setup (TSW14J56 Used as an Example)

2.1 Power Supply Setup

The steps for setting up the power supply are as follows:

1. Connect 5.5-V power supply to the power jack (PWR_JACK) connector (J19) of the TRF1208-AFE7950-EVM. The 5.5-V supply may be dropped to 5 V if power cable loss is not significant in the setup.
2. Check the D9 (PWR) LED. It should be lit up. The power supply should draw about 550 mA to 650 mA.
3. Connect a USB Type Mini-B Cable from the PC to the USB port (J20) of the TRF1208-AFE7950-EVM.
4. Check the D10 (USB_PWR) LED. It should be lit up. The LED light may be weak depending on the USB cable length. If the LED is not lit up, then use a shorter USB cable. TI tested a three foot long USB cable in this setup.
5. The power supply sequencer on the TRF1208-AFE7950-EVM has power status for each rail. If the power good (PGOOD) is in logic HI, then the corresponding power supply rail is powered correctly. The respective LED will light up. Check the following LEDs to see if they are lit.
   - D5 (1P8) LED
   - D6 (1P2) LED
   - D7 (0p9) LED
   - D8 (3p3_LMK) LED

2.2 TRF1208-AFE7950-EVM and TSW14J56 EVM Connections

The steps for connecting the TRF1208-AFE7950-EVM and TSW14J56 EVM are as follows:

1. Connect FMC connector U40 of TRF1208-AFE7950-EVM to FMC connector J4 of TSW14J56 EVM.
2. With the power supply in powered down mode, connect 5.5-V, 3-A maximum power supply to J11 *+5 V IN* connector of the TSW14J56EVM.
3. Connect USB 3.0 cable from the PC to the J9 connector of the TSW14J56 EVM.
4. With the power supply in powered down mode, connect the 5.5-V, 4-A maximum power supply to J19 *CONN JACK PWR* connector of the TRF1208-AFE7950-EVM.
5. Connect the USB 2.0 cable from the PC to the J20 connector of the TRF1208-AFE7950-EVM.
6. Optionally, connect the 10-MHz lab equipment reference to J15 (LMK_CLK_IN) connector.

2.3 RF Test Equipment Setup

RF Test Setup requires RF signal generators, spectrum analyzer, attenuator pads, power combiners, cables, and so forth. Depending on the type of test, the appropriate setup can be used. Examples of the RF Test Setup are shown in TRF1208 EVM.

3 Latte Overview

1. Launch the Latte GUI from the desktop shortcut or from All Programs > Texas Instruments. Figure 3-1 shows how the Latte GUI appears.

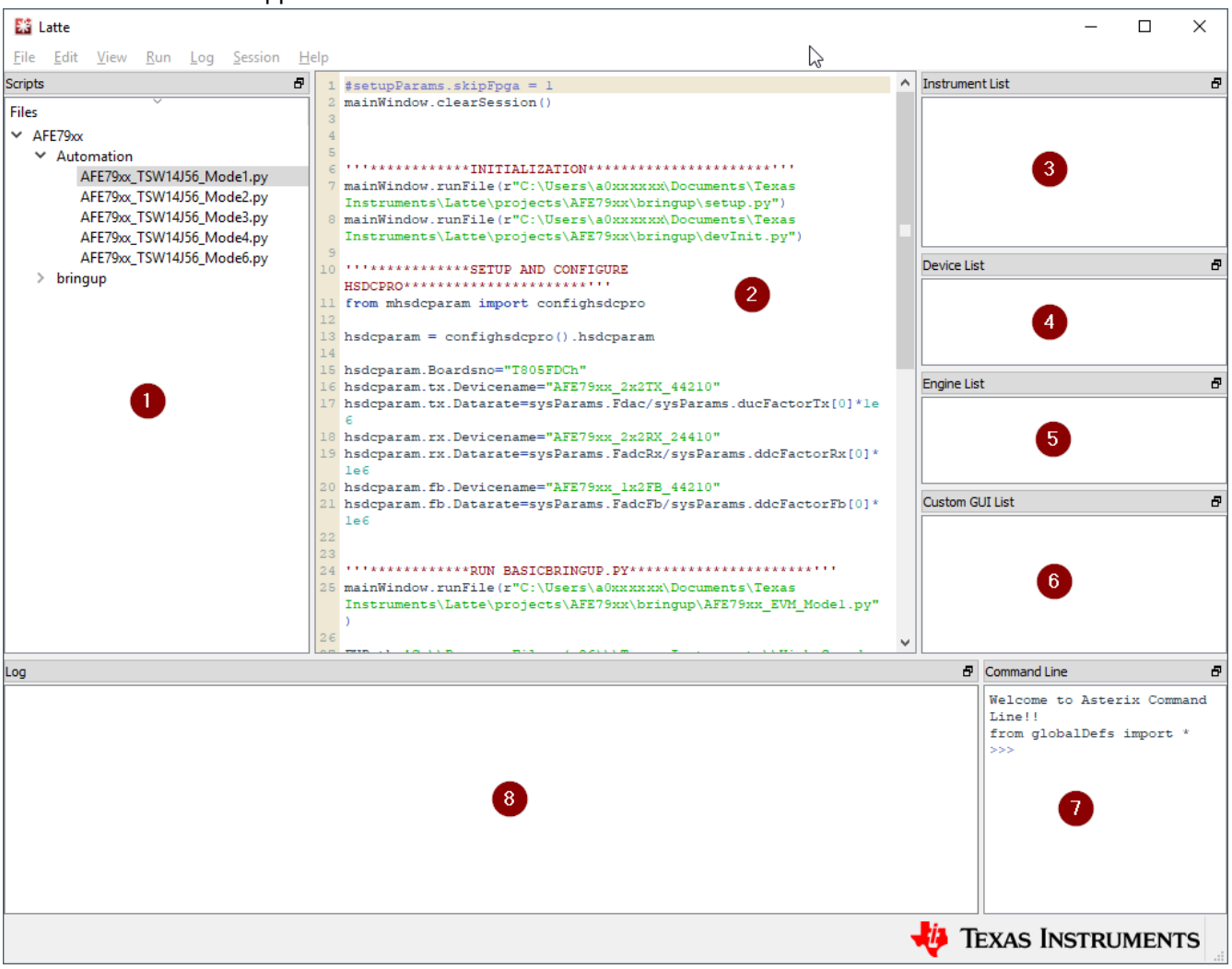

Figure 3-1. Latte GUI Overview

3.1 Latte User Interface

Figure 3-1 shows how the Latte UI is split into 8 windows (labeled 1 to 8) with the functionality that follows:

- **Window 1:**

  This window (also called *Scripts*) shows the list of python scripts available that generate the register commands to configure the TRF1208-AFE7950-EVM. The script files shown are located in the ..\Documents\Texas Instruments\Latte\projects\AFE79xx\bring-up folder. Modify and create new scripts as necessary, which appear in this sub-window when Latte is restarted.
- **Window 2:**

  This window (also called *Editor*) shows the code in the script currently selected and can be used to modify and save the code as necessary.
- **Window 3 to 6:**

  These windows get updated as the scripts run to configure the TRF1208-AFE7950-EVM, and are mostly informational.

- **Window 7:**

  This window (also called *Command Line*) is used to enter and run individual commands. Examples of such commands include changing the TX, RX, FBRX DSA, NCOs, and so forth.
- **Window 8:**

  This window (also called *Log*) displays messages during execution of scripts to display the current status. This window is also used for troubleshooting.

3.2 Useful Latte Short-Cuts

Run Script file: run a script file by first selecting the file in the Scripts window and then by pressing F5 (or selecting *Run* and then *Buffer* in the menu bar).

Run part of script: run part of a script file by selecting the lines in the Editor window and then by pressing F7 (or selecting *Run* and then *Run Selection* in the menu bar).

Stop Execution: stop the current execution by pressing F10 (or selecting *Run* and then *Stop* in the menu bar).

Clear Session: the current session can be cleared to reset the Latte UI to its initial state by pressing Ctrl-T (or selecting *Session* and then *Clear Session* in the menu bar). This process is equivalent to a restart and can be used to restart a session without closing the GUI.

4 TRF1208-AFE7950-EVM Automatic Configuration

This section guides the user through the sequence of steps to automatically bring up the TRF1208-AFE7950-EVM through the automation python routine. The example used in this section will be the default TRF1208-AFE7950-EVM Mode 1. Table 4-1 lists the default Mode 1 configuration overview.

Table 4-1. TRF1208-AFE7950-EVM Mode 1 Configuration Overview

Mode	Default Programming
TX (transmitter)	4 TXDACs are enabled, DSA = 0, LMFSHd_2TX = 44210, 6 × interpolation, 491.52-MSPS data rate
RX (receiver)	4 RXADCs are enabled, DSA = 0, LMFSHd_2RX = 24410, 12 × decimation, 245.76-MSPS data rate
FBRX (feedback receiver)	2 FBADCs are enabled, DSA = 0, LMFSHd_1FB = 22210, 6 × decimation, 491.52-MSPS data rate
SerDes	8 lanes running at 9830.4 Mbps
Data Converter Clock Rates	F_{RXADC} = 2949.12 MSPS, F_{FBADC} = 2949.12 MSPS, F_{TXDAC} = 8847.36 MSPS
Status	RX AGC is disabled, RX, TX DSA step impairments is uncorrected, DAC in interleaved mode

Table 4-2, Table 4-3, and Table 4-4 list the TSW14J5x INI files used to evaluate the RXADC, FBADC, and the TXDAC portion of the AFE79xx. The tables also list the associated channel mapping with respect to the TRF1208-AFE7950-EVM.

Table 4-2. RXADC TW14J5x INI Mapping (AFE79xx_2x2RX_24410)

ADC Channel Number in HSDC PRO ADC Panel(1)	TRF1208-AFE7950-EVM Connector	Associated AFE79xx Input
1,2	J3, RXA_IN	1RX
3,4	J1, RXB_IN	2RX
5,6	J4, RXC_IN	3RX
7,8	J2, RXD_IN	4RX

(1) For complex quadrature output (I/Q) of the RXADC, the odd number is the real channel, while the even number is the imaginary channel.

Table 4-3. FBADC TW14J5x INI Mapping (AFE79xx_1x2FB_44210)

ADC Channel Number in HSDC PRO ADC Panel(1)	TRF1208-AFE7950-EVM Connector	Associated AFE79xx Input
1,2	J6, FB1_IN	1FB
3,4	J5 and J11, FB2_IN	2FB

(1) For complex quadrature output (I/Q) of the FBADC, the odd number is the real channel, while the even number is the imaginary channel.

Table 4-4. TXDAC TSW14J5x INI Mapping (AFE79xx_2x2TX_44210)

DAC Channel Number in HSDC PRO DAC Panel(1)	AFE79xx EVM Connector	Associated AFE79xx Input
1,2	J10, TXA_OUT	1TX
3,4	J7, TXB_OUT	2TX
5,6	J9, TXC_OUT	3TX
7,8	J8, TXD_OUT	4TX

(1) For complex quadrature output (I/Q) of the TXDAC, the odd number is the real channel, while the even number is the imaginary channel.

4.1 Steps to Start Automatic Configuration

1. Within the Microsoft® Windows® PC, start the HSDC PRO software by going to Start > Texas Instruments > High Speed Data Converter Pro. As shown in Figure 4-1, ensure that the High-Speed Data Converter Pro started properly. Take note of the *Serial Numbers* of the TSW14J56 EVM after the device is connected.

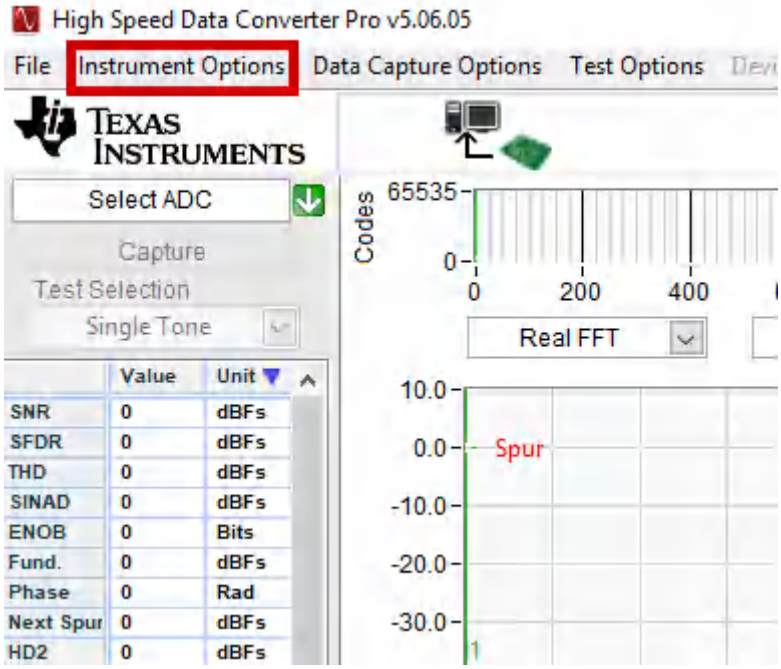

Figure 4-1. Connecting to TSW14J56 From HSDC PRO

2. Press the *OK* button to proceed the connection of the TSW14J56 EVM to the PC.

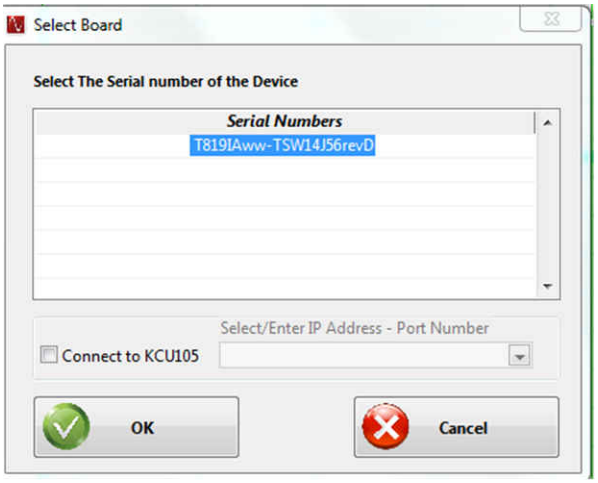

Figure 4-2. HSDC Pro Connect to Board

3. Within the Microsoft Windows PC, start the Latte software by going to Start > Texas Instruments > Latte. Ensure that the Latte software had started properly.
4. On the left hand side of the Latte, within the Scripts window, expand AFE79xx > Automation > AFE79xx_TSW14J56_Mode1.py. Figure 4-3 shows the python script.

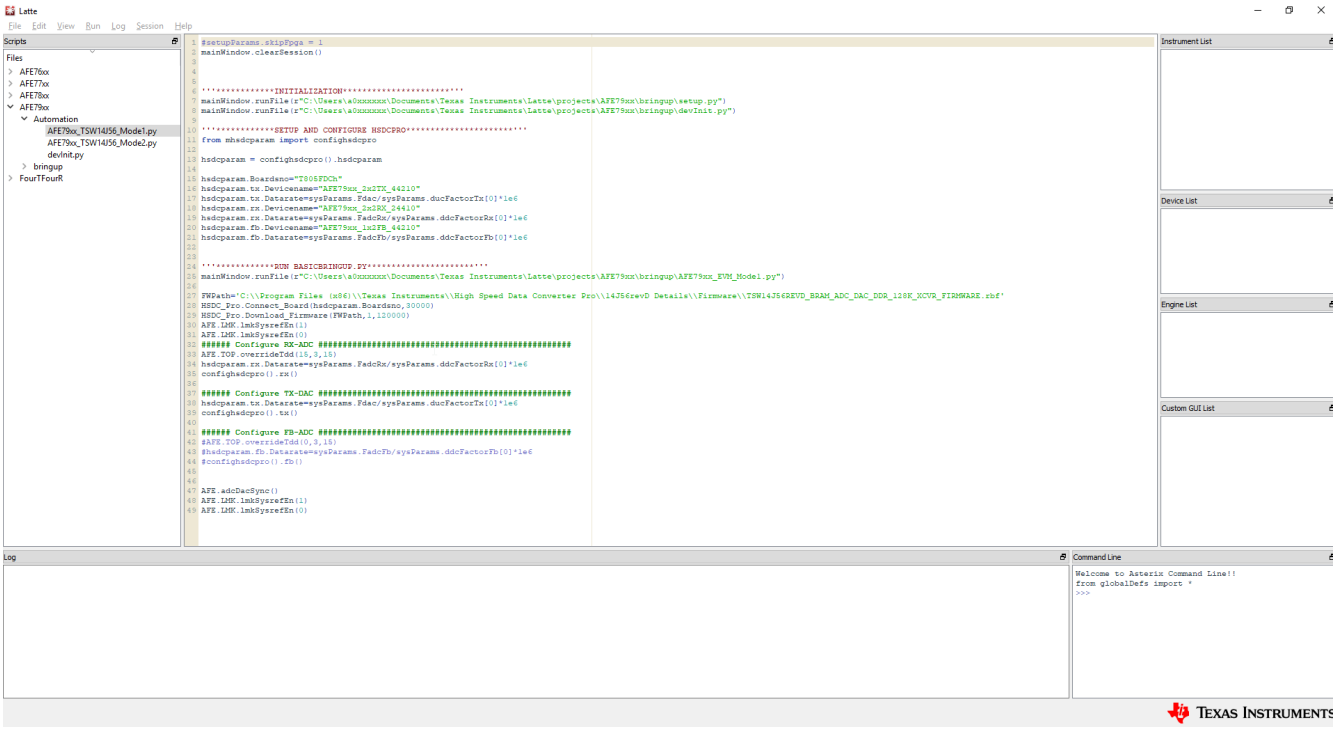

Figure 4-3. AFE79xx Mode 1 Automatic Configuration Script

5. Three parameters within the AFE79xx_TSW14J56_Mode1.py must be changed per the directory being used by the High-Speed Data Converter Pro software and the Latte software.
6. As shown in Figure 4-4, change item #1 and #2 to reflect the location of the Latte install directory for the setup.py and devInit.py. Usually the area where *a0xxxxxx* must be replaced with the Windows user ID login.

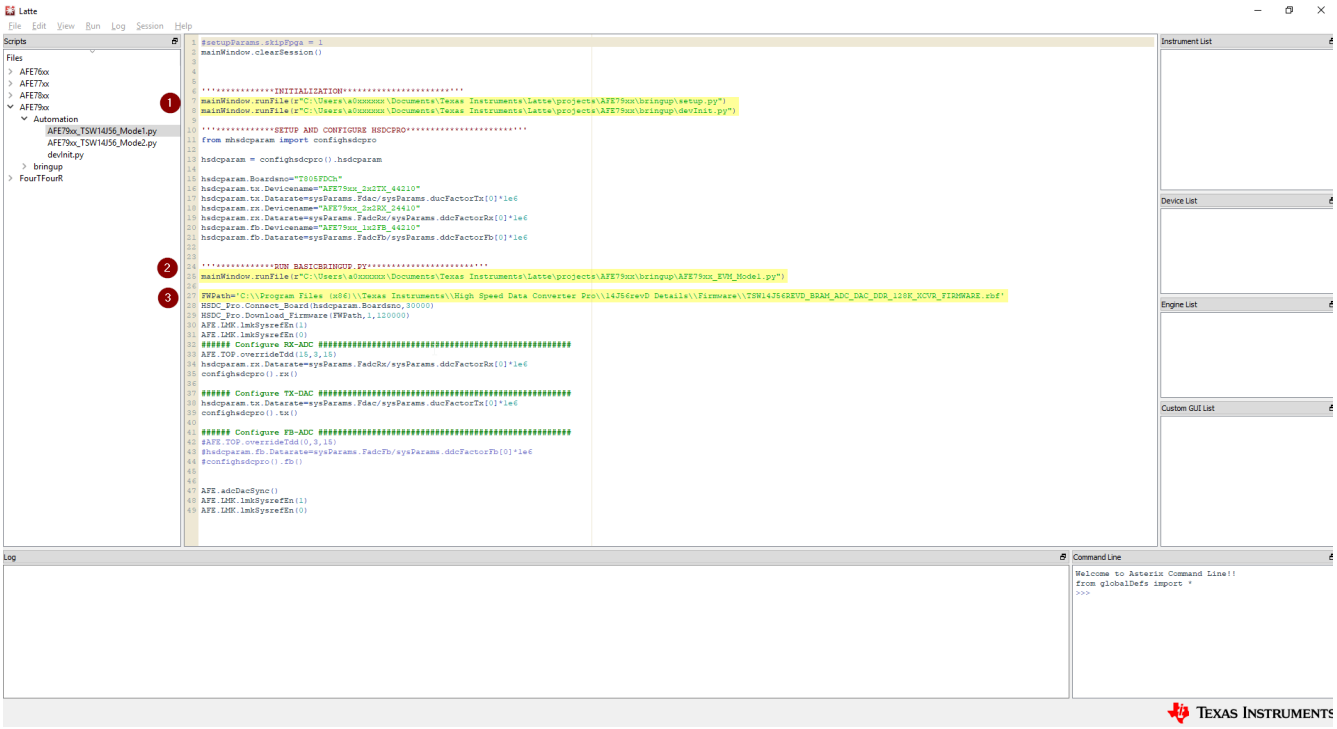

Figure 4-4. Directory Parameter to be Changed in the Automation Script

7. As shown in Figure 4-4, change item #3 to reflect the location of the High-Speed Data Converter Pro directory for the TSW14J56 firmware.

8. As shown in Figure 4-5, enter the serial number of the TSW14J56 EVM per the highlighted location in .

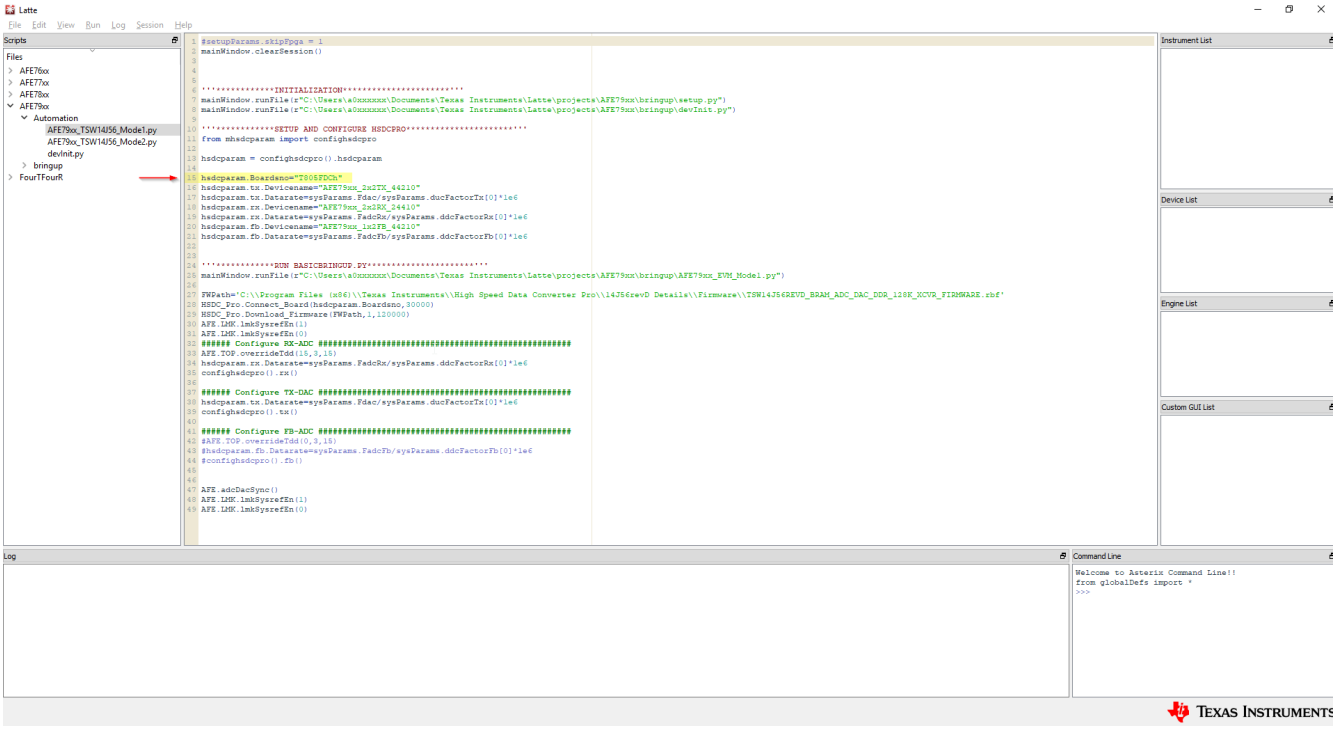

Figure 4-5. TSW14J56 EVM Serial Number Location

9. With the AFE79xx_TSW14J56_Mode1.py highlighted, press the F5 button to execute the script. The script will automate both High-Speed Data Converter Pro software and Latte software to automatically bring up the JESD204B link.
10. As shown in Figure 4-6 and Figure 4-7 expect the following two error messages after the script runs.

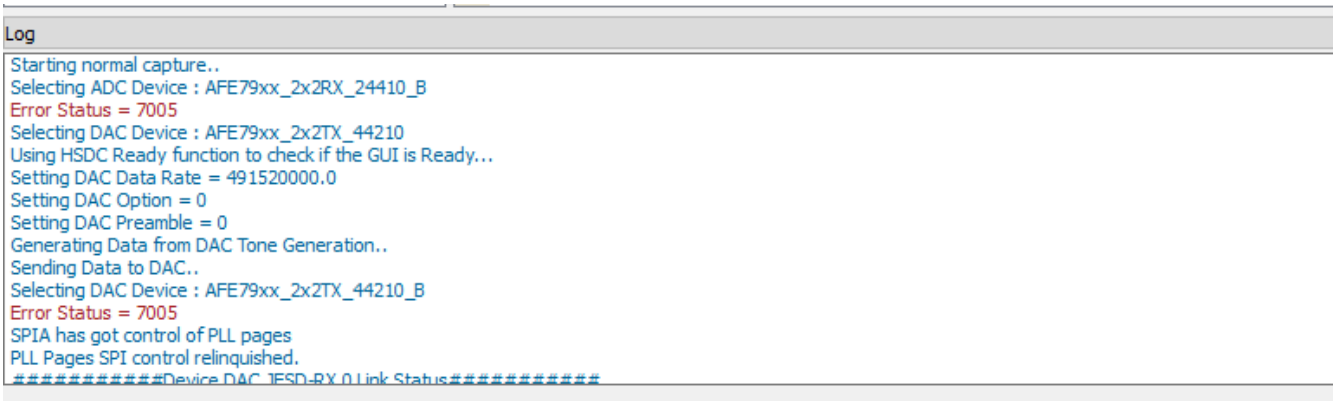

Figure 4-6. Latte Error 1

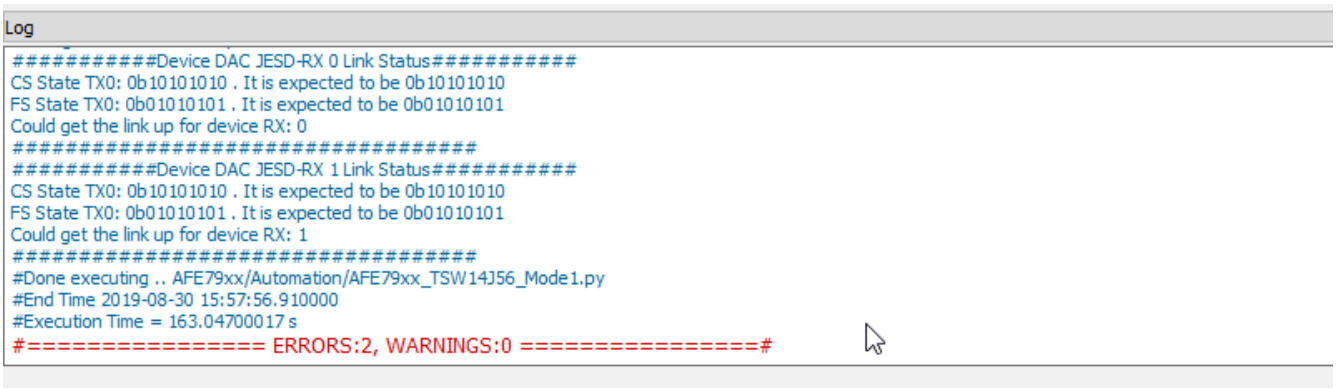

Figure 4-7. Latte Error 2

11. The default TRF1208-AFE7950-EVM has the following RF frequency matching network:
    a. RXA (TRF1208): 2.3 GHz
    b. RXB (TRF1208): 5 GHz
    c. RXC (TRF1208): 8 GHz
    d. RXD: None
    e. FB1 (TRF1208): 6 GHz
    f. FB2 (Differential connectors): 6 GHz
    g. TXA (TRF1208): 6 GHz
    h. TXB (Balun): TBD GHz
    i. TXC (Balun): 6 GHz
    j. TXD (Balun): TBD GHz
12. The example script to change the NCO to match the default RF frequency matching network is the following:

```
AFE.updateTxNco(0,6000,0,0)
AFE.updateTxNco(1,6000,0,0)
AFE.updateTxNco(2,6000,0,0)
AFE.updateTxNco(3,6000,0,0)
AFE.updateRxNco(0,2300,0,0)
AFE.updateRxNco(1,5000,0,0)
AFE.updateRxNco(2,8000,0,0)
AFE.updateRxNco(3,6000,0,0)
AFE.updateFbNco(0,6000,0)
AFE.updateFbNco(1,6000,0)
```

13. As shown in Figure 4-8, enter the commands in the command line prompt or execute AFE79xx_DC101_NCO_Setup.py (under Automation Folder of AFE79xx) in the Latte through F5 key.

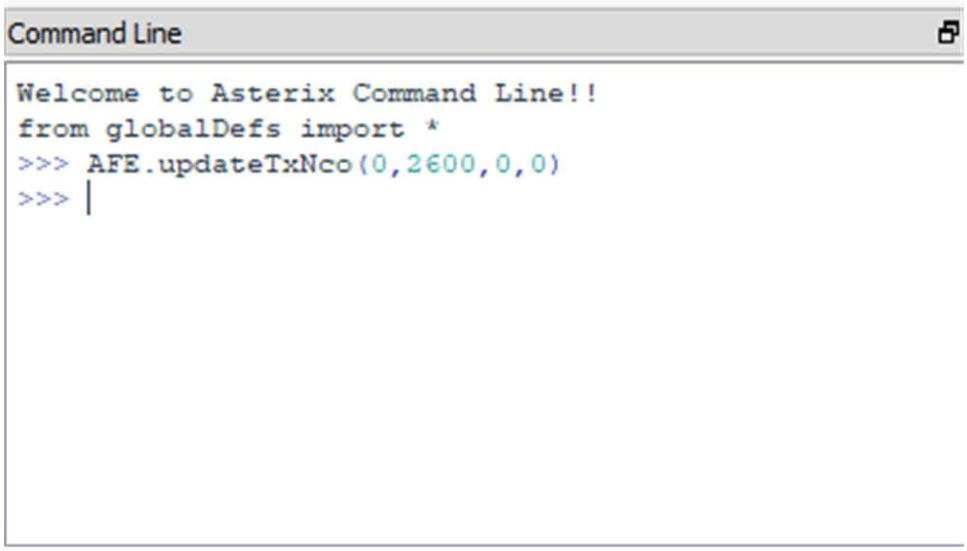

Figure 4-8. Latte Command Prompt for Updating TXNCO

4.2 TXDAC Evaluation

1. Connect the spectrum analyzer to J10 (TXA), J7 (TXB), J9 (TXC), or J8 (TXD) to monitor the TXDAC output.
2. The user may now change the DAC patterns or load custom DAC patterns through external files (see Section 7.1).

4.3 RXADC and FBADC Evaluation

1. Before starting the RXADC and FBADC performance capture, the test option of the HSDC PRO must be setup. Go to *Test Options* to enter the *Filter Parameters* menu. By default, there are 25 bins to remove on either side of fundamental and 25 bins near DC to remove. As shown in Figure 4-9, change the number of bins to remove on either side of fundamental to 100 bins.
   a. With 245.76 MSPS of data rate for RXADC at 16384 sample points, this removes 1.5 MHz of bins on either side of the fundamental.
   b. With 491.52 MSPS of data rate for FBADC at 16384 sample points, this removes 3.0 MHz of bins on either side of the fundamental.
   c. The number of bins to be removed is a standard recommendation from TI to remove the effect of the ADC sampling clock in-band phase noise from affecting the broadband noise used to calculate the SNR through the FFT engine. The number of bins must be adjusted based on the end-application standard.

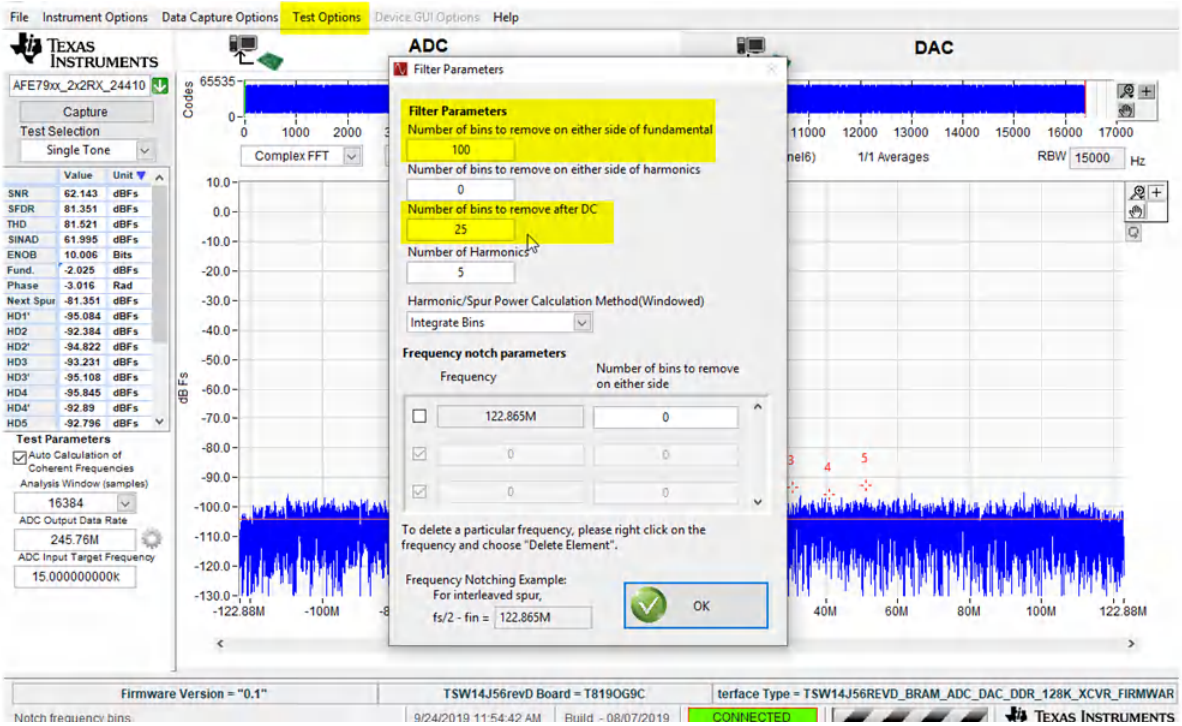

Figure 4-9. HSDC PRO ADC Performance FFT Binning Configuration

2. Connect the RF signal generator output to J3 (RXA_IN), J1 (RXB_IN), and J4 (RXC_IN) to capture the RF input to the ADC. On the High-Speed Data Converter Pro, press the *Capture* button to capture the ADC data.

3. Feed in a tone of 10 MHz offset from the channel frequency. For example, feed 2310 MHz to RXA_IN, 5010 MHz to RXB_IN, and 6010 MHz to FB1_IN. Set the signal level to get about -4 dBFS at the ADC output. Since the gain is different for various channels, the signal generator's output levels will be different.
   a. RXA_IN is Channel 1 and 2 in FFT Channel Selection
   b. RXB_IN is Channel 3 and 4 in FFT Channel Selection
   c. FB1_IN is Channel 1 and 2 in FFT under FB mode Channel Selection
4. Similarly, feed 8010 MHz to RXC_IN and 6010 MHz to FB2_IN. Set the signal level to get about -4 dBFS at ADC output.
   a. RXC_IN is Channel 5 and 6 in FFT Channel Selection
   b. FB2_IN is Channel 3 and 4 in FFT under FB mode Channel Selection
5. For Feedback ADC, execute the following commands or execute AFE79xx_FB_Capture.py through the F5 key.
   a.
```
###### Configure FB-ADC
################################################
AFE.TOP.overrideTdd(0,3,0)
hsdcparam.fb.Datarate=sysParams.FadcFb/sysParams.ddcFactorFb[0]*1e6confighsdcpro().fb()
```

5 Status Check and Troubleshooting Guidelines

This section provides a general guideline on the status indicators of the TRF1208-AFE7950-EVM and also the respective troubleshooting guidelines.

5.1 TRF1208-AFE7950-EVM Status Indicators

The green LED D3 should be lit at this point. D3 indicates that PLL loop 2 of the TRF1208 is locked. Optionally, the LED D4 indicates that PLL loop 1 of the TRF1208 is locked. If there are external equipment providing 10-MHz reference to the TRF1208 for lab equipment synchronization, then this LED D4 must be lit. The EVM is still functional without PLL loop 1 running, but PLL loop 2 is necessary for a successful bring-up.

- If PLL loop 1 is not running, then check the 10-MHz reference. This is necessary to achieve signal coherency with the signal generators and spectrum analyzer.
- If PLL loop 2 is not locked, then contact TI applications for additional support.

5.2 TSW14J56 EVM

D1 and D3 should not be lit for TSW14J56EVM. D2 and D4 should be flashing. These are necessary requirements for the JESD204B transceiver mode to work. D2 flashing indicates the TXDAC JESD204B link has been established, while D4 flashing indicates the RXADC or FBADC JESD204B link has been established.

TRF1208-AFE7950-EVM – data transmission on the DAC and data capture on the ADC should be enabled at this point. The RXNCO, FBNCO, and TXNCO can now be adjusted.

RXDSA, FBDSA, and TXDSA can be adjusted.

```
##RXDSA Adjustment
                        AFE.DSA.setRxDsa(chNo,dsaSetting)  ##chNo: ranges 0-3. dsaSetting: DSA
setting in dB
                        ##FBDSA Adjustment
                        AFE.DSA.setFbDsa(chNo,dsaSetting)  ##chNo: ranges 0-1. dsaSetting: DSA
setting in dB
                        ##TXDSA Adjustment
                        AFE.DSA.setTxDsa(chNo,dsaSetting)  ##chNo: ranges 0-3. dsaSetting: DSA
setting in dB
```

6 TRF1208-AFE7950-EVM Manual Configuration

This section guides the user through the sequence of steps to manually bring up the TRF1208-AFE7950-EVM. The automatic setup process is broken down in this section to allow the user to understand the process and make modifications accordingly.

6.1 TSW14J5x DAC Pattern Setup

Configure the HSDC Pro GUI to send a DAC pattern from the TSW14J5x board. If needed, see Section 7.1 and Section 7.2.

Note

Send a digital-to-analog converter (DAC) pattern to the TRF1208-AFE7950-EVM before configuring the EVM to provide the proper training SERDES signal for the adaptation algorithm of the AFE79xx SerDes RX equalizer. The DAC pattern can be sent from the TSW14J5x board controlled through the HSDC Pro GUI.

6.2 Connect Latte to Board

This step establishes a connection between the PC running Latte and the TRF1208-AFE7950-EVM.

1. In the scripts window, select *setup.py* and press F5 to run the program.
2. Check the Log window to ensure there are no errors where the following line should be displayed four times: *Kintex RegProgrammer – USB Instrument created*.
3. Missing or obsolete drivers for the FT4232H chip in the TRF1208-AFE7950-EVM is a common error source. Use the device manager to verify a connection between the PC and the EVM by checking the USB instantiations.
4. Update the PC with the appropriate driver, if necessary.

6.3 Compile Libraries

In this step, the library of scripts packaged with the Latte UI is compiled and takes approximately half a minute to run.

1. In the scripts window, select *devInit.py*.
2. Press F5 to run the program.
3. Check the Log window for status and errors.

6.4 Program TRF1208-AFE7950-EVM

In this step, the TRF1208 and AFE79xx on the TRF1208-AFE7950-EVM is programmed.

1. Click on the script named *AFE79xx_EVM_Mode1.py* and press F5. No errors are expected, but warnings regarding SPI control, relinquish, and reset property can be ignored. This step takes a few minutes.
2. Check the Log window to monitor any errors. This step completes the TRF1208-AFE7950-EVM configuration. Current consumption into the TRF1208-AFE7950-EVM is approximately 3 A.
3. An LOS error indicates that the SerDes RX is electrically idle, in which case, the TX output will not be normal. This error can be resolved by resending the data (the DAC pattern) and reconfiguring the TRF1208-AFE7950-EVM (that is, run *basicbring-up.py* again).
4. GPIO warnings or sysref errors usually indicate supply voltage or current limitations. Verify the power supply to the TRF1208-AFE7950-EVM and ensure a 5.5-V supply voltage and a 4-A current limit is used. Restart the Latte UI and rerun the scripts.

6.5 Modify Configuration

The examples in the previous sections show how to configure the AFE79xx with the default mode set in Latte scripts. The mode can be changed by modifying a set of parameters.

6.5.1 Data Rate and JESD Parameters

Data rates in the signal chain are often connected with the JESD mode (LMFS, SerDes rate), and a list of compatible modes are provided in the device data sheet. The following parameters in the *basicbring-up.py* script can be used to modify the configuration. Rerun the script after assigning new values to the following parameters.

```
## In below parameters, each element sets the particular LMFS-Hd for the particular channels.
# JESD and Serdes Parameters
sysParams.LMFSHdRx               = ["24410","24410","24410","24410"]
sysParams.LMFSHdFb               = ["22210","22210"]
sysParams.LMFSHdTx               = ["44210","44210","44210","44210"]
# Decimation and interpolation parameters for the data converter signal chains.
sysParams.ddcFactorRx               = [12,12,12,12]
sysParams.ddcFactorFb               = [6,6]
sysParams.ducFactorTx               = [6,6,6,6]
```

6.5.2 Data Converter Clocks Settings

This parameter is used to configure the data converter clocks and clock distribution path.

```
#Configures the reference input frequency to the on-chip PLL of the AFE7920.
sysParams.FRef     = 491.52
#Configures the RXADC converter sample rate.
sysParams.FadcRx   = 2949.12
#Configures the FBADC converter sample rate.
sysParams.FadcFb         = 2949.12
#Configures the TXDAC converter sample rate.
sysParams.Fdac     = 2949.12*3
#Sets the clock source for the RXADC converters. The source is now from the on-chip PLL.
sysParams.externalClockRx = False
#Sets the clock source for the TXDAC converters. The source is now from the on-chip PLL.
sysParams.externalClockTx = False
```

7 Setup the TSW14J5x With the HSDC Pro

This chapter is intended to serve as a quick-start guide for users not familiar with the TSW14J5x and the HSDC Pro GUI. See the *High Speed Data Converter Pro GUI User's Guide* for more details.

7.1 DAC Pattern Setup and Send

This section lists the steps to create and send a DAC pattern from the TSW14J5x board.

1. Click on the HSDC Pro DAC tab. Figure 7-1 shows a brief description of the DAC tab.

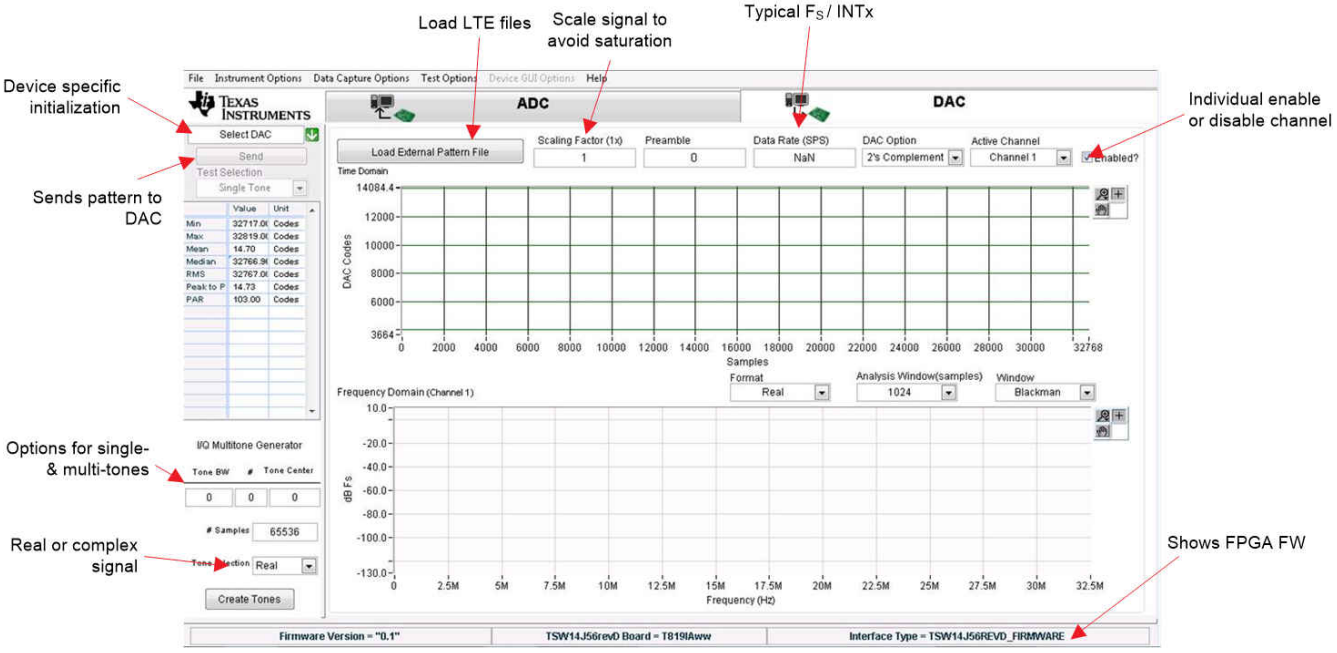

Figure 7-1. HSDC Pro DAC Tab Overview

2. A pictorial representation to create and send a sinusoid is shown in Figure 7-2.

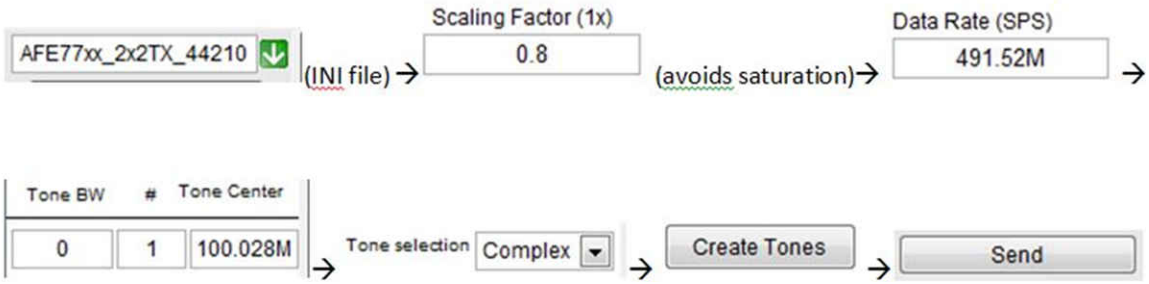

Figure 7-2. Setup a Sinusoid

3. How to create and send a sinusoid is outlined in the steps that follow:
   a. Select *AFE79xx_2x2TX_44210* in the device-specific initialization option. Click *Yes* if prompted to download the firmware (FW). The default option is to run the board in the transceiver mode of operation, which enables simultaneous operation of the TX and the RX and FBRX. The FW used in transceiver mode has the letters *XCVR* in its name.
   b. Enter *491.52 M* as the data rate and *0.9* for a scaling factor.
   c. Create a sinusoid by entering the frequency in the *Tone Generator* section of the HSDC Pro window.
   d. Press *Send* to transmit the DAC pattern to the TRF1208-AFE7950-EVM. Figure 7-3 shows the resulting message with the lane rate and reference clock expected in the FPGA. Click OK.

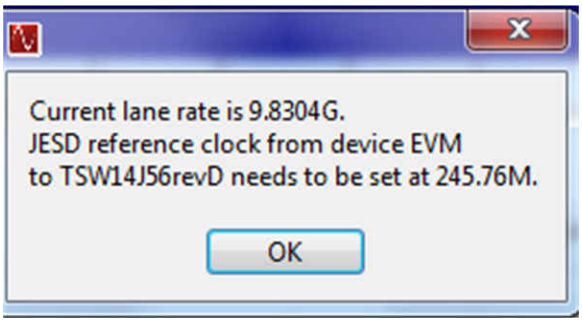

Figure 7-3. HSDC Pro Lane and Reference Clock Rate Pop-Up

Figure 7-4 shows an example setup with a 100-MHz sinusoid.

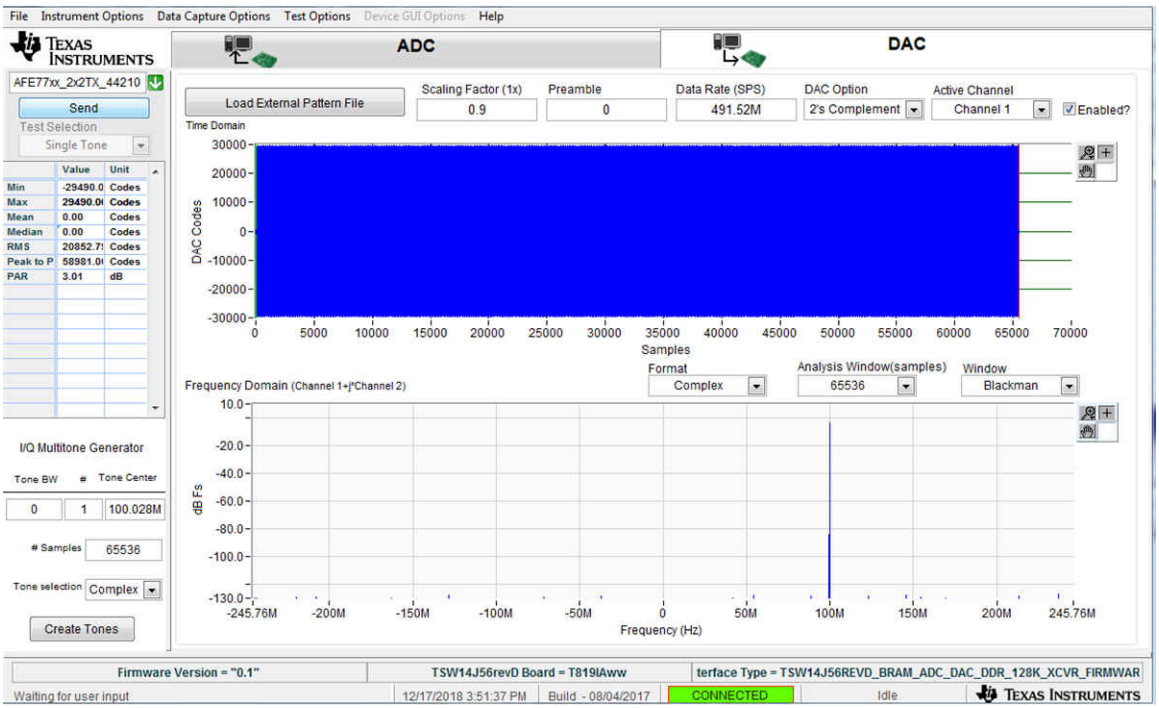

Figure 7-4. HSDC Pro CW

Alternately, a pattern file (for example, LTE) can be loaded and sent using the *Load External Pattern File* button.

The DAC setup is now complete.

7.2 DAC Synchronization Check

The steps for checking the DAC synchronization are as follows:

1. LED D2 on the TSW14J56 board blinks to indicate a successful JESD link on the DAC side.
2. If the LED is not blinking, then send the DAC pattern again.

7.3 ADC Data Capture

The steps to capture the ADC output are as follows:

1. Click on the HSDC Pro *ADC* tab. Figure 7-5 shows a brief description of the ADC tab.

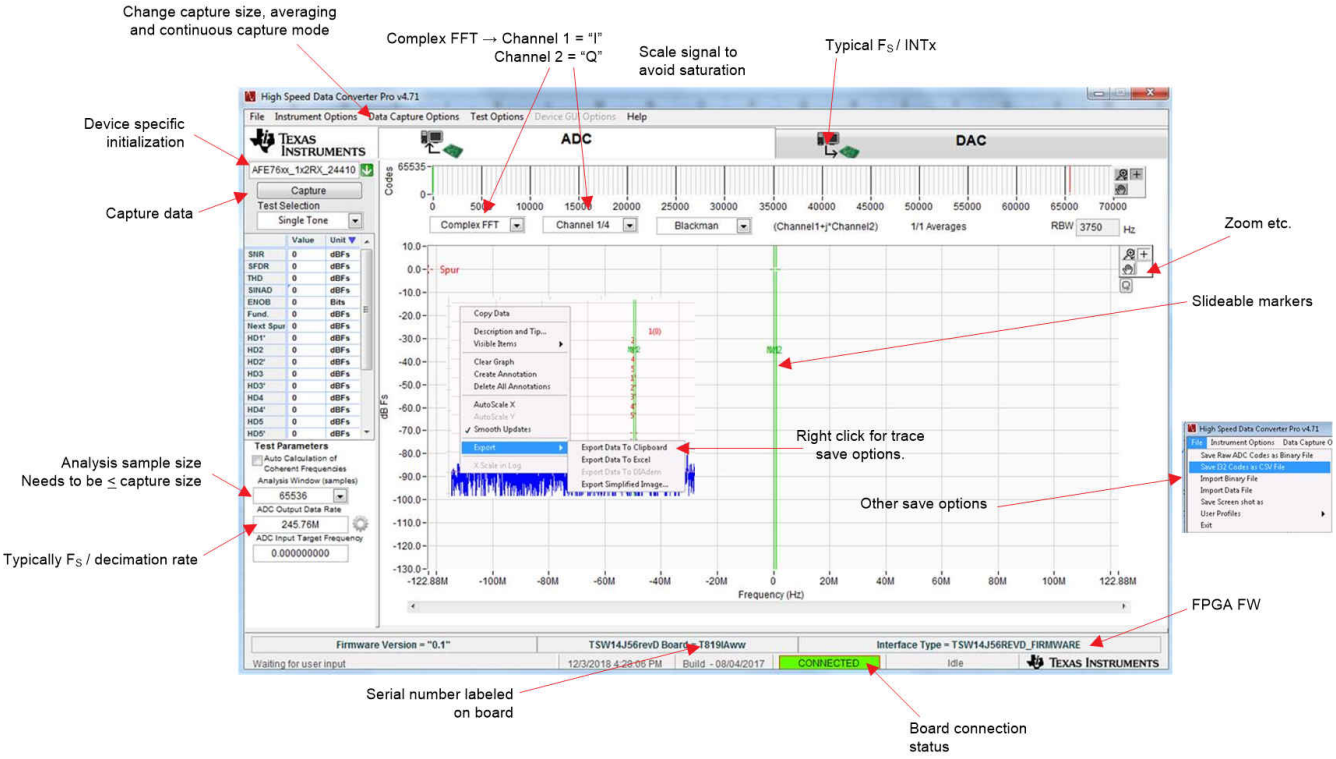

Figure 7-5. HSDC Pro ADC Tab Overview

2. Select *AFE79xx_2x2RX_24410* as the device.
3. Go to *Data Capture Options* in the menu bar and choose the *Capture* option. Set #samples (per channel) to 16384. Click the *OK* button.
4. Select *16384* in the *Analysis* window located in the lower left section of the GUI.
5. Enter *245.76 M* for ADC output data rate.
6. Click the *Capture* button.

The capture size is set to a lower value (such as 16K) because of the limited BRAM memory available in the FPGA.

7.4 ADC Synchronization Check

After a successful capture on the ADC side, LED D4 on the TSW14J56 board blinks to indicate a successful JESD link on the ADC side. The FFT output should also be seen. A timeout on the ADC capture indicates a unsuccessful bring-up of the AFE79xx. Try again after rerunning the AFE79xx configuration.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2022) to Revision A (January 2023)	Page
• Changed the part number from: *AFE7950-TRF1208-EVM* to: *TRF1208-AFE7950-EVM*	2

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