

# MOSFET - Power, Single N-Channel

100 V, 10.6 mΩ, 57.8 A

## NVTFWS010N10MCL

### Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVTFWS010N10MCLTAG – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	100	V
Gate-to-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJC</sub> (Notes 1, 2, 3)	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub> 57.8 A
		T <sub>C</sub> = 100°C	40.8
Power Dissipation R <sub>θJC</sub> (Notes 1, 2)	Steady State	T <sub>C</sub> = 25°C	P <sub>D</sub> 77.8 W
		T <sub>C</sub> = 100°C	38.9
Continuous Drain Current R <sub>θJA</sub> (Notes 1, 2, 3)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub> 11.7 A
		T <sub>A</sub> = 100°C	8.3
Power Dissipation R <sub>θJA</sub> (Notes 1, 2)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub> 3.2 W
		T <sub>A</sub> = 100°C	1.6
Pulsed Drain Current	T <sub>C</sub> = 25°C, t <sub>p</sub> = 10 μs	I <sub>DM</sub> 232	A
Source Current	I <sub>S</sub>	64.8	A
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 2.9 A)	E <sub>AS</sub>	526	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T <sub>L</sub>	260	°C

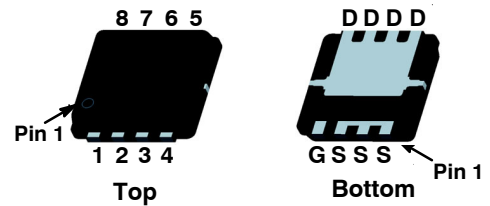
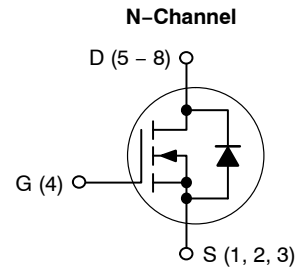
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

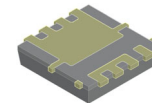
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	R <sub>θJC</sub>	1.93	°C/W
Junction-to-Ambient – Steady State (Note 2)	R <sub>θJA</sub>	46.6	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
100 V	10.6 mΩ @ 10 V	57.8 A
	15.9 mΩ @ 4.5 V	

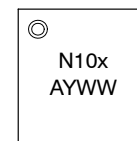


WDFN8  
(3.3x3.3, 0.65 P)  
CASE 511DY



WDFNW8  
(Full-Cut μ8FL Fused WF)  
CASE 515AP

### MARKING DIAGRAM



N10x = Specific Device Code  
x = L or W  
A = Assembly Location  
Y = Year Code  
WW = Work Week Code

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# NVTFS010N10MCL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			64		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 85\ \mu\text{A}$	1.0	1.5	3.0	V	
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-5.3		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}$		9.1	10.6	m $\Omega$
		$V_{GS} = 4.5\text{ V}$	$I_D = 12\text{ A}$		13.5	15.9	
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 15\text{ A}$		54		S	

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		1530	2150	pF
Output Capacitance	$C_{OSS}$			625	875	
Reverse Transfer Capacitance	$C_{RSS}$			10	18	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 50\text{ V}; I_D = 15\text{ A}$		10		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}; I_D = 15\text{ A}$		22	30	
Gate-to-Source Charge	$Q_{GS}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}; I_D = 15\text{ A}$		4.0		nC
Gate-to-Drain Charge	$Q_{GD}$			3.0		

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 15\text{ A}, R_G = 6\ \Omega$		9.0		ns
Rise Time	$t_r$			3.0		
Turn-Off Delay Time	$t_{d(OFF)}$			28		
Fall Time	$t_f$			5.0		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 15\text{ A}$		0.8	1.3	V
Reverse Recovery Time	$t_{RR}$	$I_F = 8\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		22	36	ns
Reverse Recovery Charge	$Q_{RR}$			35	56	nC
Reverse Recovery Time	$t_{RR}$	$I_F = 8\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$		17	30	ns
Reverse Recovery Charge	$Q_{RR}$			79	126	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

# NVTF5010N10MCL

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

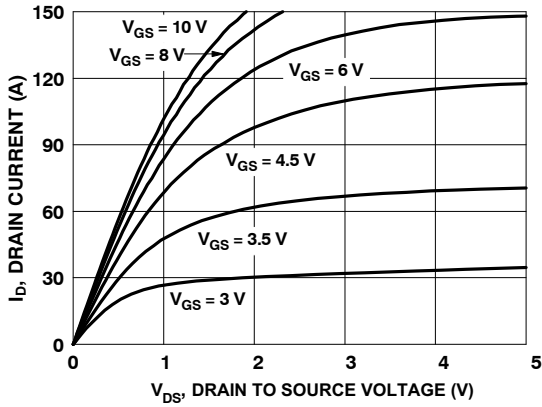


Figure 1. On Region Characteristics

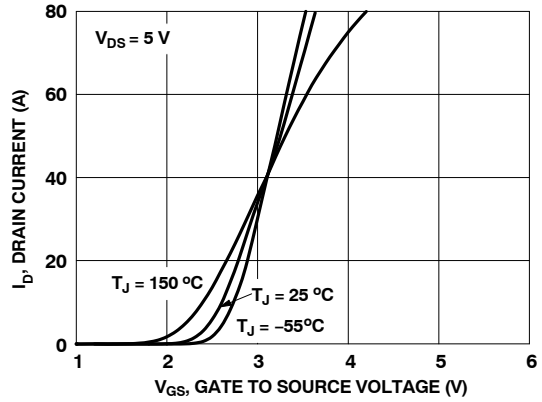


Figure 2. Transfer Characteristics

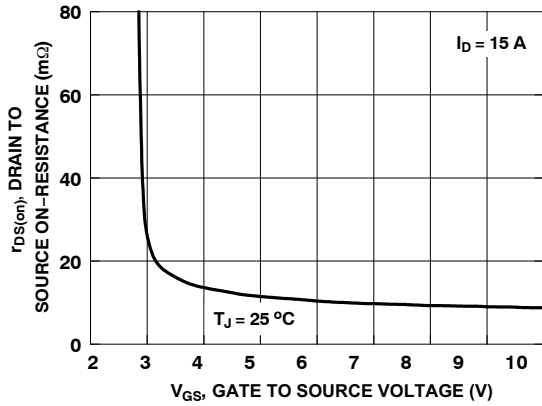


Figure 3. On-Resistance vs. Gate to Source Voltage

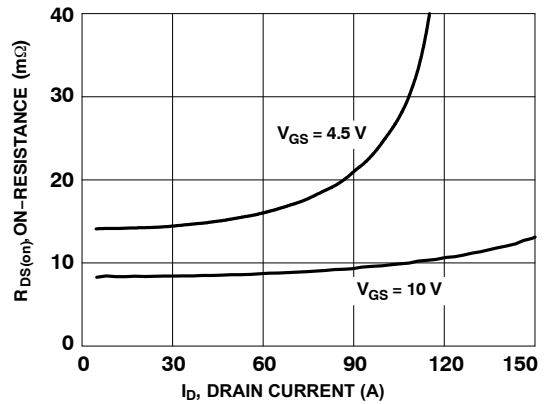


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

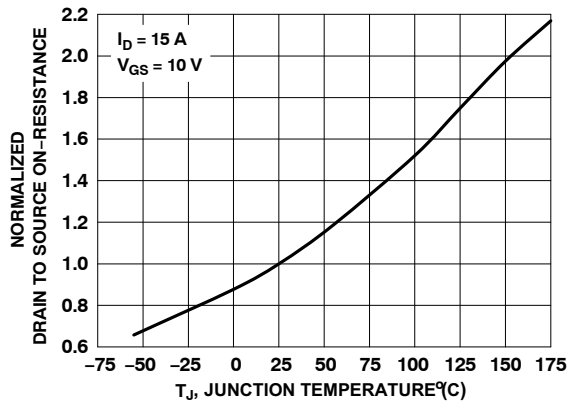


Figure 5. Normalized On Resistance vs. Junction Temperature

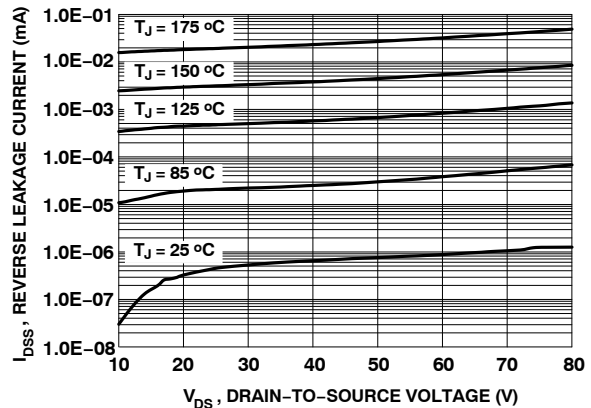


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVTFS010N10MCL

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

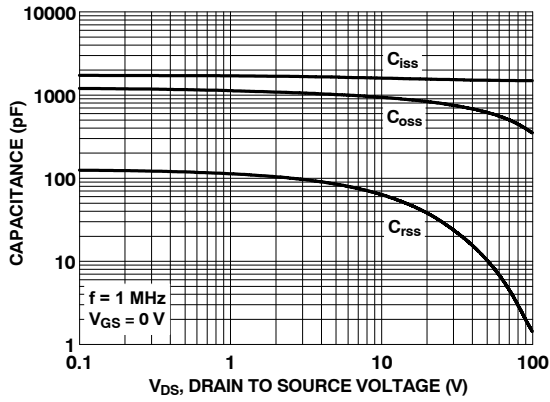


Figure 7. Capacitance vs. Drain to Source Voltage

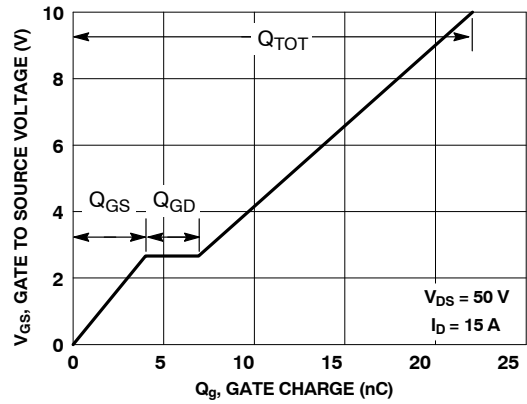


Figure 8. Gate Charge Characteristics

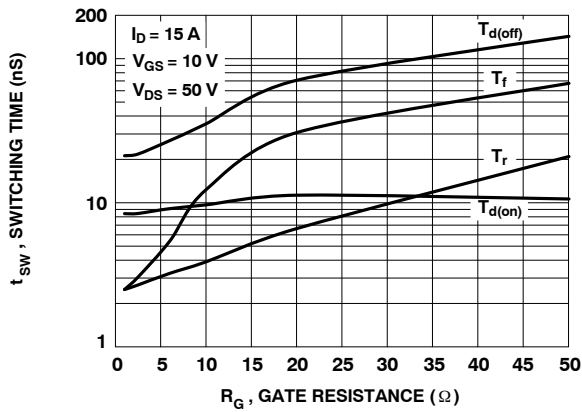


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

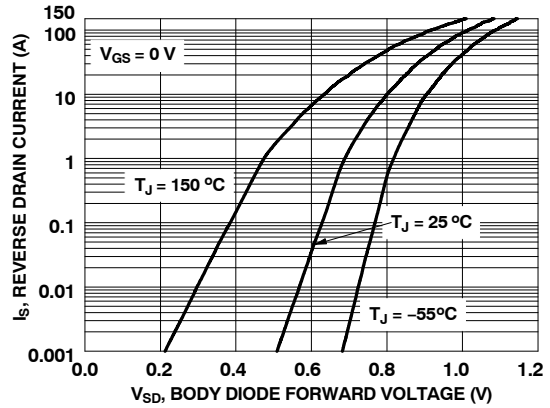


Figure 10. Source to Drain Diode Forward Voltage vs. Source Current

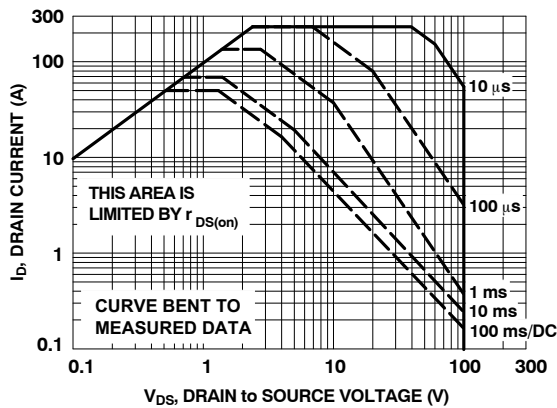


Figure 11. Forward Bias Safe Operating Area

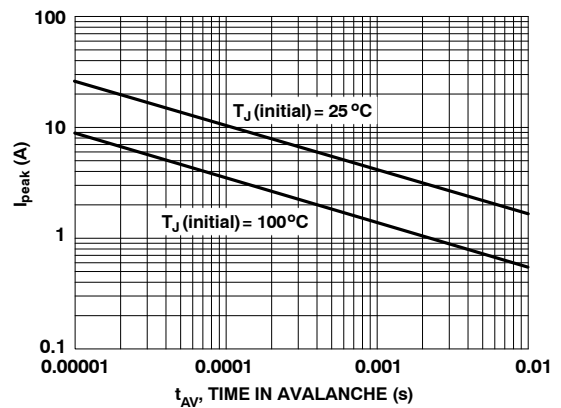


Figure 12. Unclamped Inductive Switching Capability

# NVTFS010N10MCL

## TYPICAL CHARACTERISTICS (CONTINUED)

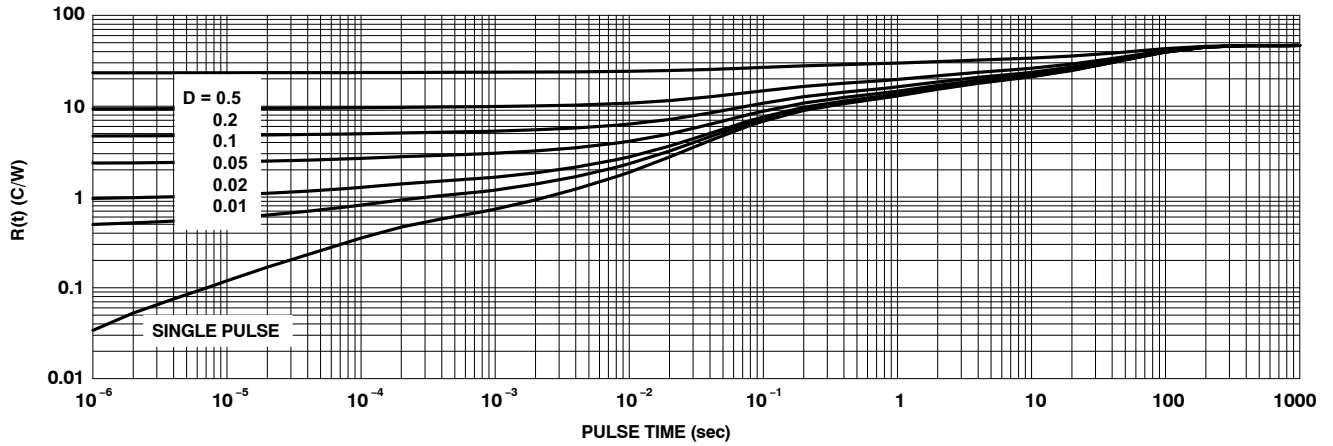


Figure 13. Junction-to-Case Transient Thermal Response Curve

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVTFS010N10MCLTAG	N10L	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFWS010N10MCLTAG	N10W	WDFNW8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

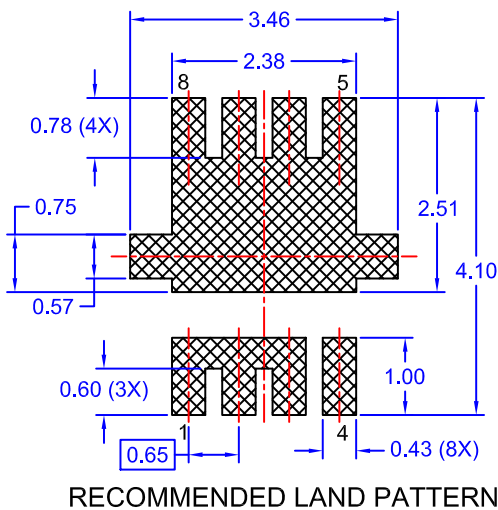
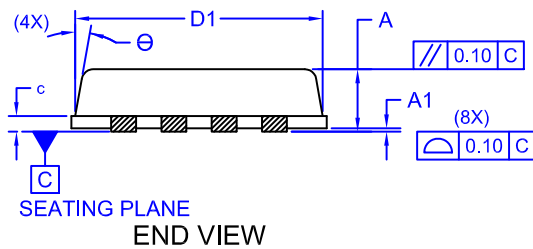
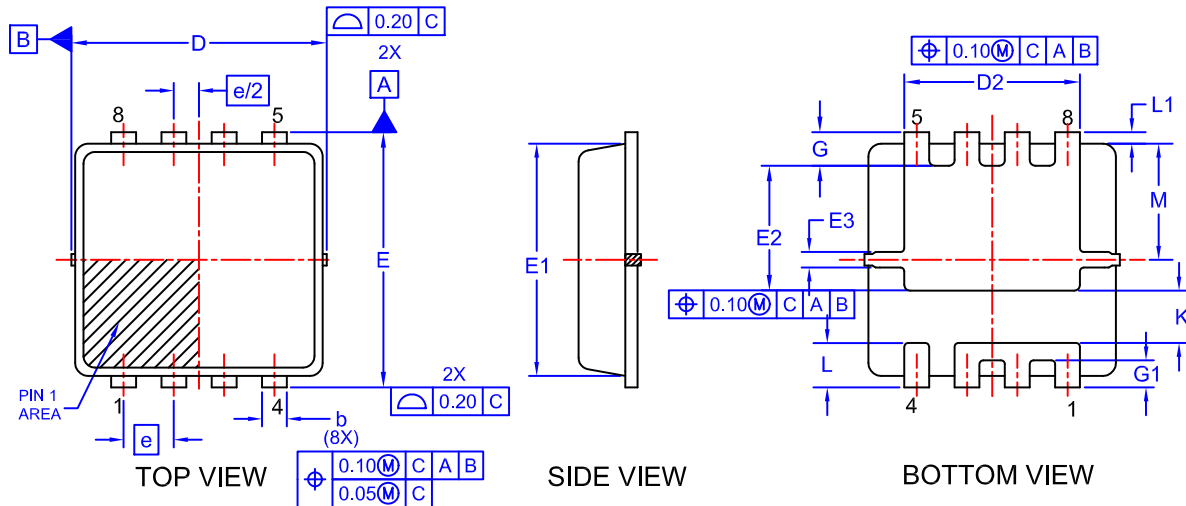
## PACKAGE DIMENSIONS

ON Semiconductor®



WDFN8 3.3x3.3, 0.65P  
CASE 511DY  
ISSUE A

DATE 21 AUG 2018

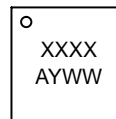


**NOTES:**

1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS D1 & E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
M	1.35	1.50	1.60
Θ	0	-	12

**GENERIC MARKING DIAGRAM\***



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year Code  
WW = Work Week Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

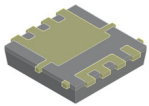
<b>DOCUMENT NUMBER:</b>	<b>98AON90827G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>WDFN8 3.3x3.3, 0.65P</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

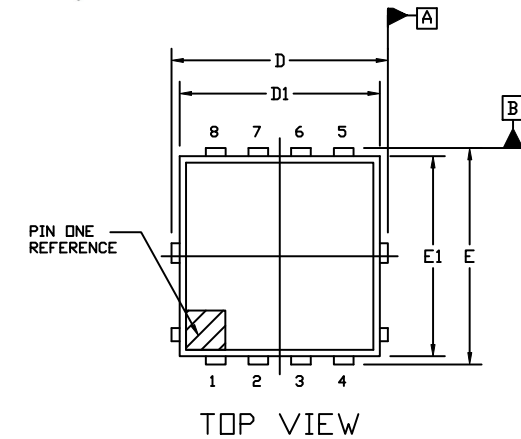


### WDFNW8 3.3x3.3, 0.65P (Full-Cut $\mu$ 8FL Fused WF) CASE 515AP ISSUE O

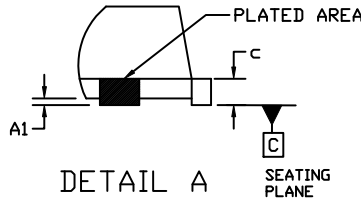
DATE 25 AUG 2020

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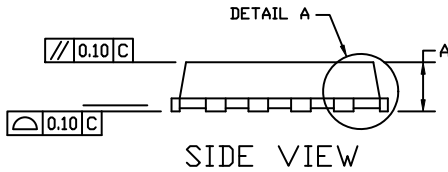
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



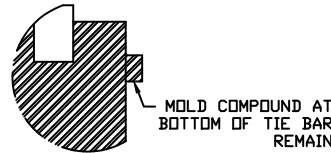
TOP VIEW



DETAIL A

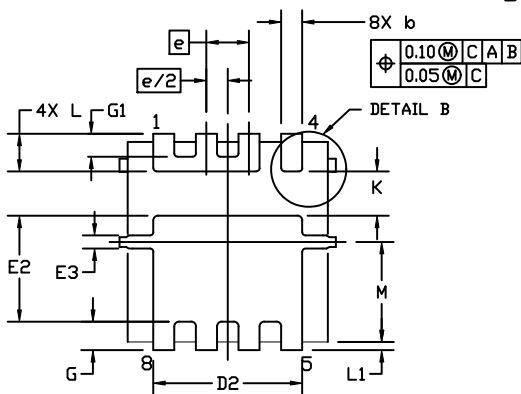


SIDE VIEW

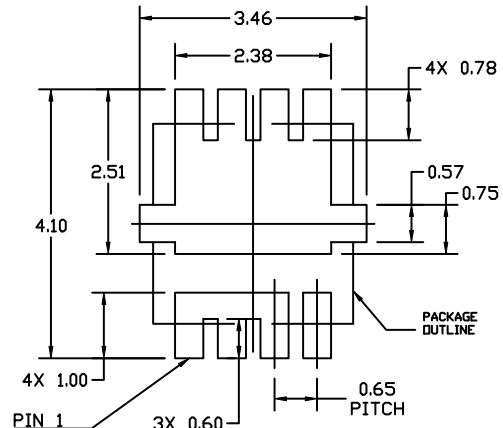


DETAIL B

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
M	1.35	1.50	1.60



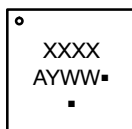
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

(Note: Microdot may be in either location)

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<b>DESCRIPTION:</b>	<b>WDFNW8 3.3x3.3, 0.65P (Full-Cut <math>\mu</math>8FL Fused WF)</b>	<b>PAGE 1 OF 1</b>

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