MOSFET - Power, Single N-Channel

100 V, 10.6 mΩ, 57.8 A

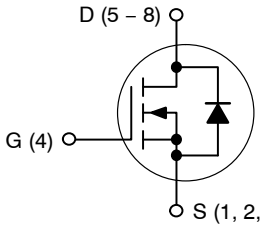
NVTFS010N10MCL

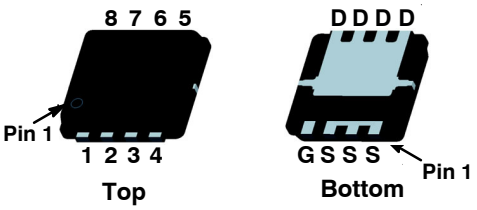
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
100 V	10.6 mΩ @ 10 V	57.8 A
	15.9 mΩ @ 4.5 V	

Features

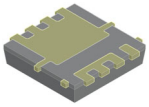
- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVTFWS010N10MCLTAG – Wettable Flanks Product
- AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free and are RoHS Compliant

N–Channel





WDFN8
(3.3x3.3, 0.65 P)
CASE 511DY



WDFNW8
(Full–Cut μ8FL Fused WF)
CASE 515AP

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	100	V
Gate–to–Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	T_C = 25°C	I_D	57.8	A
		T_C = 100°C		40.8	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)		T_C = 25°C	P_D	77.8	W
		T_C = 100°C		38.9	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	11.7	A
		T_A = 100°C		8.3	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.2	W
		T_A = 100°C		1.6	
Pulsed Drain Current	T_C = 25°C, t_p = 10 μs		I_{DM}	232	A
Source Current			I_S	64.8	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	–55 to +175	°C
Single Pulse Drain–to–Source Avalanche Energy ($I_{L(pk)}$ = 2.9 A)			E_{AS}	526	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

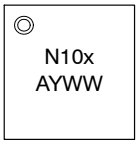
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction–to–Case – Steady State (Note 2)	$R_{\theta JC}$	1.93	°C/W
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	46.6	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface–mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



N10x = Specific Device Code
x = L or W
A = Assembly Location
Y = Year Code
WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		100			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				64		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	T_J = 25°C			1.0	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 85 μA		1.0	1.5	3.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−5.3		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 15 A		9.1	10.6	mΩ
		V_{GS} = 4.5 V	I_D = 12 A		13.5	15.9	
Forward Transconductance	g_{FS}	V_{DS} =5 V, I_D = 15 A			54		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 50 V			1530	2150	pF
Output Capacitance	C_{OSS}				625	875	
Reverse Transfer Capacitance	C_{RSS}				10	18	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 50 V; I_D = 15 A			10		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 50 V; I_D = 15 A			22	30	
Gate−to−Source Charge	Q_{GS}	V_{GS} = 10 V, V_{DS} = 50 V; I_D = 15 A			4.0		nC
Gate−to−Drain Charge	Q_{GD}				3.0		
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 15 A, R_G = 6 Ω			9.0		ns
Rise Time	t_r				3.0		
Turn−Off Delay Time	$t_{d(OFF)}$				28		
Fall Time	t_f				5.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 15 A			0.8	1.3	V
Reverse Recovery Time	t_{RR}	I_F = 8 A, di/dt = 300 A/μs			22	36	ns
Reverse Recovery Charge	Q_{RR}				35	56	nC
Reverse Recovery Time	t_{RR}	I_F = 8 A, di/dt = 1000 A/μs			17	30	ns
Reverse Recovery Charge	Q_{RR}				79	126	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS (T_J = 25°C UNLESS OTHERWISE NOTED)

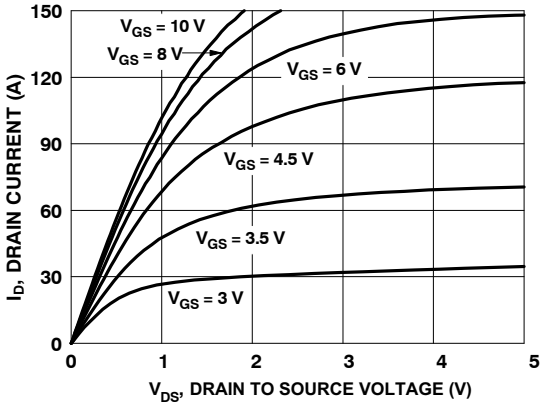


Figure 1. On Region Characteristics

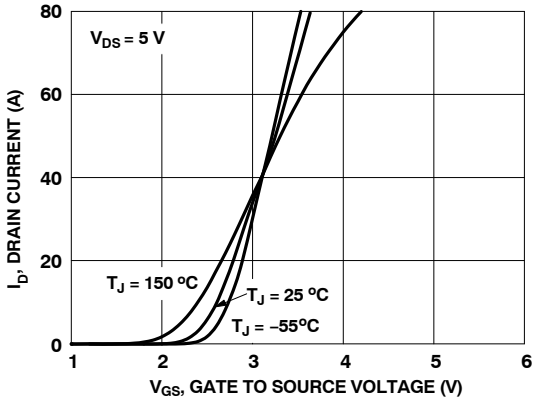


Figure 2. Transfer Characteristics

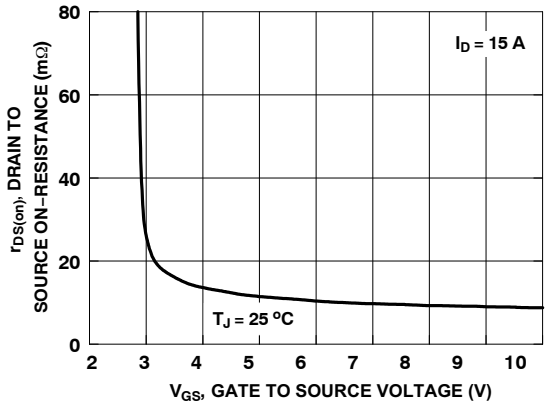


Figure 3. On-Resistance vs. Gate to Source Voltage

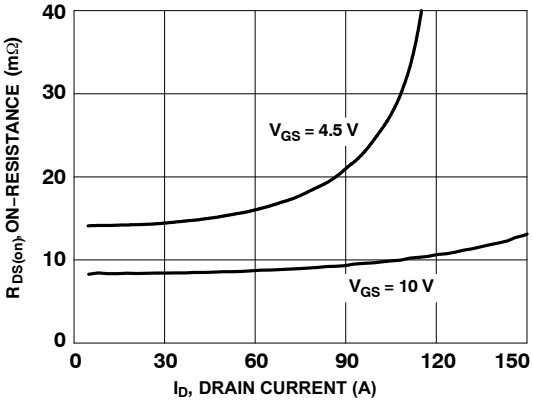


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

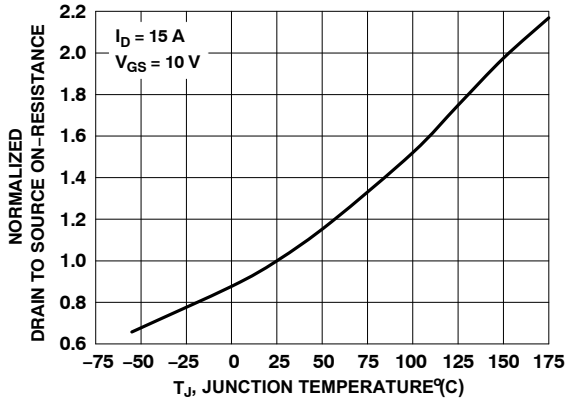


Figure 5. Normalized On Resistance vs. Junction Temperature

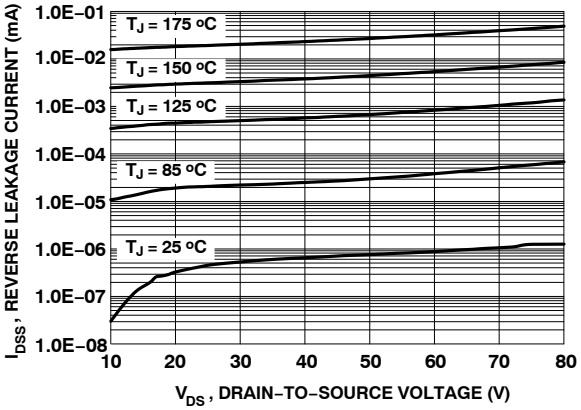


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (T_J = 25°C UNLESS OTHERWISE NOTED)

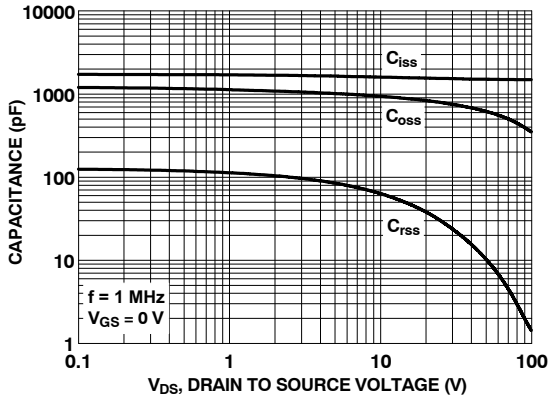


Figure 7. Capacitance vs. Drain to Source Voltage

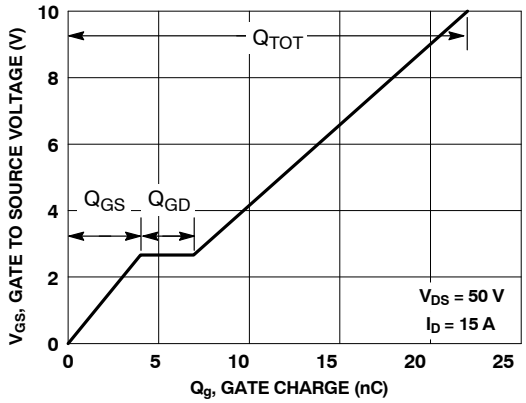


Figure 8. Gate Charge Characteristics

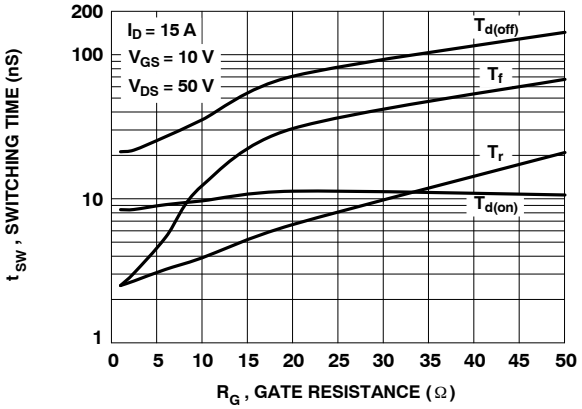


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

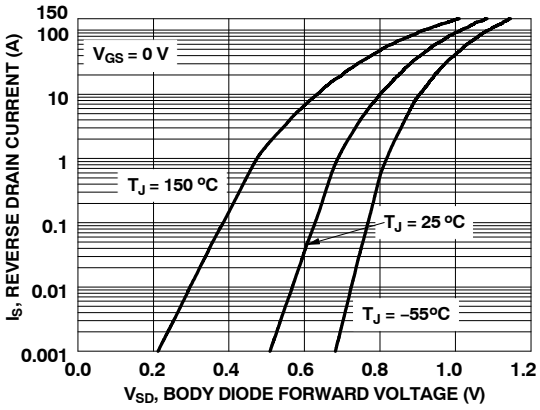


Figure 10. Source to Drain Diode Forward Voltage vs. Source Current

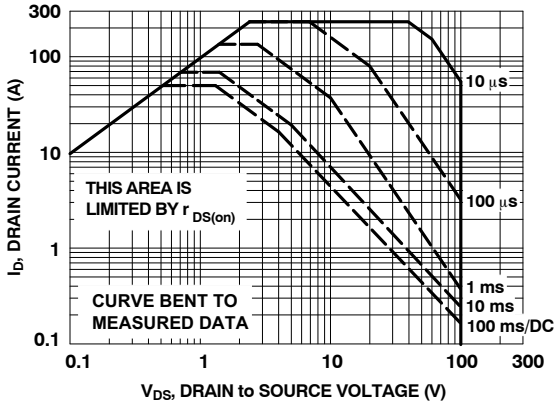


Figure 11. Forward Bias Safe Operating Area

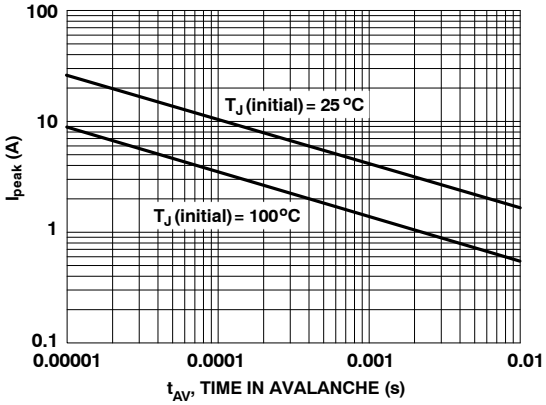


Figure 12. Unclamped Inductive Switching Capability

TYPICAL CHARACTERISTICS (CONTINUED)

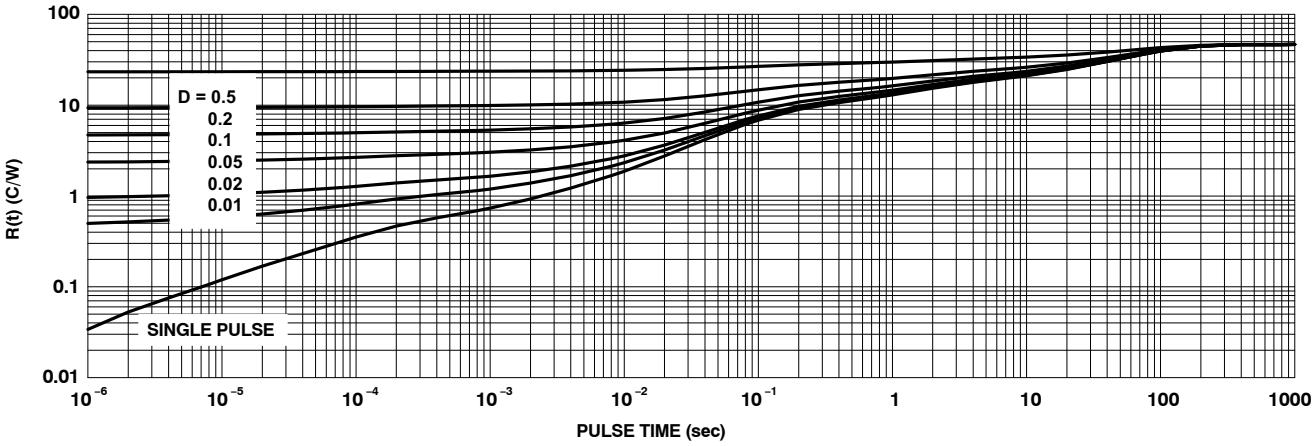


Figure 13. Junction−to−Case Transient Thermal Response Curve

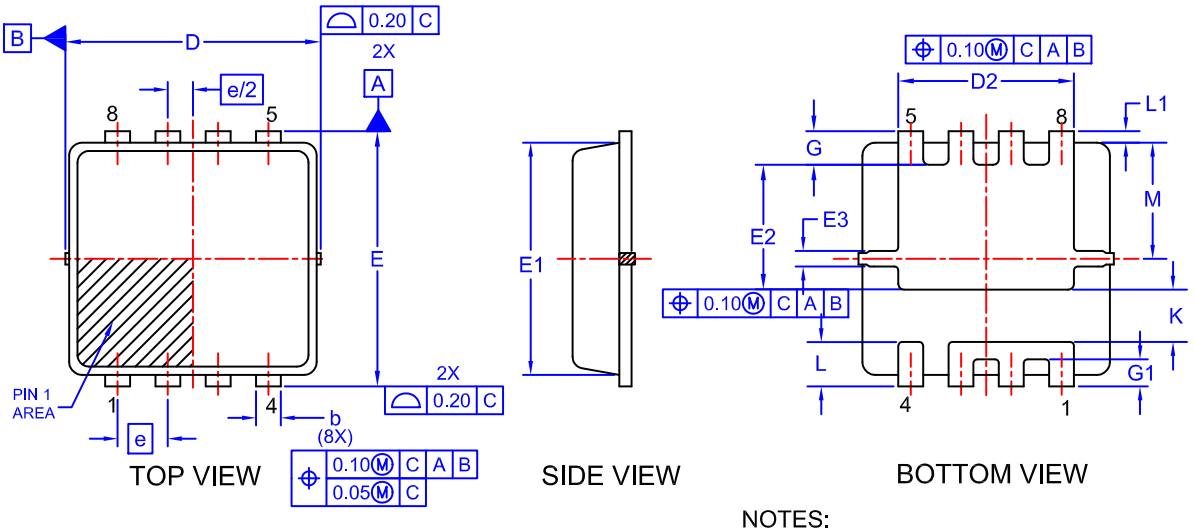
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVTFS010N10MCLTAG	N10L	WDFN8 (Pb−Free)	1500 / Tape & Reel
NVTFWS010N10MCLTAG	N10W	WDFNW8 (Pb−Free, Wettable Flanks)	1500 / Tape & Reel

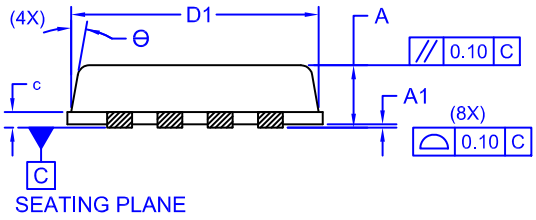
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WDFN8 3.3x3.3, 0.65P
CASE 511DY
ISSUE A

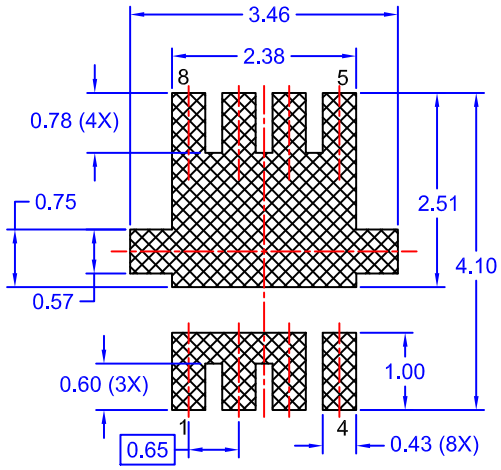
DATE 21 AUG 2018



NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS D1 & E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
M	1.35	1.50	1.60
Θ	0	-	12



GENERIC MARKING DIAGRAM*

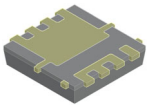
XXXX = Specific Device Code
A = Assembly Location
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON90827G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**WDFN8 3.3x3.3, 0.65P**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

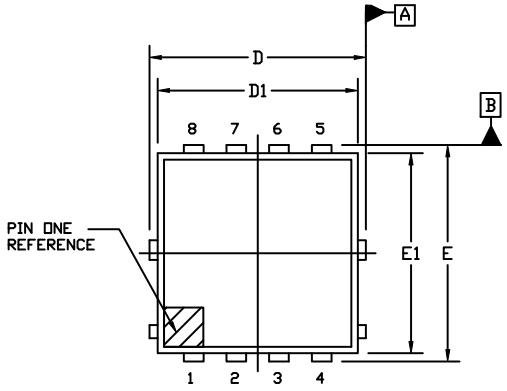
ON Semiconductor®



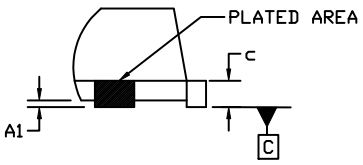
WDFNW8 3.3x3.3, 0.65P (Full−Cut μ8FL Fused WF)
CASE 515AP
ISSUE O

DATE 25 AUG 2020

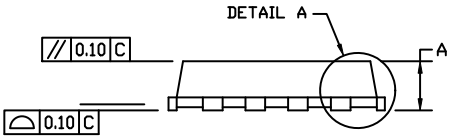
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



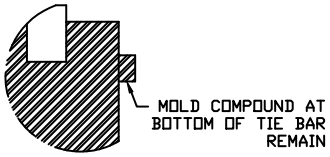
TOP VIEW



DETAIL A

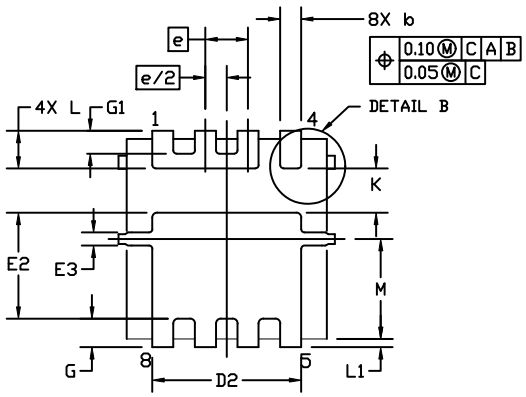


SIDE VIEW

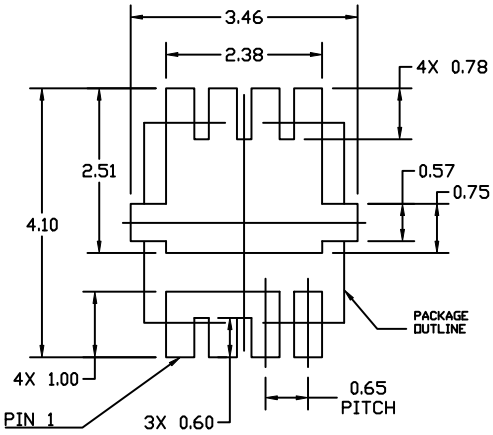


DETAIL B

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
M	1.35	1.50	1.60



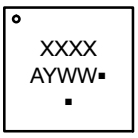
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON24557H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**WDFNW8 3.3x3.3, 0.65P (Full−Cut μ8FL Fused WF)**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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