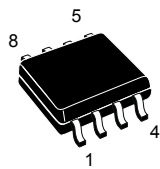
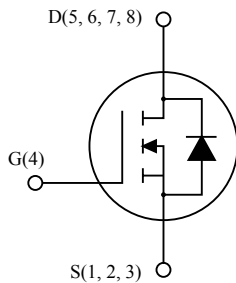



Automotive-grade N-channel 60 V, 21 mΩ typ., 8 A STripFET F6 Power MOSFET in an SO-8 package


SO-8


AM01475v3

Features

| Order code | V_{DS} | $R_{DS(on)}$ max. | I_D | P_{TOT} |
|-------------|----------|-------------------|-------|-----------|
| STS8N6LF6AG | 60 V | 24 mΩ | 8 A | 3.2 W |

- AEC-Q101 qualified 
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Logic level

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.



Product status link

[STS8N6LF6AG](#)

Product summary

| | |
|-------------------|---------------|
| Order code | STS8N6LF6AG |
| Marking | 8N6LF6 |
| Package | SO-8 |
| Packing | Tape and reel |

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---------------------------------------------------------------------|------------|------------------|
| V_{DS} | Drain-source voltage | 60 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$ | 8 | A |
| | Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$ | 5.8 | |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 32 | A |
| P_{TOT} | Total power dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$ | 3.2 | W |
| T_{stg} | Storage temperature range | -55 to 175 | $^\circ\text{C}$ |
| T_J | Operating junction temperature range | | $^\circ\text{C}$ |

1. When mounted on a 1-inch² FR-4, 2 Oz copper board, $t < 10\text{ s}$.
2. Pulse width is limited by safe operating area.

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|------------------|-----------------------------------------|-------|---------------------------|
| $R_{thJA}^{(1)}$ | Thermal resistance, junction-to-ambient | 47 | $^\circ\text{C}/\text{W}$ |

1. When mounted on an 1-inch² FR-4, 2 Oz copper board, $t < 10\text{ s}$.

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------------|-----------------------------------|-------|------|
| I_{AV} | Avalanche current, not repetitive | 6 | A |
| $E_{AS}^{(1)}$ | Single pulse avalanche energy | 72 | mJ |

1. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 43.5\text{ V}$.

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. Static

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|--------------------------------------------------------|------|------|-----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$ | 60 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 60\text{ V}$ | | | 1 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 1 | | 2.5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 4\text{ A}$ | | 21 | 24 | m Ω |
| | | $V_{GS} = 4.5\text{ V}$, $I_D = 4\text{ A}$ | | 22 | 26 | |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|--------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 1340 | - | pF |
| C_{oss} | Output capacitance | | - | 90 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 60 | - | pF |
| Q_g | Total gate charge | $V_{DD} = 30\text{ V}$, $I_D = 8\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior) | - | 27 | - | nC |
| Q_{gs} | Gate-source charge | | - | 4.6 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 4.3 | - | nC |

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 30\text{ V}$, $I_D = 4\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ | - | 9.6 | - | ns |
| t_r | Rise time | | - | 20 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 56 | - | ns |
| t_f | Fall time | | - | 7 | - | ns |

Table 7. Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|-------------------------------------------------------------------------------------|------|------|------|------|
| I_{SD} | Source-drain current | | - | | 8 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 32 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS} = 0\text{ V}$, $I_{SD} = 8\text{ A}$ | - | | 1.3 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, | - | 22.5 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 48\text{ V}$, $T_J = 25\text{ °C}$ | - | 22.2 | | nC |
| I_{RRM} | Reverse recovery current | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 2.0 | | A |

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

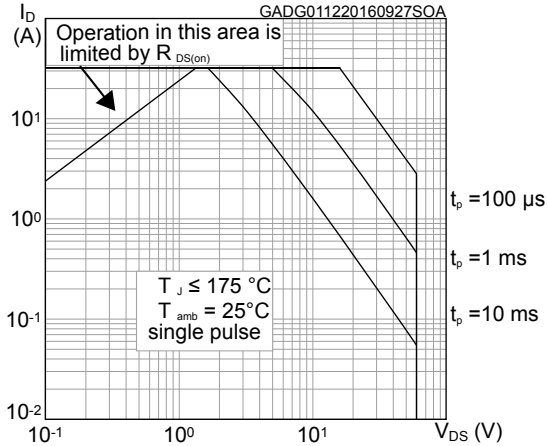


Figure 2. Thermal impedance

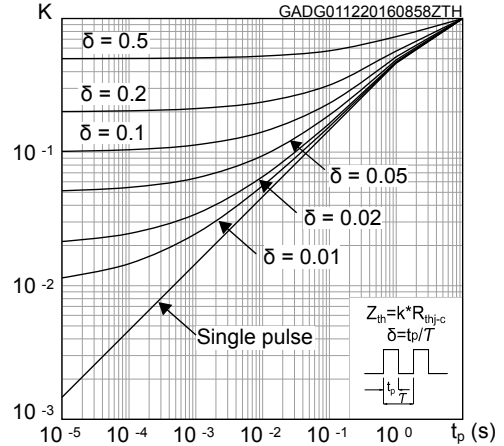


Figure 3. Output characteristics

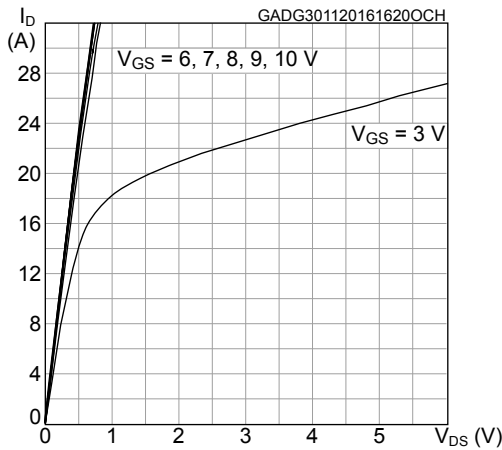


Figure 4. Transfer characteristics

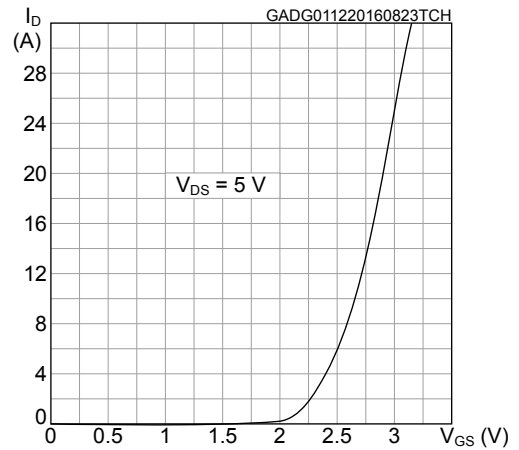


Figure 5. Gate charge vs gate-source voltage

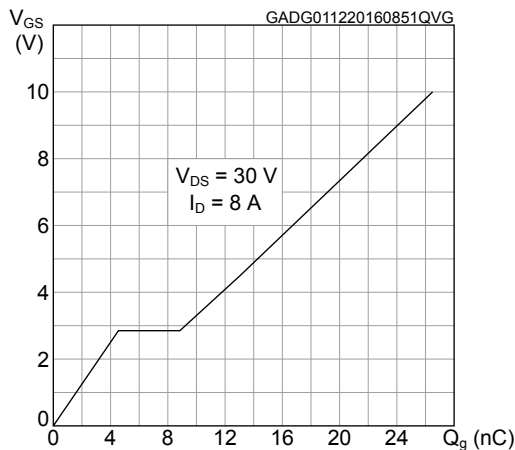


Figure 6. Static drain-source on-resistance

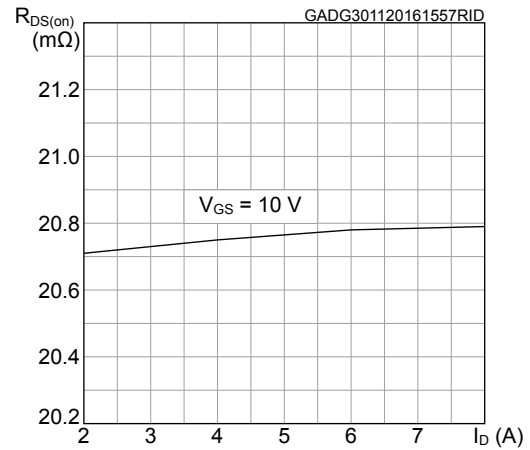


Figure 7. Capacitance variations

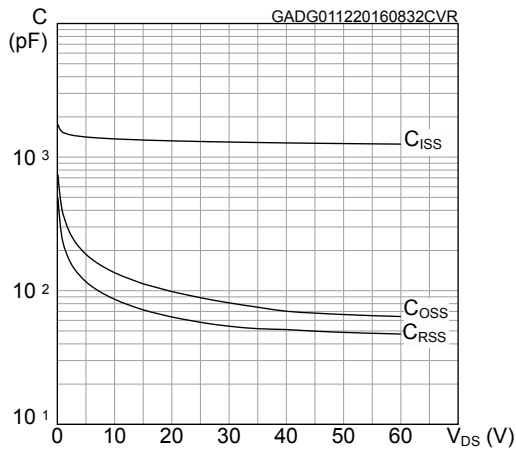


Figure 8. Normalized gate threshold voltage vs temperature

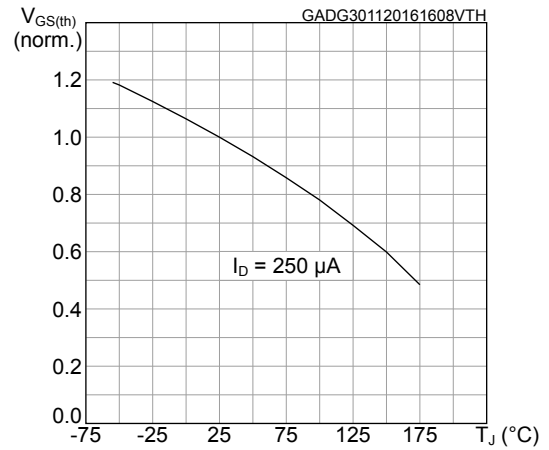


Figure 9. Normalized on-resistance vs temperature

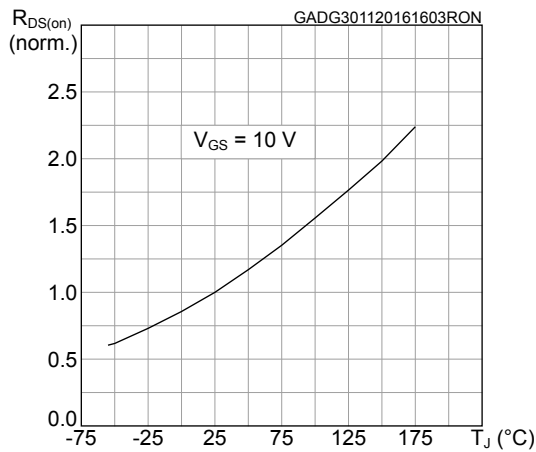


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

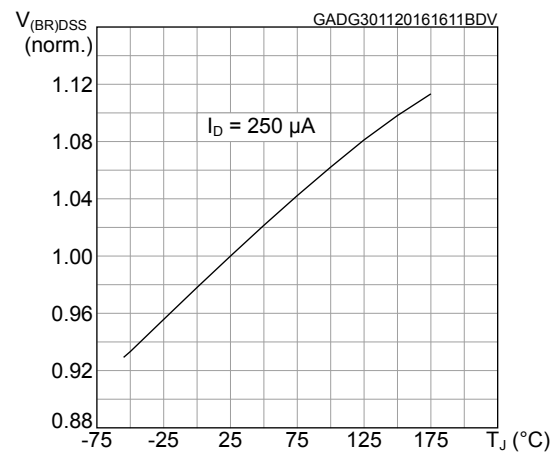
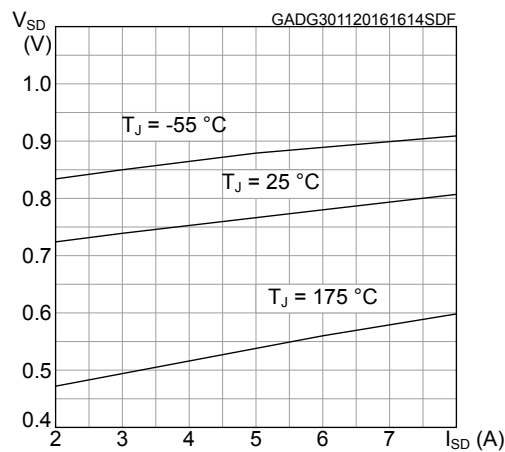
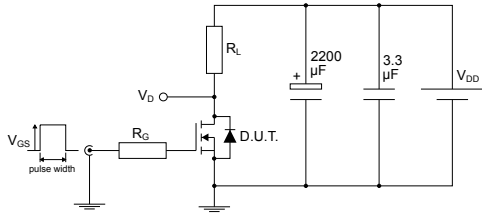


Figure 11. Source-drain diode forward characteristics



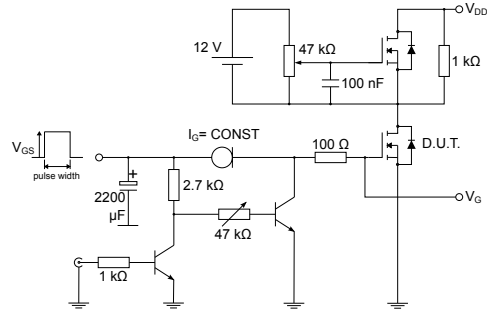
3 Test circuits

Figure 12. Test circuit for resistive load switching times



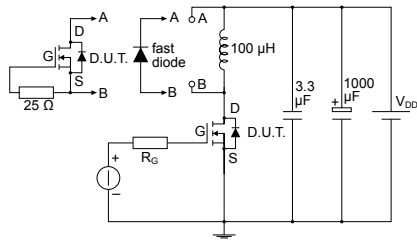
AM01468v1

Figure 13. Test circuit for gate charge behavior



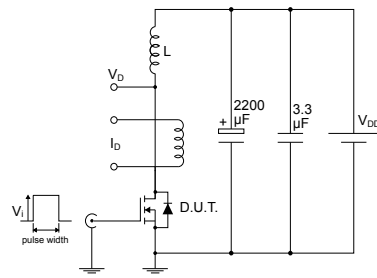
AM01469v1

Figure 14. Test circuit for inductive load switching and diode recovery times



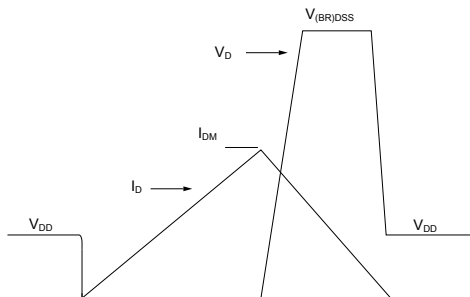
AM01470v1

Figure 15. Unclamped inductive load test circuit



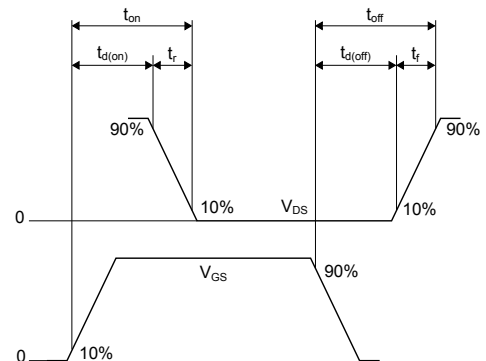
AM01471v1

Figure 16. Unclamped inductive waveform



AM01472v1

Figure 17. Switching time waveform



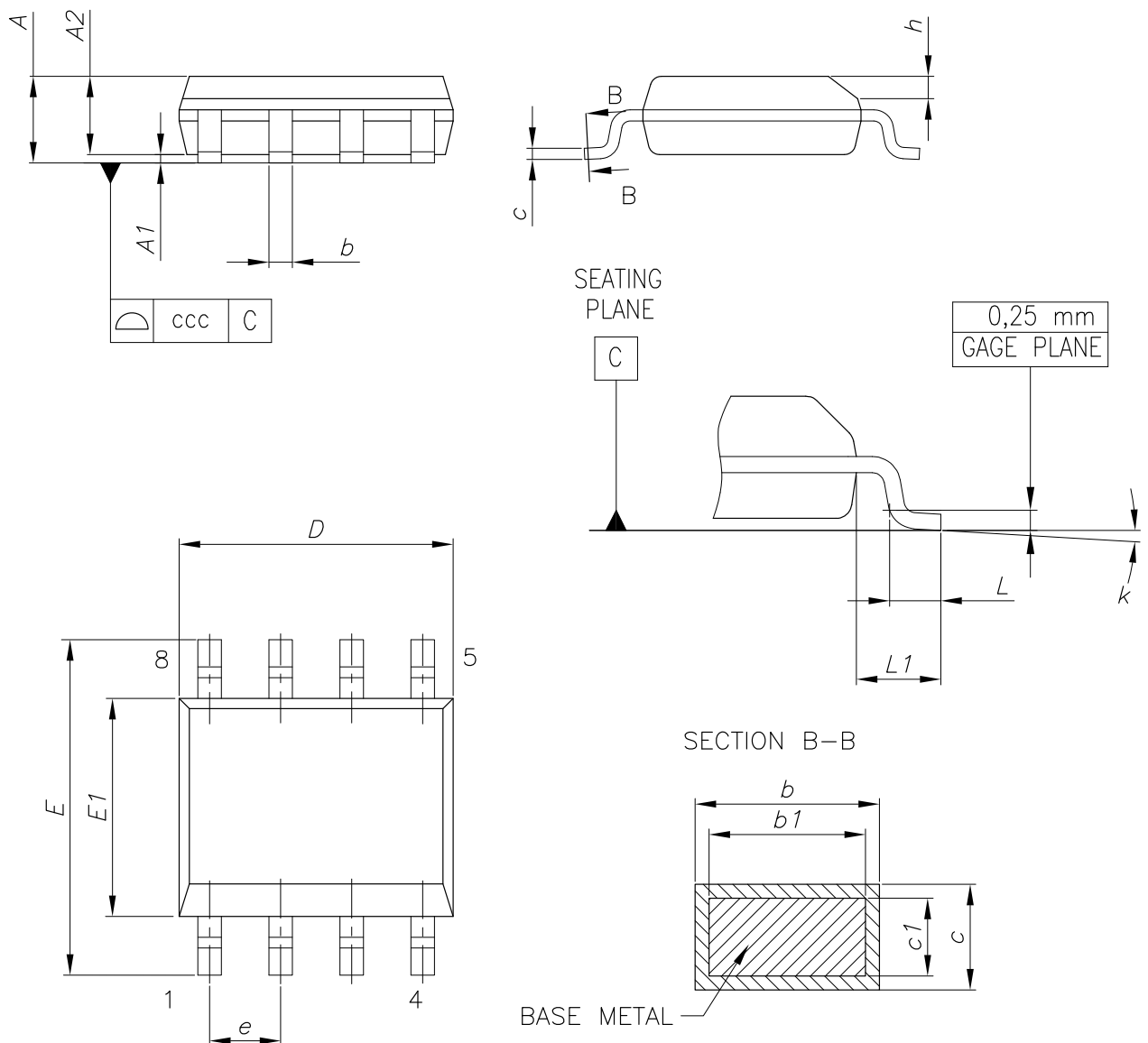
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SO-8 package information

Figure 18. SO-8 package outline

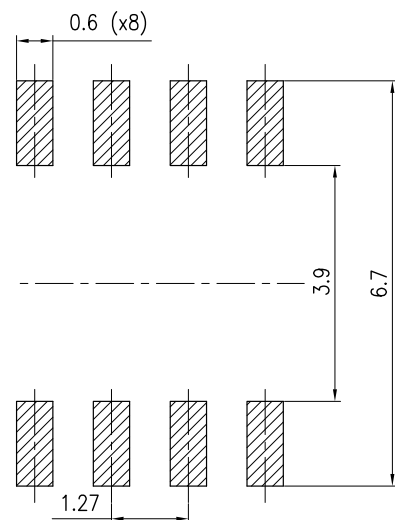


0016023_So-807_fig2_Rev10

Table 8. SO-8 mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | |
| b | 0.31 | | 0.51 |
| b1 | 0.28 | | 0.48 |
| c | 0.10 | | 0.25 |
| c1 | 0.10 | | 0.23 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| L1 | | 1.04 | |
| L2 | | 0.25 | |
| k | 0° | | 8° |
| ccc | | | 0.10 |

Figure 19. SO-8 recommended footprint (dimensions are in mm)



0016023_So-807_footprint_Rev10

4.2 SO-8 packing information

Figure 20. SO-8 tape and reel dimensions

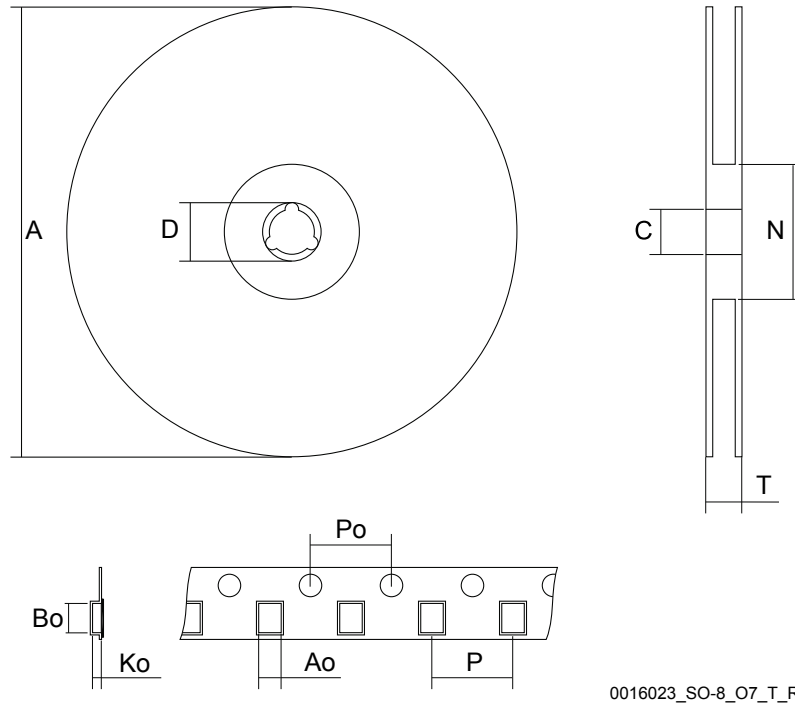


Figure 21. Tape orientation

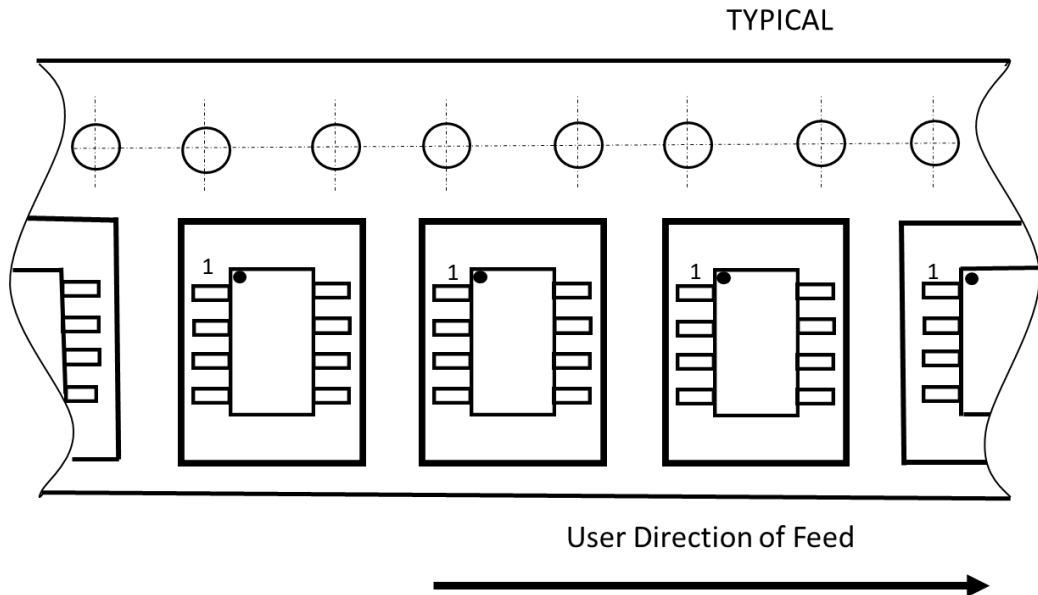


Table 9. SO-8 tape and reel mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | | | 330 |
| C | 12.8 | | 13.2 |
| D | 20.2 | | |
| N | 60 | | |
| T | | | 22.4 |
| Ao | 6.5 | - | 6.7 |
| Bo | 5.4 | | 5.6 |
| Ko | 2.0 | | 2.2 |
| Po | 3.9 | | 4.1 |
| P | 7.9 | | 8.1 |

Revision history

Table 10. Document revision history

| Date | Version | Changes |
|-------------|---------|-----------------------------------------------------------------------------------------------------|
| 24-Jan-2017 | 1 | First release. |
| 08-Mar-2021 | 2 | Updated Internal schematic. Updated Section 4.2 SO-8 packing information. Minor text changes. |
| 21-Jul-2021 | 3 | Updated Section Internal schematic. |

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