

Common Anode Silicon Dual Switching Diodes

DAP222M3T5G

These Common Anode Silicon Epitaxial Planar Dual Diodes are designed for use in ultra high speed switching applications. The DAP222 device is housed in the SOT-723 package which is designed for low power surface mount applications, where board space is at a premium.

Features

- Fast t_{rr}
- Low C_D
- Available in 4 mm Tape and Reel
- This is a Pb-Free Device

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	80	V
Peak Reverse Voltage	V_{RM}	80	V
Forward Current	I_F	100	mA

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Power Dissipation	P_D	260	mW
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 ~ +150	$^\circ\text{C}$

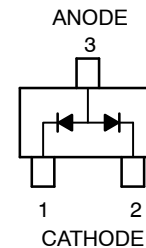
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $t = 1.0 \mu\text{s}$.

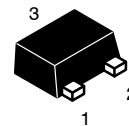


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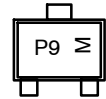
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MARKING DIAGRAM



SOT-723
CASE 631AA
STYLE 4



P9 = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
DAP222M3T5G	SOT-723 (Pb-Free)	8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

DAP222M3T5G

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	Condition	Min	Max	Unit
Reverse Voltage Leakage Current	I _R	V _R = 70 V	-	0.1	μA
Forward Voltage	V _F	I _F = 100 mA	-	1.2	V
Reverse Breakdown Voltage	V _R	I _R = 100 μA	80	-	V
Diode Capacitance	C _D	V _R = 6.0 V, f = 1.0 MHz	-	3.5	pF
Reverse Recovery Time	t _{rr} (Note 2)	I _F = 5.0 mA, V _R = 6.0 V, R _L = 100 Ω, I _{rr} = 0.1 I _R	-	4.0	ns

2. t_{rr} Test Circuit for DAP222 in Figure 4.

TYPICAL ELECTRICAL CHARACTERISTICS

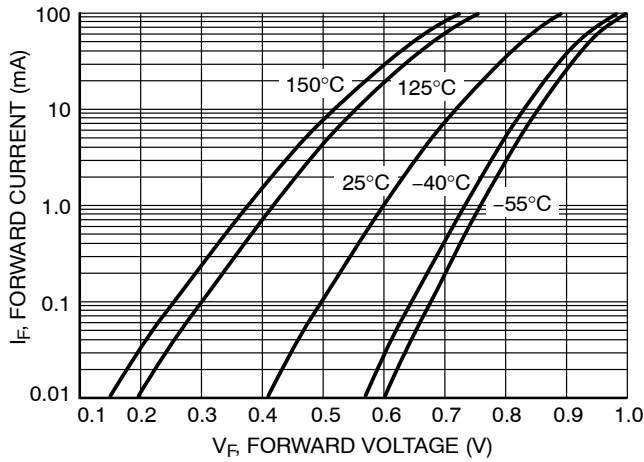


Figure 1. Forward Voltage

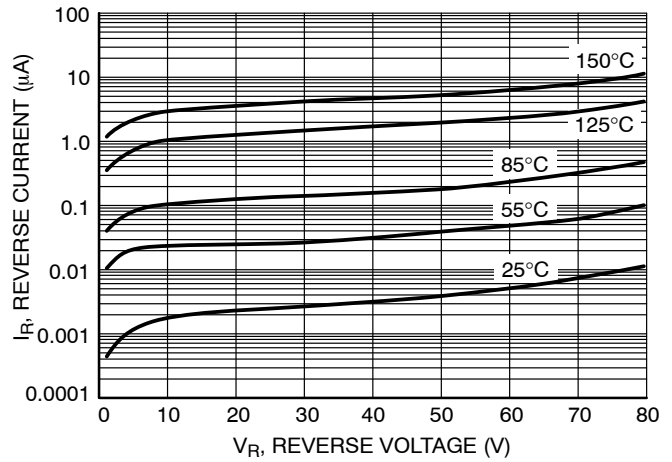


Figure 2. Reverse Current

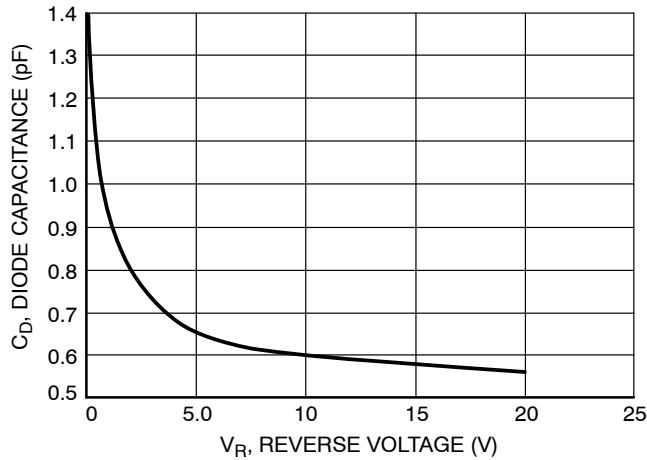
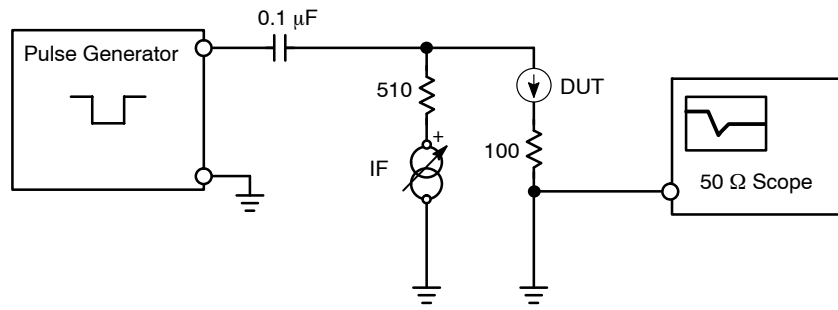
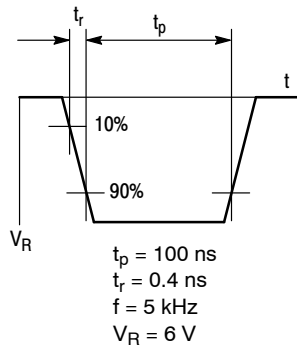


Figure 3. Diode Capacitance

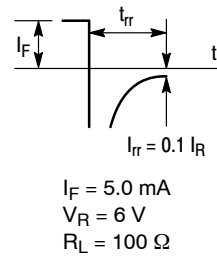
DAP222M3T5G



RECOVERY TIME EQUIVALENT TEST CIRCUIT



INPUT PULSE



OUTPUT PULSE

Figure 4. Reverse Recovery Time Test Circuit

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

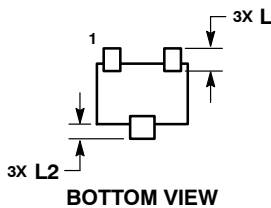
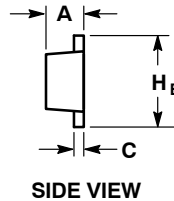
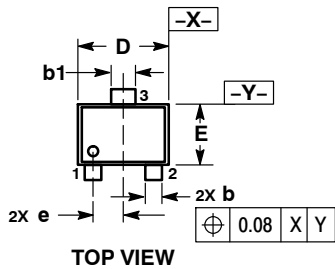
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SCALE 4:1

SOT-723
CASE 631AA-01
ISSUE D

DATE 10 AUG 2009

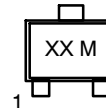


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
b	0.15	0.21	0.27
b1	0.25	0.31	0.37
C	0.07	0.12	0.17
D	1.15	1.20	1.25
E	0.75	0.80	0.85
e	0.40 BSC		
H E	1.15	1.20	1.25
L	0.29 REF		
L2	0.15	0.20	0.25

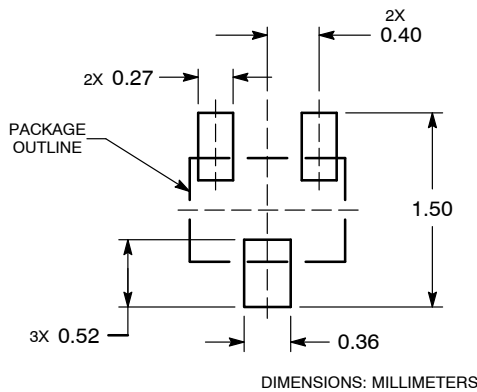
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

- | | | | | |
|---|--|--|--|--|
| STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE | STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE | STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN |
|---|--|--|--|--|

RECOMMENDED SOLDERING FOOTPRINT*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	SOT-723	PAGE 1 OF 1

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