PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-IPC/14/8692
Dated 03 Oct 2014

Micro Leadframe Package conversion to High Density Leadframe in CARSEM sites

Table 1. Change Implementation Schedule

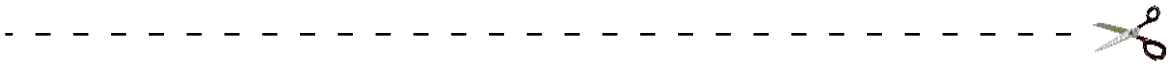
Forecasted implementation date for change	15-Nov-2014
Forecasted availability date of samples for customer	20-Oct-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	26-Sep-2014
Estimated date of changed product first shipment	02-Jan-2015

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached
Type of change	Package assembly material change
Reason for change	To harmonize the Bill of Material as used in CARSEM sites.
Description of the change	Micro Lead-frame Package (MLP) built on standard Lead-frame will be converted to High Density Lead-frame (HDL) on products assembled in package FPN3*3, 4*4 in Carsem Ipoh and FPN 5*5 in CARSEM Suzhou. Impacted packaged products with HDL will also use the improved dedicated molding compound (G770HCD). Combination of HDL and GC770HCD has been already qualified and it is running in production on similar product/packages.
Change Product Identification	By a new Finished Goods code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-IPC/14/8692**
Please sign and return to STMicroelectronics Sales Office	**Dated 03 Oct 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Arrigo, Domenico Massimo	Marketing Manager
Borghi, Maria Rosa	Marketing Manager
Naso, Lorenzo	Marketing Manager
Pioppo, Sergio Franco	Marketing Manager
Arrigo, Domenico Massimo	Product Manager
Borghi, Maria Rosa	Product Manager
Naso, Lorenzo	Product Manager
Pioppo, Sergio Franco	Product Manager
Moretti, Paolo	Q.A. Manager

ATTACHMENT TO PCN IPD-IPC/14/8692

Micro Leadframe Package conversion to High Density Leadframe in CARSEM sites

WHAT*:*
Micro Lead-frame Package (MLP) built on standard Lead-frame will be converted to High Density Lead-frame (HDL) on products assembled in package FPN3*3, 4*4 in Carsem Ipoh and FPN 5*5 in CARSEM Suzhou.
Impacted packaged products with HDL will also use the improved dedicated molding compound (G770HCD).
Combination of HDL and GC770HCD has been already qualified and it is running in production on similar product/packages.

WHY*:*
The above mentioned change will be implemented in order to harmonize Bill of Material as used in CARSEM Suzhou and Ipoh sites .

HOW*:*
This change has been qualified using the standard STMicroelectronics procedures for quality and reliability.
The details are described in the attached reports on the products which have been used as test vehicles to qualify the new material.

WHEN*:*
The change will be implemented within middle of Q4-2014 and the parts will be shipped from December 2014.

Reliability Report

STLD81

In

WFQFPN 32 5X5X0.8

General Information	
Product Line	*U1B4*
Product Description	Programmable Gamma Buffers & VCOM Buffer with Embedded NVM
P/N	STLD81QTR$Q2
Product Group	*IPD*
Product division	Handheld & Computer PM
Package	*WFQFPN 32 5X5X0.8*
Silicon Process technology	*BCD6 SHRINK*

Locations	
Wafer fab	*CT8*
Assembly plant	*Carsem China*
Reliability Lab	*Catania*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	Dec-2013	6	Angelo Donzuso	Giovanni Presti	Final issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

New Product qualification for **STLD81-U1B4** in WFQFPN 32 5X5X0.8 (wire 0,8 mils Au)

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The STLD81 provides a complete 14-channel total gamma solution for TFT-LCD displays. Through the I2C interface user can digitally program the Gamma Buffers and the VCOM Buffer

4.2 Construction note

	P/N STLD81QTR$Q2
Wafer/Die fab. information	
Wafer fab manufacturing location	Catania CT8
Technology	BCD6S
Die finishing back side	RAW SILICON
Die size	3192 x 2809 micron
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo KIO EWS
Tester	ETS364 MX50
Test program	STLD81_EWS.cpy
Assembly information	
Assembly site	SC - CARSEM - CHINA
Package description	WFQFPN 32 5X5X0.8
Molding compound	Epoxy
Frame material	442253 QFN 5x5 32L 154x154 RT2
Die attach material	Epoxy
Wires bonding materials/diameters	0,8 mil Au
Final testing information	
Testing location	Carsem CHINA
Tester	ETS364 MX50
Test program	STLD81_EWS.cpy

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot	#	Trace Code	Process/ Package	Product Line	Comments
1	5305111E	MQBG*U1B4AC5	BCD6 S WFQFPN 32 5X5X0.8	U1B4	

5.2 Test plan and results summary

P/N STLD81QTR$Q2

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Oriented Tests							
HTOL	N	JESD22 A-108	Tj = 125°C, Bias 5,5V,8V,-6V		168 H 500 H 1000 H	0/77 0/77 0/77	(1)
HTSL	N	JESD22 A-103	Ta = 150°C		168 H 500 H 1000 H	0/45 0/45 0/45	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		168 H	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy 200 cy 500 cy	0/77 0/77 0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, Bias 5,5V,8V,-6V		168 H 500 H 1000 H	0/77 0/77 0/77	(1)
Other Tests							
ESD	N	JEDEC JS001 JESD22-C101 JESD22-A115	HBM		±3KV	Passed	
			CDM		±1,5KV	Passed	
			MM		±300V	Passed	
LU	N	JESD78D	Current Inj. Overvoltage		±200mA	Passed	

Note (1): Samples soldered on Card Edge.

6 ANNEXES

6.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL Higt Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance.The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

Reliability Report

BCD6S (CT8) + Cu damascene (R2)

TV: ST1S50-UI78

in

VDFPN 3x3x1.0 10 PITCH 0.50, *1.3 mils Cu wires*

General Information	
Product Line	UI78
Product Description	4 A step-down switching regulator
P/N	ST1S50PUR
Product Group	IPD
Product division	IND.& POWER CONV.
Package	VDFPN 3x3x1.0 10 PITCH 0.50 1.3 mils Cu wires
Silicon Process technology	BCD6 S

Locations	
Wafer fab	AGRATE R2 AGRATE AG8 CATANIA CTM8
Assembly plant	CARSEM China
Reliability Lab	*CATANIA*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	August-2013	6	Angelo Donzuso	Giovanni.Presti	Final

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
REL 6043-018-W-13	Rel. Report on ST1S50- UI78 BCD6S (CT8), Cu Damascene metal process Agrate R2, 1.3 mils Au wires

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Aim: Reliability Evaluation on BCD6S (Catania M5) + Cu damascene (Agrate R2). TV: ST1S50.

Assembly Carsem China with 1,3 mils Cu wires

The BCD6SOI with Cu Damascene process and Cu wires in Carsem China is already qualified by other products.

The reliability verification will include the following TVs:

- ST1S50- UI78 BCD6S (CT8), Cu Damascene metal process Agrate R2, 1.3 mils Au wires (report issued REL 6043-018-W-13)
- ST1S50- UI78 BCD6S (CT8) + Cu Damascene metal process (Agrate R2), 1.3 mils Cu wires

3.2 Conclusion

Qualification Plan requirements have been fulfilled. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The ST1S50 is a 500 kHz fixed-frequency PWM synchronous step-down regulator. ST1S50 operates from 4.0 V to 18 V input, while it regulates an output voltage as low as 0.8V and up to 0.88 x VIN.

4.2 Construction note

	P/N ST1S50
Wafer/Die fab. information	
Wafer fab manufacturing location	AGRATE R2 +AGRATE AG8 + CATANIA CTM8
Technology	BCD 6 S
Process family	BCD6S (CT8) + Cu damascene (R2)
Die finishing back side	Cr/NiV/Au
Die finish front	SiN/TEOS/SiN
Die size	2182 X 1286 micron
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Assembly information	
Assembly site	CARSEM CHINA
Package description	VDFPN 3x3x1.0 10 PITCH 0.50
Molding compound	Epoxy
Frame material	Pure Tin Plating Sn 100%
Die attach material	Epoxy
Wires bonding materials/diameters	1.3 mils Cu
Final testing information	
Testing location	CARSEM China
Tester	ASL1K
Test program	ST1S50_rev1

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot	#	Assy Lot	Trace Code	Process/ Package	Product Line	Comments
1	5203856	C201311001402-01	MYWQ*UI78AC5	VDFPN 3x3x1.0 10 PITCH 0.50	UI78	

5.2 Test plan and results summary

P/N ST1S50

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Oriented Tests							
HTOL	N	JESD22 A-108	Tj = 125°C BIAS= Vin=18V, VFB/VEN=3V		168 H	0/77	
					500 H	0/77	
					1000 H	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/25	
					500 H	0/25	
					1000 H	0/25	
HTS	N	JESD22 A-103	Ta = 175°C		168 H	0/25	Engineering evaluation
					500 H	0/25	
					1000 H	0/25	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/25	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/25	
					200 cy	0/25	
					500 cy	0/25	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85% BIAS= Vin=18V , VFB/VEN=3V		168 H	0/25	
					500 H	0/25	
					1000 H	0/25	
Other Tests							
ESD	N	JEDEC JS001	HBM	3	+/-2000V	Pass	
		ESDA S 5.3	CDM	3	+/-500V +/-750V	Pass	
LU	N	JESD78D	Current Inj.Overvoltage	6	±100mA at 85ºC	Pass	

5.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL Higt Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD **Electro Static Discharge**	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CDM: Charged Device Model HBM: Human Body Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU **Latch-Up**	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

Reliability Evaluation Report

ST8034

New Product Qualification

General Information	
Product Line	*UI87*
Product Description	*Smartcard interfaces*
P/N	*ST8034HNQR* *ST8034PQR* *ST8034ATDT*
Product Group	*AMS*
Product division	*STD Products & HiRel*
Package	*QFN 24L* *QFN 16L*
Silicon Process technology	*BCD6S-3M*

Locations	
Wafer fab	*Catania M5*
Assembly plant	*Carsem S* *QFN 24L* *QFN 16L*
Reliability Lab	*Catania Reliability Lab*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	25-Mar-2013	11	A.Riciputo	G.Presti	
1.1					QFN 4x4 24L and QFN 3X3-16Lpackages

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47E	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

New Product.

The present evaluation plan includes different packages for the same product:

QFN 4x4 24L and QFN 3X3-16L packages using CU wires 1 mil, assembled in CARSEM S.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Smartcard interfaces

4.2 Construction note

	ST8034	
Wafer/Die fab. information		
Wafer fab manufacturing location	Catania M5	
Technology	BCD6S	
Die finishing back side	RAW SILICON	
Die size	1608x1700µm	
Passivation type	TEOS/SiN/Polyimide	
Wafer Testing (EWS) information		
Electrical testing manufacturing location	TPY	
Tester	J750 Teradyne	
Assembly information		
Assembly site	Carsem S	
Package description	QFN 4x4 24L	QFN 3x3-16L
Molding compound	EPOXY	
Wires bonding materials/diameters	Cu 1mil	
Final testing information		
Testing location	Carsem S	
Tester	ASL1K	

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Tech. Code	Process/ Package	Product Line	Comments
1	5226598	ENGC3402	AYD8*UI87AA5	BCD6S-3M/ QFN 4x4 24L	UI87	
2		ENGC4003				
3		ENGC3404	AY94*UI87AA5	BCD6S-3M/ QFN 3x3 16L		

5.2 Test plan and results summary

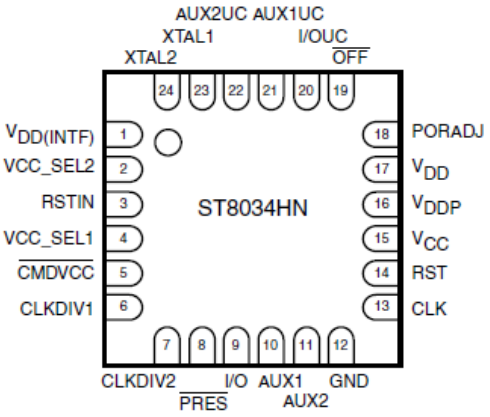
ST8034

Test	PC	Std ref.	Conditions	Steps	Failure/SS				Note
					Lot 1	Lot 2	Lot 3		
Die Oriented Tests									
HTB	N	JESD22 A-108	Tj = 125°C, Vbias=+6V	168 H	0/77				
				500 H	0/77				
				1000 H	0/77				
HTSL	N	JESD22 A-103	Ta = 150°C	168 H	0/45	0/45	0/45		
				500 H	0/45	0/45	0/45		
				1000 H	0/45	0/45	0/45		
Package Oriented Tests									
PC		JESD22 A-113	Drying 24H@125°C Store 168H@Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	Final	Pass	Pass	Pass		
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	96 H	0/77	0/77	0/77		
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	100 cy	0/77	0/77	0/77		
				200 cy	0/77	0/77	0/77		
				500 cy	0/77	0/77	0/77		
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85% Vbias=+5V,	168 H	0/77	0/77			
				500 H	0/77	0/77			
				1000 H	0/77	0/77			
Other Tests									
ESD	N	AEC Q101-001, 002 and 005	HBM	±2KV	Pass				All pins
				±8KV	Pass				I/O, RST, VCC, CLK,PRES Pins
			CDM	±500V	Pass	Pass	Pass		
			MM	±200V	Pass				
LU	N	AEC Q100 - 004	Current Inj. Overvoltage		Pass				

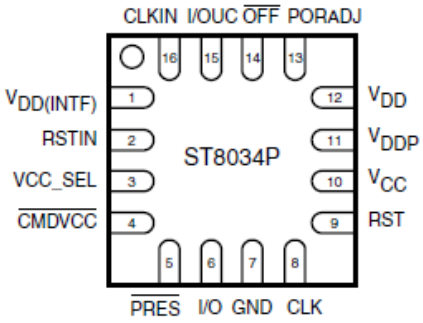
6 ANNEXES

6.1 Device details

6.1.1 Pin connection

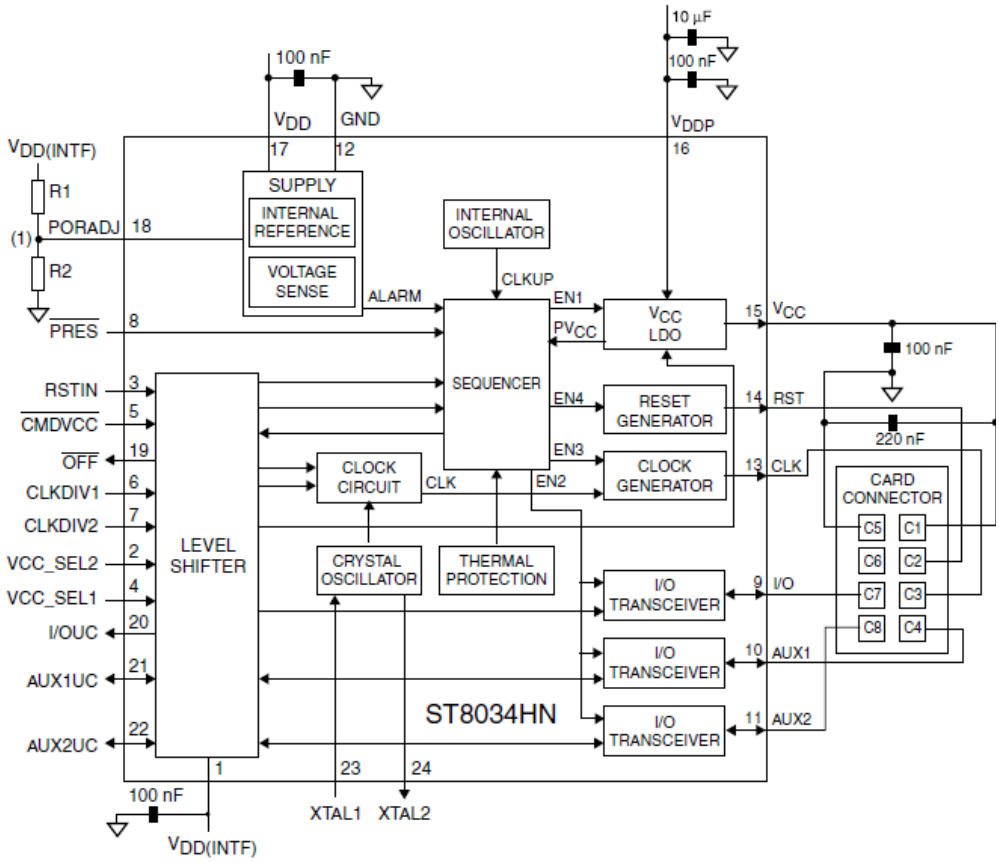


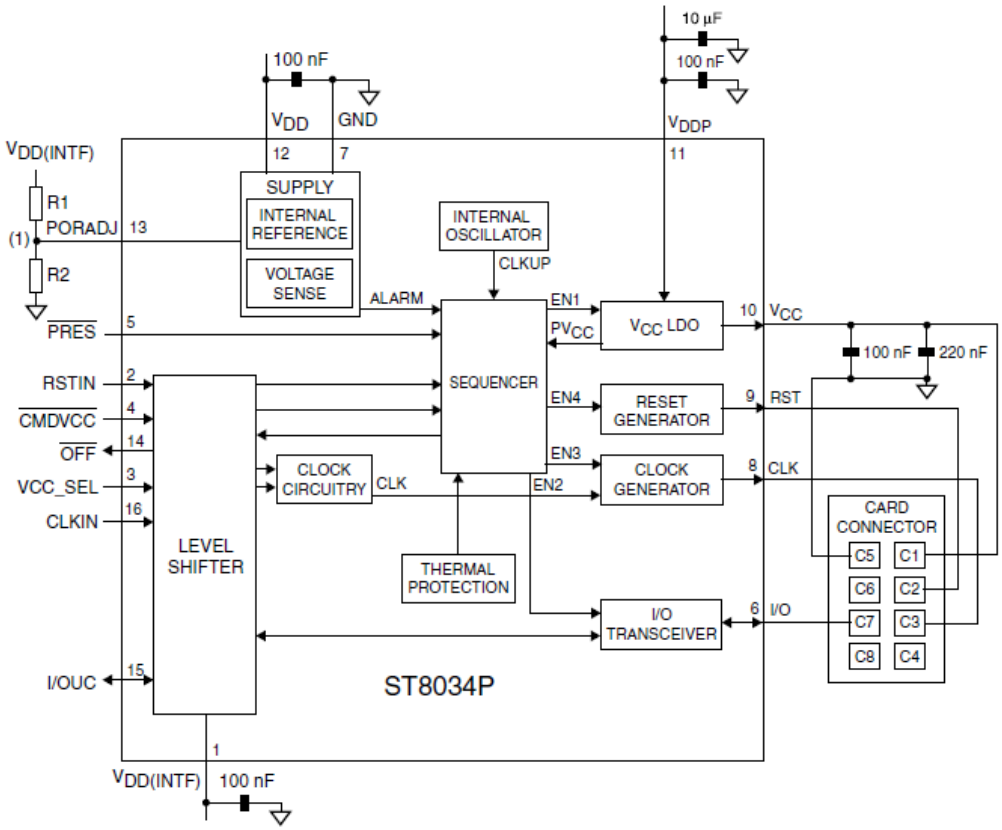
QFN24 - 4 x 4 x 0.8 mm, 0.5 mm pitch

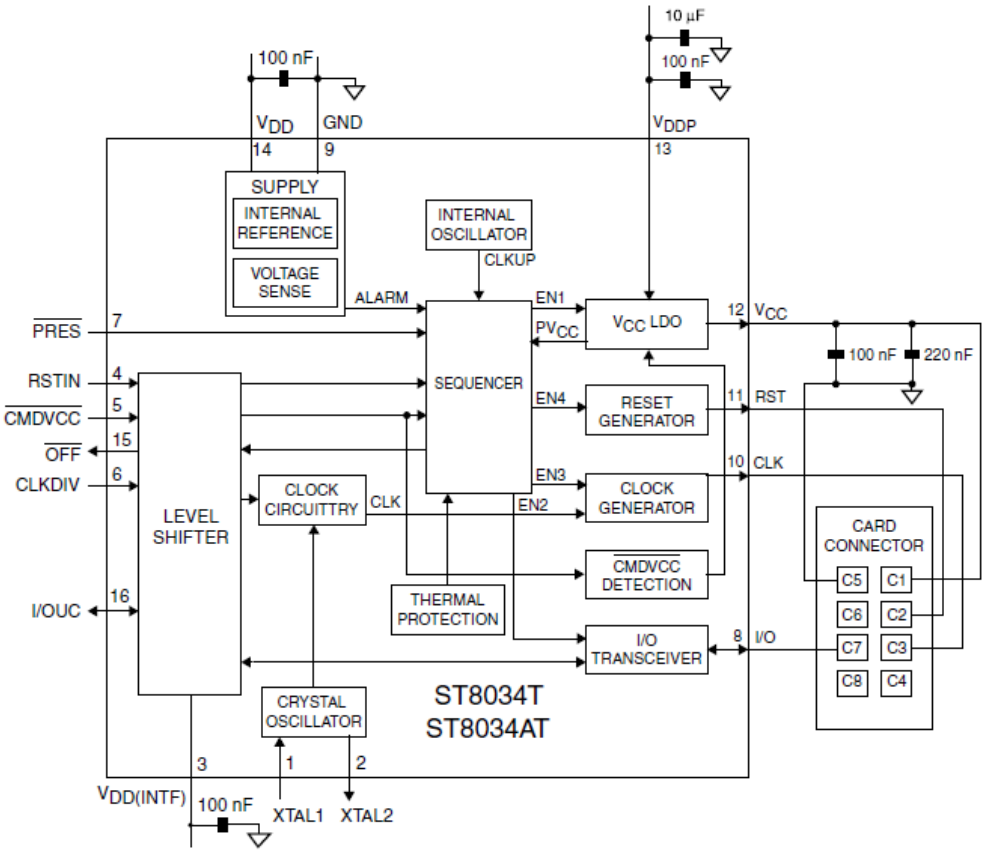


QFN16 3 x 3 x 0.8 mm, 0.5 mm pitch

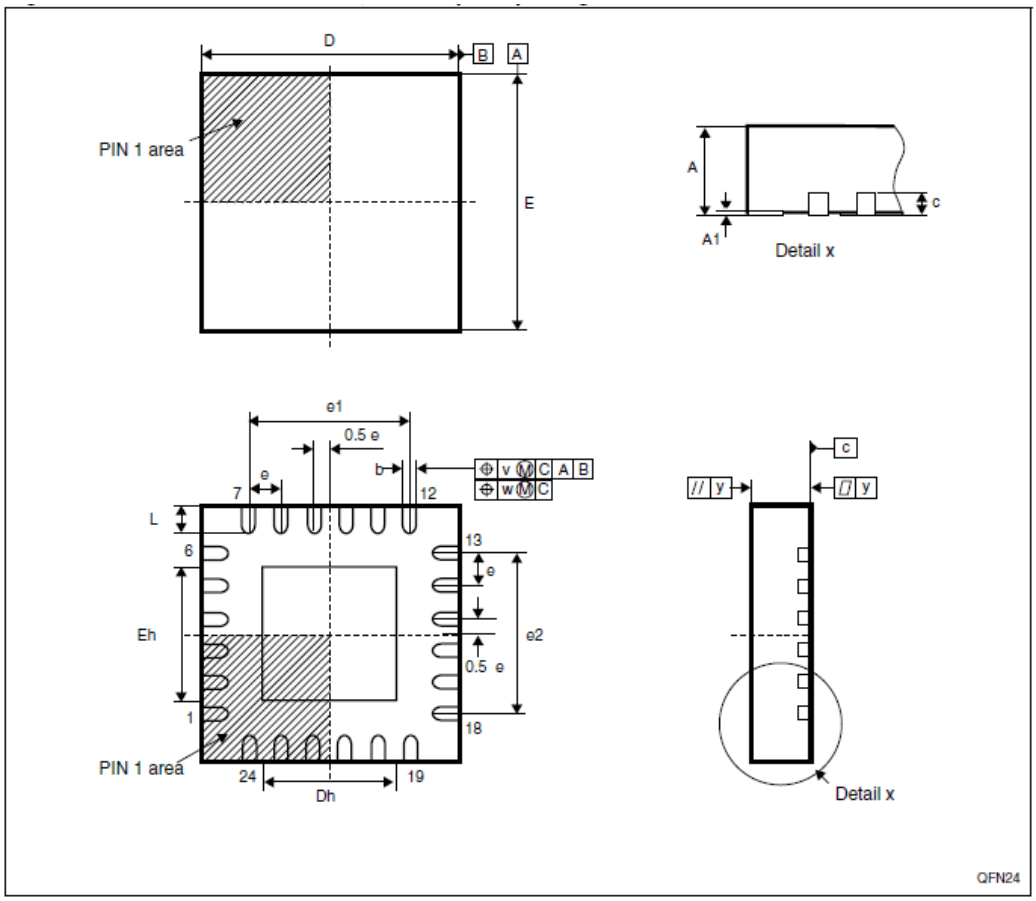
6.1.2 Block diagram




10 µF
100 nF
100 nF
VDD
GND
VDDP
VDD(INTF)
12
7
11
SUPPLY
INTERNAL REFERENCE
VOLTAGE SENSE
INTERNAL OSCILLATOR
R1
(1)
PORADJ
13
R2
CLKUP
ALARM
EN1
PVCC
VCC LDO
10
VCC
PRES
5
100 nF
220 nF
RSTIN
2
SEQUENCER
EN4
RESET GENERATOR
9
RST
CMDVCC
4
OFF
14
EN3
CLOCK GENERATOR
8
CLK
VCC_SEL
3
CLOCK CIRCUITRY
CLK
EN2
CLKIN
16
CARD CONNECTOR
C5
C1
C6
C2
C7
C3
C8
C4
LEVEL SHIFTER
THERMAL PROTECTION
I/O TRANSCEIVER
6
I/O
I/OUC
15
ST8034P
1
VDD(INTF)
100 nF


10 µF
100 nF
100 nF
VDD
GND
VDDP
14
9
13
SUPPLY
INTERNAL REFERENCE
VOLTAGE SENSE
INTERNAL OSCILLATOR
CLKUP
ALARM
EN1
PVCC
VCC LDO
12 VCC
PRES
7
RSTIN
4
CMDVCC
5
OFF
15
CLKDIV
6
SEQUENCER
EN4
RESET GENERATOR
11 RST
100 nF
220 nF
EN3
CLOCK GENERATOR
10 CLK
CLOCK CIRCUITTRY
CLK
EN2
LEVEL SHIFTER
CARD CONNECTOR
C5
C1
C6
C2
C7
C3
C8
C4
CMDVCC DETECTION
THERMAL PROTECTION
I/OUC
16
I/O TRANSCEIVER
8 I/O
ST8034T
ST8034AT
CRYSTAL OSCILLATOR
3
1
2
VDD(INTF)
100 nF
XTAL1
XTAL2

6.1.3 Package outline/Mechanical data



Symbol	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1	Unit
Dim.	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1	mm

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

Reliability Evaluation Report

STOD32- BCD8SP

Cu metal RDL (R2+AG8)

New Product + Technology Validation

General Information	
Product Line	*UAP5*
Product Description	*300mA TRIPLE DC/DC CONVERTER FOR POWERING AMOLED*
P/N	*STOD32ATPQR*
Product Group	*IPG*
Product division	*Handheld & Computer*
Package	*VFQFPN 16L 3X3X0.55 PITCH 0.5*
Silicon Process technology	*BCD8SP*

Locations	
Wafer fab	*R2+AG8*
Assembly plant	*CARSEM*
Reliability Lab	*Catania Reliability Lab*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	July-2014	7	Giuseppe Giacopello	Giovanni Presti	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

New Product + New Technology Validation

The product is a new development coming from STOD30 solution having better performance in terms of efficiency, TDMA noise, Load transient and package. In addition it adds more flexibility, thanks to the possibility to program/select different functionalities by Swire.

Silicon oriented stress:

The technology BCD8SP Cu metal RDL (R2+AG8) to be validated. Key features are:

8V PMOS extension of P2 for Step-up section
DTI (Deep Trench Isolation) integration for Substrate Noise reduction (on Power Device)
Cu RDL area 29% (with drop in)
Thickness 125 um

Package Oriented stresses:

QFN 16L 0.5mm pitch, 0.6mm thickness in CARSEM (1.3 Cu wire)
New Frame

FE/BE Compatibility to be investigated.

Telecom Mobile and Consumer Mission Profile and Technology Validation:

Product Mission Profile:
14h operation/day @ 50degC average temperature over 10 years period is equivalent to 5.8 years of continuous operating life. Equivalent reliability stress is 500h @ 125 °C.

In order to validate the technology the reliability stress has been continued until 1000h

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

Present reliability verification it is valid both for STOD32A and STOD32B versions.

4 DEVICE CHARACTERISTICS

4.1 Device description

The STOD32 is a triple DC/DC converter for AMOLED display panel. It integrates 300mA step-up and inverting DC-DC converters plus auxiliary step-up converter. The device it particularly suitable for battery operated products, in which the major concern is the overall system efficiency.

4.2 Construction note

	P/N STOD32ATPQR
Wafer/Die fab. information	
Wafer fab manufacturing location	R2+AG8
Technology	BCD8SP
Process	BCD8SP Cu metal RDL, DTI (Deep Trench Isolation)
Die finishing back side	Raw Silicon
Die size	1648 X 1740 micron
Passivation type	HDP/TEOS/NITRIDEX
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio
Tester	ASL 1000
Assembly information	
Assembly site	CARSEM
Package description	VFQFPN 16L 3X3X0.55 PITCH 0.5
Die Attach Process	Epoxy
Die Attach Material	Glue
Molding compound	Epoxy
Wires bonding materials/diameters	1.2 mils Cu
Lead Finishing	Process 100% pure Sn
Final testing information	
Testing location	Carsem
Tester	ASL1000

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Comments
1	BCD8SP Cu metal RDL, DTI (Deep Trench Isolation)	
2		
3		
4	VFQFPN 16L 3X3X0.55 PITCH 0.5	
5		

5.2 Test plan and results summary

P/N STOD32ATPQR

Test	PC	Std ref.	Conditions		Steps	Failure/SS			Note
						Lot 1	Lot 4	Lot 5	
Die Oriented Tests									
HTOL	N	JESD22 A-108	Ta = 125°C, BIAS= -5V/6V/8V		168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/25	0/25	0/25	
					500 H	0/25	0/25	0/25	
					1000 H	0/25	0/25	0/25	
Package Oriented Tests									
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/25	0/25	0/25	
TC	Y	JESD22 A-104	Ta = -40°C to 125°C		100 cy	0/25	0/25	0/25	
					200 cy	0/25	0/25	0/25	
					500 cy	0/25	0/25	0/25	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS= -5V/6V/8V		168 H	0/25	0/25	0/25	
					500 H	0/25	0/25	0/25	
					1000 H	0/25	0/25	0/25	
Other Tests									
ESD	N	JEDEC JS001 ANSI/ESDA JESD22-A115	HBM		2KV	Pass			
			CDM		CLASS C3	Pass			
			MM		200V	Pass			
LU	N	JESD78D	Current Inj. Overvoltage		±200mA	Pass			

Test	PC	Std ref.	Conditions		Steps	Failure/SS				
						Lot 2	Lot 3	Lot 4	Lot 5	
Die Oriented Tests										
ELFR	N	JESD22 A-108	Ta = 125°C, BIAS= -5V/6V/8V		48H	0/526	0/282	0/803	0/999	

5.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
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