



Click [here](#) for the 3D model.

Dimensions

D	9.845mm +/-0.955mm
L	6.35mm MIN
T	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
A	9.144mm MAX
C	10.16mm +/-0.635mm
E	11.18mm MAX
G	1.4mm +/-0.254mm
LO	1.586mm MAX
LW	0.508mm +/-0.051mm

Packaging Specifications

Packaging	Waffle, Box
Packaging Quantity	36

General Information

Series	KPS LDD Mil SMPS PRF49470
Style	Leaded Stacked Chip
Description	Low ESR, High Current Stacked Ceramic Chips
Features	Low ESR, High Current
RoHS	No
Prop 65	⚠ WARNING: Cancer and reproductive harm - http://www.p65warnings.ca.gov .
SCIP Number	2499890a-0e07-42ff-98a1-bd02d3b7c2ec
Termination	60/40 Solder Coated
Lead	Wire Leads
Failure Rate	N/A
Testing and Reliability	Level B
Qualifications	MIL-PRF-49470
AEC-Q200	No
Notes	Note: Number of chips in stack depends on design. Note: Lead alignment within pin rows shall be within ±0.13 mm.

Specifications

Capacitance	8.2 uF
Capacitance Tolerance	10%
Voltage DC	50 VDC
Dielectric Withstanding Voltage	125 VDC
Temperature Range	-55/+125°C
Temperature Coefficient	BX
Dissipation Factor	2.5%
Insulation Resistance	121.951 MOhms