CORELIS
An EWA Company

Program

PXI Express

75 MHz

Test

4

4 TAPs

PXIe-1149.1/4E™

High-Performance 4-TAP PXI Express JTAG Controller

Features

- High-performance multi-TAP JTAG controller with integrated I^2C and SPI interfaces.
- Four TAP connections for designs with multiple scan chains.
- User programmable JTAG TCK rate up to 75 MHz, SPI SCK rate up to 50 MHz, and I2C SCL rate up to 5 MHz.
- Assignable signal pins on each TAP for additional versatility.
- Three general purpose I/O signals per TAP for a total of twelve (12) GPIOs.
- Variable output voltage and configurable input voltage threshold.
- Automatic signal delay compensation for long cable lengths.
- High-speed PXI Express interface ideal for the ATE system integration.
- Supports Microsoft Windows and Linux operating systems.

Boundary-scan has proven itself time and again to be a truly versatile interface for structural test, embedded functional test, built-in self-test (BIST), software debug, and in-system programming. Supporting such diverse applications requires a controller with high-performance specifications and diverse features.

The **PXIe-1149.1/4E** is a high-performance, multi-feature boundary-scan controller for multi-TAP and concurrent JTAG test and in-system programming. Featuring a high-speed PXI Express (PXIe) interface with four independent and configurable Test Access Ports (TAPs) along with direct serial programming capability, the PXIe-1149.1/4E enables of boundary-scan integration with PXIe systems.

Applications

Boundary-Scan Test
Use boundary-scan to test, debug, and verify hardware through all phases of the product life-cycle, from development through production and into to the field.

JTAG Embedded Test
Control a microprocessor through the JTAG debug port to run functional tests without requiring boot code.

In-System Programming
Read, erase, program, and verify flash memory, serial PROMs, CPLDs, FPGAs, and other programmable devices directly within a circuit or system design.

High Volume Production
Run concurrent tests and ISP on up to four UUTs with ScanExpress Runner™ Gang Edition.

Benefits

- Save time at test-stations with high performance up to 75 MHz on all TAPs for lightning-fast test and in-system-programming.
- Integrate JTAG/boundary-scan into PXIe-based ATE systems.
- Reduce costs associated with fixtures; the multi-TAP controller connects to up to four TAPs for multi-TAP and/or gang operation.
- Compatible with the complete ScanExpress™ family of boundary-scan and JTAG embedded test products.

PXIe-1149.1/4E

High Performance & Versatility

The Corelis PXIe-1149.1/4E is fully compliant with the IEEE Standard 1149.1 (commonly referred to as JTAG) for test access. Based on the Corelis IEEE-1149.1/4E 4-TAP architecture, the PXIe card can be installed in a PXIe chassis to provide up to four test access port (TAP) connections on any JTAG-based target system. Support for concurrent (Gang) test execution and in-system programming, configurable pinout, and integrated serial interfaces on each TAP interface make the PXIe-1149.1/4E ideal for multi-TAP and high-volume JTAG and serial bus-programming integration.

Scan Function Library

For applications that require a low-level interface or integration with third-party software, Corelis offers a Scan Function Library (SFL). The SFL is provided as a DLL for Microsoft Windows and provides all functions necessary to operate the JTAG port to send and receive JTAG instructions and data from the target system. The SFL can be incorporated in custom application software or integrated with third-party systems such as National Instruments LabVIEW, National Instruments TestStand, and Keysight VEE.

Ordering Information

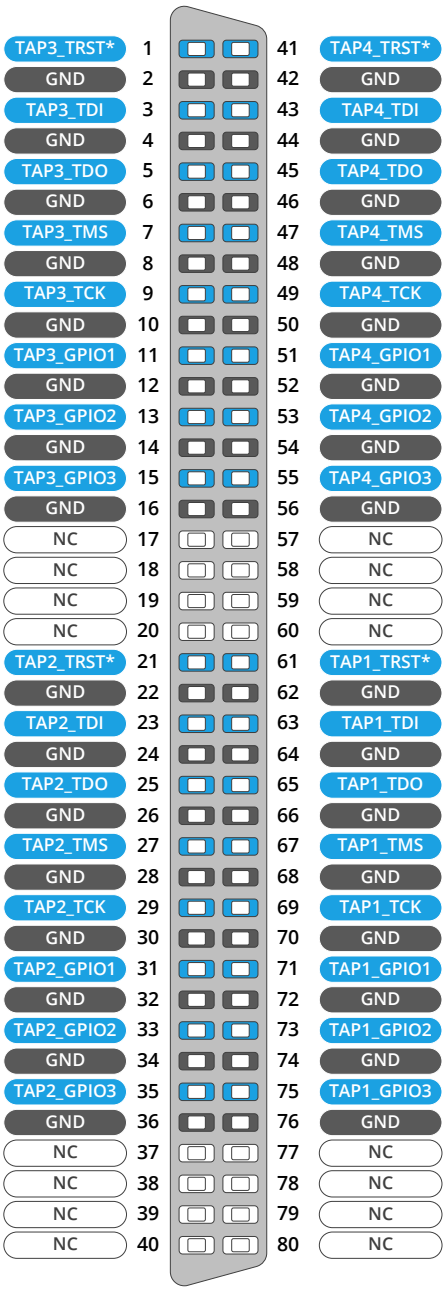
PXIe-1149.1/4E - Part Number 10420

For more information or to request a quote, please visit our website at www.corelis.com

Hardware Specifications

General	
Mechanical dimensions (4-TAP)	8.5 inches x 0.8 inches x 5.1 inches
Host Interface	
PXIe interface	3U PXIe slot using 1 lane of PCIe
Power Requirements	12 V, 3.3 V provided by the PXIe interface
Target Interface	
Test access ports (TAPs)	80 Position D-Type Receptacle TE Connectivity AMP part no. 5787190-8 or equivalent
Mating Connector	80 Position D-Type Plug TE Connectivity AMP part no. 5749621-8 or equivalent
TAP Cable	One 80-pin to Four 20-pin TAP Cable, Corelis P/N 15467 Additional options are available.
Output Voltage	Programmable from 1.25 V to 3.30 V in 0.05 V steps
Threshold Voltage	Programmable from 0.50 V to 2.00 V in 0.05 V steps
JTAG Interface	
Compliance	IEEE-1149.1 compliant interface
TCK frequency range	0.050 MHz to 75 MHz
I²C Interface	
SCL frequency	0.050 MHz to 5 MHz
SPI Interface	
SCK frequency range	0.050 MHz to 50 MHz
Chip Selects	5 per TAP

Please refer to the PXIe-1149.1/4E User's Manual for complete specifications.



The PXIe front panel connector features 4 TAPs with configurable signal pins

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