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Evaluating the ADMV7320 81 GHz to 86 GHz, E-Band Upconverter SiP

FEATURES

Simple power-up with on-board LDO regulators
Gain tuning and device bias adjustment with potentiometers
Option to bypass LDO regulators with connector jumpers

EVALUATION KIT CONTENTS

ADMV7320-EVALZ
Connector jumpers

EQUIPMENT NEEDED

+5 V dc and −5 V dc power supplies
Baseband signal generator
RF signal generator
E-band spectrum analyzer
WR-12 waveguide

ADMV7320-EVALZ PHOTOGRAPHY

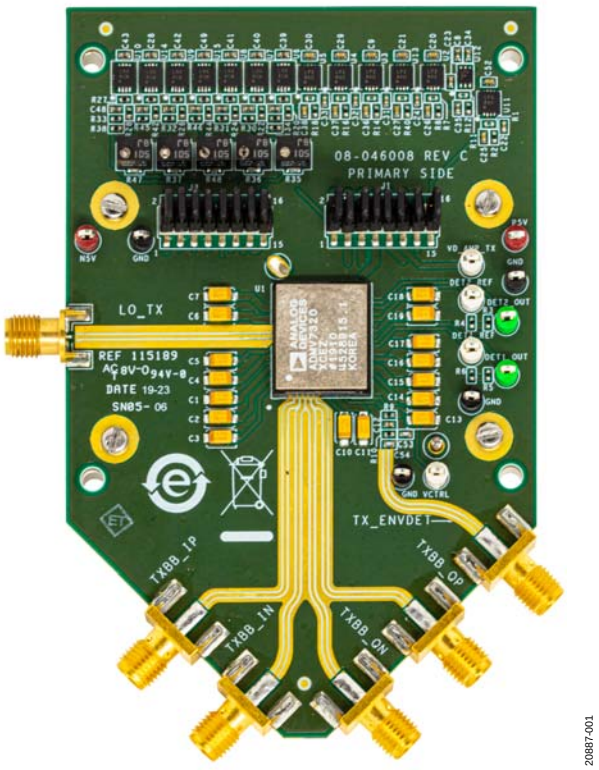

Figure 1.

GENERAL DESCRIPTION

The ADMV7320-EVALZ evaluation board incorporates the ADMV7320 with low dropout (LDO) regulators, potentiometers, and a waveguide back plate to allow quick and easy evaluation of the ADMV7320. The LDO regulators allow the ADMV7320 to be powered on by ±5 V dc supplies. Potentiometers allow gates tuning for various gain range.

The ADMV7320 is a fully integrated system in package (SiP) inphase/quadrature (I/Q) upconverter that operates from 81 GHz to 86 GHz.

For full details, see the ADMV7320 data sheet, which must be consulted and used in conjunction with this user guide when using the ADMV7320-EVALZ.

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REVISION HISTORY

11/2019—Revision A: Initial Version

EVAULATION BOARD QUICK START PROCEDURES

The ADMV7320-EVALZ is equipped with LDO regulators to provide drains and gates biases. Only +5 V dc and −5 V dc power supplies are required to power up the chip. Note that the evaluation board is tuned to achieve a typical current level.

To ensure that damage does not occur, use the following sequence to power up:

1. Place jumpers on all pins of the J3 connector.
2. Place jumpers on all pins of the J1 connector, except Pin 1 and Pin 2.
3. Connect the −5 V dc power supply to the N5V test point and ground the supply to the nearest GND test point.
4. Connect the 5 V dc power supply to the P5V test point.
5. Turn on the −5 V dc supply and then turn on the +5 V dc supply.
6. Place jumpers on Pin1 and Pin2 of the J1 connector.
7. Connect VCTRL to the −5 V dc supply for maximum gain.
8. Adjust the dc voltages between −0.2 V and +0.2 V for the TXBB_IN, TXBB_IP, TXBB_QN, and TXBB_QP ports for LO nulling.

To power down the chip, use the following sequence:

1. Disconnect the −5 V dc supply on VCTRL.
2. Turn off the 5 V dc supply.
3. Turn off the −5 V dc supply.

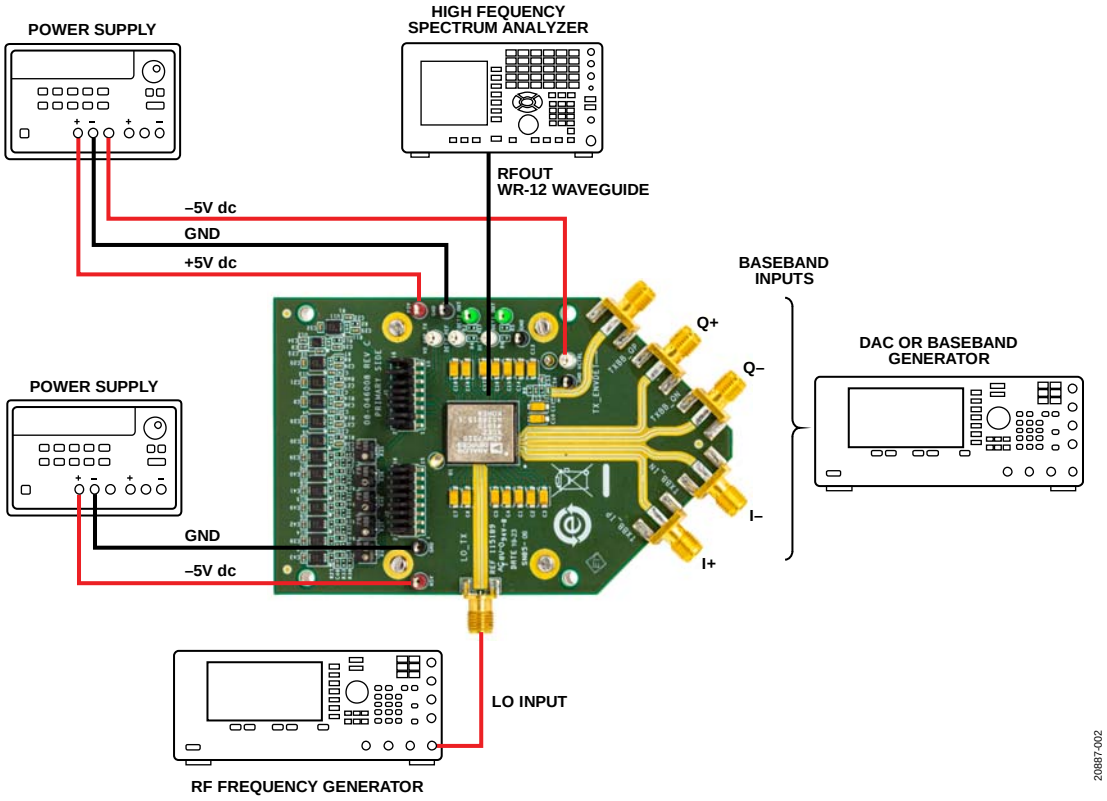

Figure 2. ADMV7320-EVALZ Lab Bench Setup

GAIN TUNING PROCEDURE

Three different mechanisms are available to control the total gain of the transmitter (follow the gain tuning order in Table 1 to achieve the correct gain level for optimal performance).

Table 1. Gain Tuning Summary

Gain Tuning Order	Gain Reduction Range (dB)	Gain Tuning	Recommended Gain Tuning Voltage Range (V)
First	0 to 10	VGA_VCTRL12	−5 to −1
Second	10 to 25	VGA_VG345 and VGA_VG6	−2 to 0
Third	25 to 40	PA_VG1	−2 to 0

VGA_VCTL12

The VGA_VCTL12 pin is tied to the VCTRL test point. To achieve maximum gain, set the VCTRL test point to the −5 V dc supply. To achieve a gain reduction between 0 dB and 10 dB, adjust the VCTRL test point voltage between −5 V and −1 V (typical minimum gain for variable gain amplifier).

VGA_VG345 and VGA_VG6

If further gain reduction is needed after conducting the first step in the gain tuning order, lower the I_{D_VGA345} and I_{D_VGA6} drain current levels, by adjusting VGA_VG345 and VGA_VG6 together, between −2 V and 0 V to achieve the proper gain level. The total current consumption of I_{D_VGA345} and I_{D_VGA6} can be lowered to 45 mA.

To tune VGA_VG345 and VGA_VG6 on ADMV7320-EVALZ, use the following sequence:

1. Power down the chip by turning off the 5 V dc supply and then turning off the −5 V dc supply.
2. The R36 potentiometer tunes VGA_VG345 and VGA_VG6. Place an ampere meter between Pin 9 and Pin 10 on J1 to monitor the I_{D_VGA345} and I_{D_VGA6} current.
3. Power up the chip by turning on the −5 V supply and then turning on the +5 V dc supply.
4. Adjust the R36 resistor to tune VGA_VG345 and VGA_VG6. The total current of VGA_ID345 and VGA_ID6 must not drop below 45 mA.

PA_VG1 Tuning

If further gain reduction is needed after conducting the first and second steps in the gain tuning order, lower the I_{D_PA1} drain current level by adjusting PA_VG1 between −2 V to 0 V to achieve the proper gain level. The current consumption of I_{D_PA1} can be lowered to 100 mA.

To tune PA_VG1 on ADMV7320-EVALZ, use the following sequence:

1. Power down the chip by turning off the +5 V dc supply and then turning off the −5 V dc supply.
2. The R47 potentiometer tunes the PA_VG1 pin. Place an ampere meter between Pin 3 and Pin 4 on J1 to monitor the current of PA_VD1.
3. Power up the chip by turning on the −5 V dc supply and then turning on the +5 V dc supply.
4. Adjust the R47 to tune PA_VG1. The P1_VD1 current must not drop below 100 mA for PA1 tuning.

EVALUATION BOARD SCHEMATICS

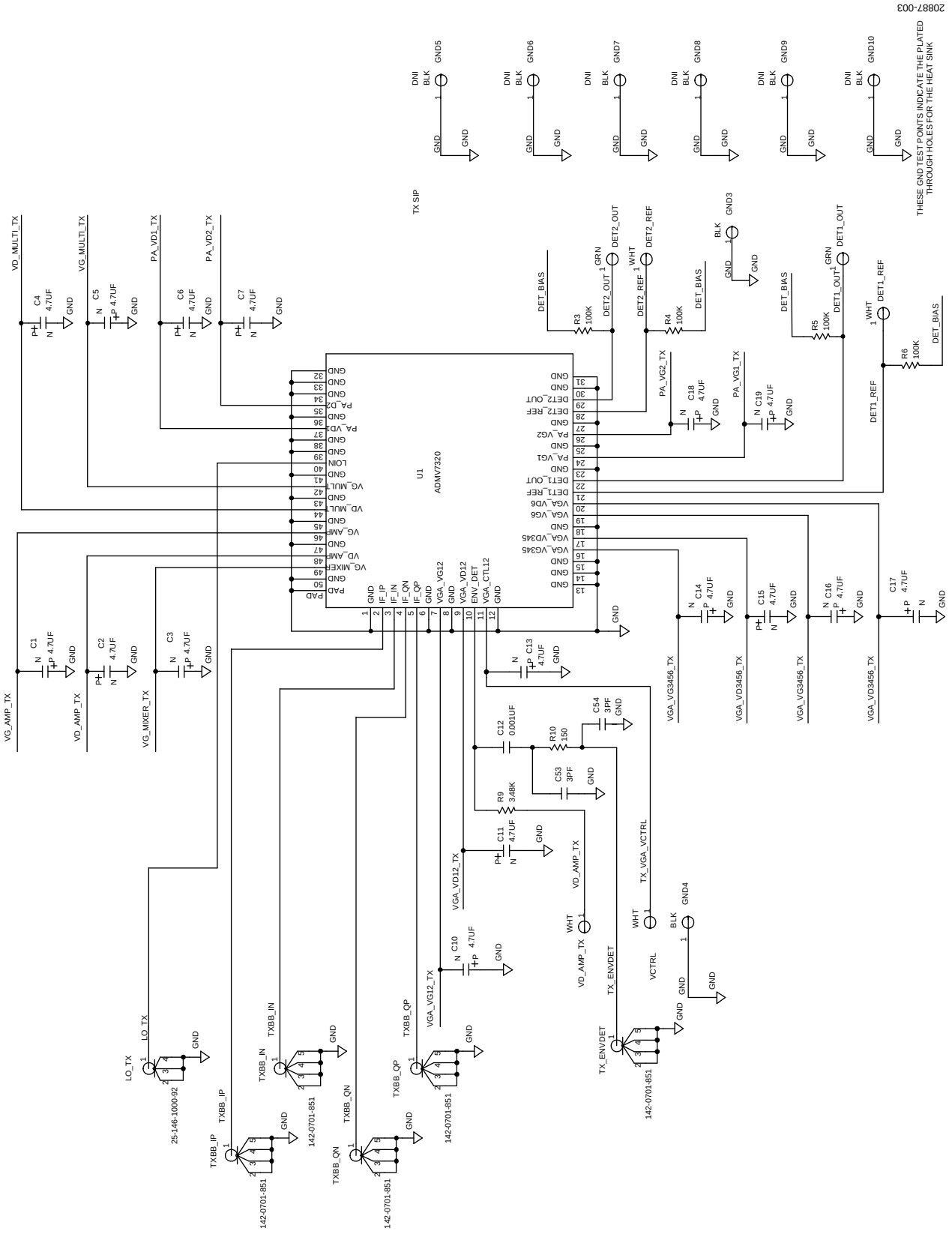

Figure 3. ADMV7320-EVALZ Schematic, Page 1

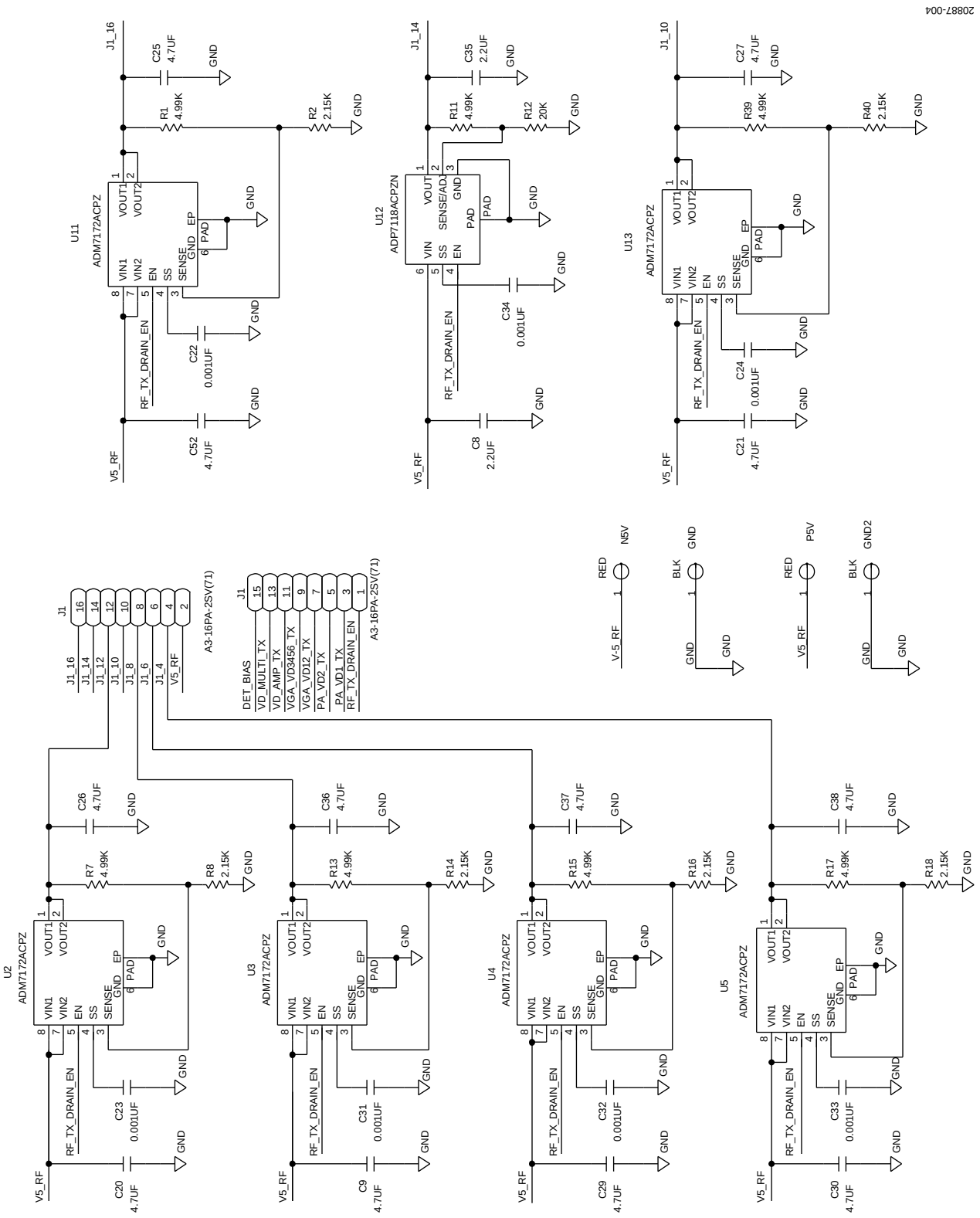

Figure 4. ADMV7320-EVALZ Schematic, Page 2

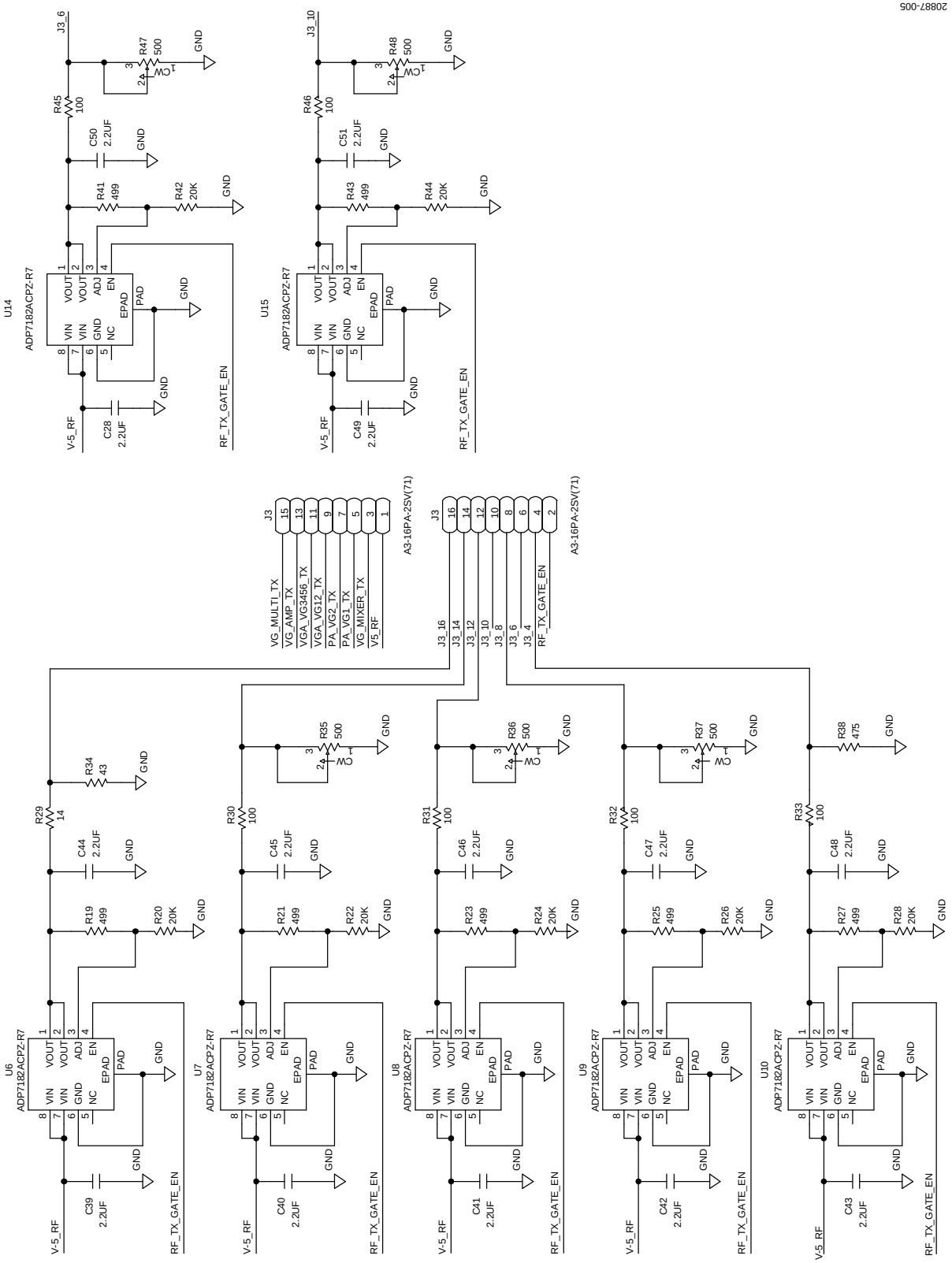

Figure 5. ADMV7320-EVALZ Schematic, Page 3

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Qty.	Reference Designator	Description
16	C1 to C7, C10, C11, C13 to C19	Capacitor, tantalum, 4.7 µF
8	C12, C22 to C24, C31 to C34	Capacitor, ceramic, 1 nF
12	C9, C20, C21, C25 to C27, C29, C30, C36 to C38, C52	Capacitor, ceramic, 4.7 µF
16	C8, C28, C35, C39 to C51	Capacitor, ceramic, 2.2 µF
2	C53, C54	Capacitor, ceramic, 3 pF
2	J1, J3	Connector, miniature, 2 mm
1	LO_TX	Connector, RF, 2.92 mm, SRI 25-146-1000-92
7	R1, R7, R11, R13, R15, R17, R39	Resistor, chip, 4.99 kΩ
1	R10	Resistor, chip, 150 Ω
8	R12, R20, R22, R24, R26, R28, R42, R44	Resistor, chip, 20 kΩ
6	R2, R8, R14, R16, R18, R40	Resistor, chip, 2.15 kΩ
7	R19, R21, R23, R25, R27, R41, R43	Resistor, chip, 499 Ω
1	R29	Resistor, chip, 14 Ω
4	R3 to R6	Resistor, chip, 100 kΩ
6	R30 to R33, R45, R46	Resistor, chip, 100 Ω
1	R34	Resistor, chip, 43 Ω
5	R35 to R37, R47, R48	Potentiometer, trimmer, 500 Ω
1	R38	Resistor, chip, 475 Ω
1	R9	Resistor, chip, 3.48 kΩ
5	TXBB_IN, TXBB_IP, TXBB_QN, TXBB_QP, TX_ENVDET	Connector, SMA, JOHNSON 142-0701-851
1	U1	ADMV7320
7	U6 to U10, U14, U15	LDO, ADP7182ACPZ-R7
6	U2 to U5, U11, U13	LDO, ADM7172ACPZ-R7
1	U12	LDO, ADP7118ACPZN
8	DET1_OUT, DET2_OUT, DET1_REF, DET2_REF, VCTRL, VD_AMP_TX, N5V, P5V	Test point