



18 Bit RGB, 8/16-bit parallel, SPI interface



Dimension Display 54.7x83x2.2mm Incl. PCAP 65x100x4.35mm

## FEATURES

- 3.5" TFT DISPLAY, IPS TECHNOLOGY
- 320x480 WIDE SCREEN
- OPTIONALLY PCAP TOUCHPANEL OPTICALLY BONDED
- SUPER BRIGHT >1000cd/m<sup>2</sup> (850 cd/m<sup>2</sup> INCL. PCAP)
- HIGH CONTRAST TFT PANEL
- INTEGRATED CONTROLLER HX8357D
- 18 BIT RGB INTERFACE
- 8 BIT / 16 BIT DATABUS INTERFACE
- I<sup>2</sup>C BUS INTERFACE FOR PCAP
- 3.3V SUPPLY VOLTAGE
- WIDE TEMPERATURE RANGE (T<sub>OP</sub> -20 .. +70°C)
- INDUSTRIAL GRADE DISPLAY

## **ORDERING CODES**

 $3.5"\ {\rm TFT},\ 320x480\ {\rm IPS}\ {\rm COLOR}\ {\rm DISPLAY}\ 1000 {\rm cd/m^2}$  AS ABOVE BUT WITH OPTICALLY BONDED PCAP

EA TFT035-34AINN EA TFT035-34AITC

## ACCESSORY

ZIF CONNECTOR 0.3MM, BOTTOM CONTACT (Datasheet: https://www.lcd-module.de/eng/pdf/zubehoer/WF030-39S.pdf) EA WF030-39S

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### REVISION

DATE	REF.PAGE PARAGRAPH DRAWING No.	REVISED No.	SUMMARY	REMARK
2020-03-18		V01	First Issue	
2021-05-20		V02	Addes initialisation example	





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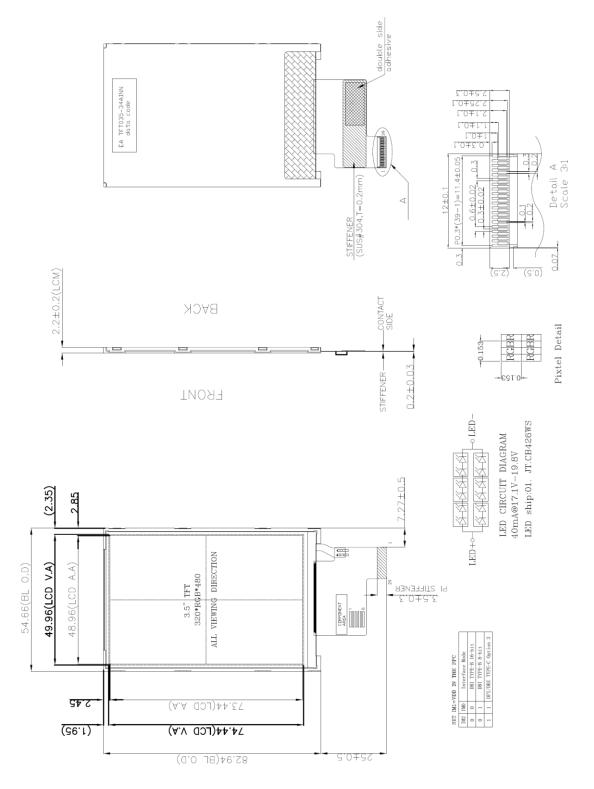
### **1. GENERAL SPECIFICATION**

Item	Contents	Unit
LCD type	TFT/Transmissive normally black	
Module size (W*H*T)	65.0*100.0*4.35	mm
w. PCAP	54.66*82.94*2.2	mm
Active size (W*H)	48.96*73.44	mm
Pixel pitch (W*H)	0.153*0.153	mm
Number of dots	320*RGB*480	
Driver IC	HX8357D	
Interface type	8-Bit, 16-Bit, 18-Bit RGB	
Top polarizer type	Anti-Glare	
Recommend viewing direction	All around	0
Gary scale inversion direction		0
Backlight type	6 dies white LED	
Touch panel type	Capacitive, EA TFT035-34AITC only	
Touch panel controller	GT911, EA TFT035-34AITC only	





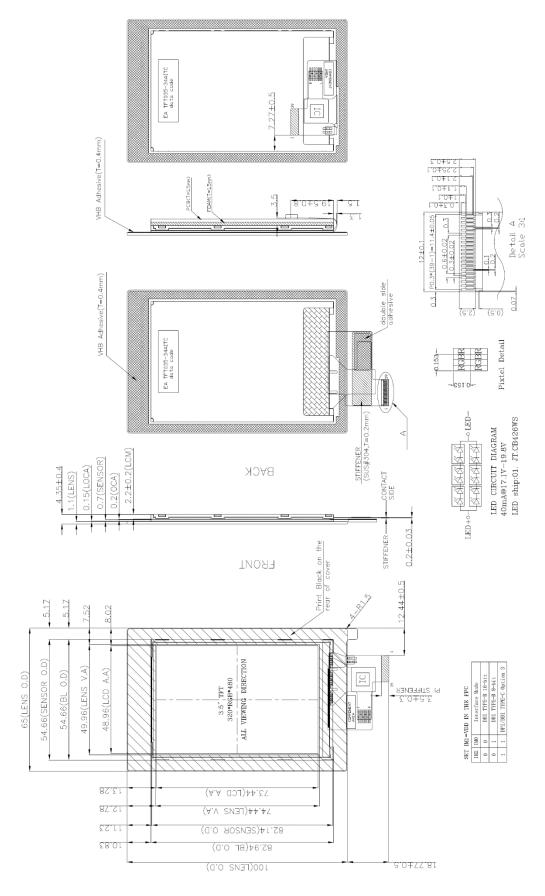
### 2.1 MECHANICAL DRAWING EA TFT035-34AINN







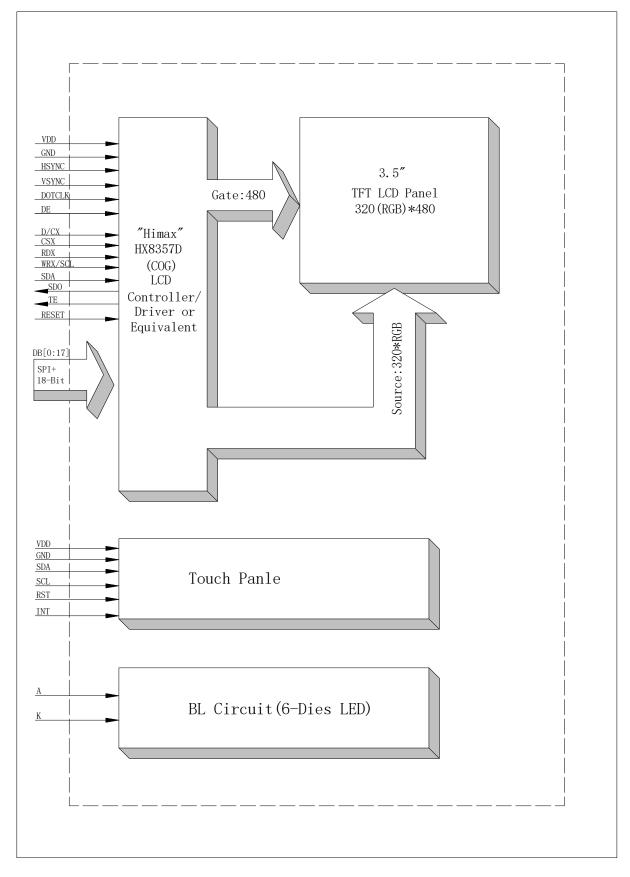
### 2.2 MECHANICAL DRAWING EA TFT035-34AITC (with PCAP)







### **3. BLOCK DIAGRAM**







### **4. INTERFACE PIN FUNCTION**

Symbol	Description
LED-	Cathode of LED backlight.
LED+	Anode of LED backlight.
VDD / TOUCH VDD	Power supply for analog voltage.
GND / TOUCH GND	Power ground.
D0~D5	Data bus or B0B5
D6~D11	Data bus or G0G5
D12~D17	Data bus or R0R5
	Data enable signal in RGB interface.
DOTCER	If this pin is not used, connect it to GND.
	A data ENABLE signal in RGB mode.
	If this pin is not used, connect it to GND.
HSYNC	Horizontal synchronizing signal in RGB interface.
Потно	If this pin is not used, connect it to GND.
VSYNC	Vertical synchronizing signal in RGB interface.
Volito	If this pin is not used, connect it to GND.
TE	Tearing effect output.
	If not used, please open this pin.
	Chip select signal.
CSX	Low: chip can be accessed;
	High: chip cannot be accessed.
	If this pin is not used, connect it to VDD
204	Serial data input pin and output pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal.
SDA	If not used, please let it open.
	Serial data output.
	If bit SDO_EN=0, SDO is not use.
SDO	If bit SDO_EN=1, SDO is serial data output.
	If not used, please let it open.
	MPU, SPI-4 line: Data / Command Selection pin.
D/CX	If this pin is not used, connect it to GND.
	MPU mode: Serves as a write signal and write data at the low level.
WRX/SCL	SPI mode: it servers as SCL (Serial Clock)
	If this pin is not used, connect it to GND.
RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
IMO	Note
IM2	Note
אחש	MPU mode: Serves as a read signal and read data at the low level.
KDA	If this pin is not used, connect it to GND.
TOUCH CLK	I2C clock input ( EA TFT035-34AITC only)
TOUCH SDA	I2C data input and output (EA TFT035-34AITC only)
TOUCH INT	Interrupt request to the host or Wakeup request from the host (EA TFT035-34AITC only)
	LED- LED+ VDD / TOUCH VDD GND / TOUCH GND D0~D5 D6~D11 D12~D17 DOTCLK ENABLE HSYNC VSYNC TE CSX SDA SDA SDA D/CX WRX/SCL RESET IM0 IM2 RDX TOUCH CLK TOUCH CLK TOUCH SDA

#### Note

IM2	IMO	Interface Mode (IM1 is connected with VDD internally)
0	0	16-bit bus DBI TYPE-B
0	1	8-bit bus DBI TYPE-B
1	1	16 Bit RGB DPI/DBI TYPE-C Option 3



### **5. ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Supply voltage for analog	VCC	-0.3	4.6	V
Supply voltage for logic	IOVCC	-0.3	4.6	V
Supply current (LED)	ILED		60	mA
Operating temperature	T <sub>OP</sub>	-20	+70	°C
Storage temperature	T <sub>ST</sub>	-30	+80	°C

## **6. ELECTRICAL CHARACTERISTICS**

#### 6.1 INPUT POWER

Item	Symbol	Min	Тур.	Max	Unit
Supply Voltage for Analog	VCC	2.5	2.8	3.3	V
Supply Voltage for Logic	IOVCC	1.65	1.8/2.8	3.3	V
	VIL	GND	-	0.3IOVCC	V
Input Voltage	Vih	0.7 IOVCC	-	IOVCC	V
Input leakage Current	Ilkg	-1		1	μA

### **6.2 BACKLIGHT DRIVING CONDITIONS**

ltem	Symbol	Value			Unit	Remark	
item	Symbol	Min.	Тур.	Max.	Onit	Kennark	
Voltage for LED Backlight	VF	17.1	19.2	19.8	V	I <sub>LED</sub> =40mA	
Current for LED Backlight	I <sub>LED</sub>		40		mA		
Power Consumption	Р		0.768		W		
LED Life Time		30,000			Hr	Note	

Note: Brightness to be decreased to 50% of the initial value at ambient temperature  $T_A=25^{\circ}C$ 





### **6.3 PCAP ELECTRICAL CHARACTERISTICS**

FPC Design	ltem	Description	Remark
	IC solution on TP Model	GT911	
	Touch Count Max	5 Point	
COF	Display Resolution	320*480	
COF	Interface Type	I2C	
	I2C Slave Address	0xBA/0xBB	
	Origin of Coordinate	Top left corner	

Parameter	Symbol	Min	Тур.	Max	Unit
Interface Signal for Analog	VDD	2.7	3.3	3.6	V
Supply Voltage for Logic	IOVCC	1.71	3.3	3.6	V





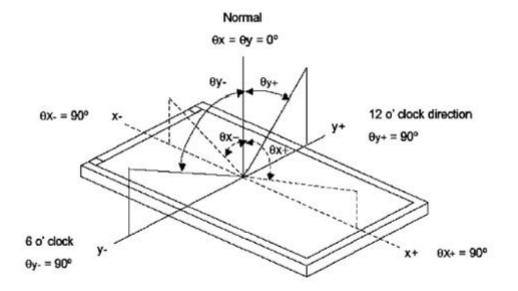
## 7. OPTICAL CHARACTERISTICS

ITEN	ITEM		CONDITIONS	SPE	CIFICATI	ONS	UNIT
		SYMBOL CONDITIONS		MIN	TYP.	MAX	UNIT
Lumina			EA TFT035-43-AINN	800	1000	1400	cd/m²
Lumina	nce	L	EA TFT035-43-AITC	510	850	1200	cd/m²
Contrast	Ratio	CR	θ=0°		700		
Deepenag	Response Time		25%		20		
Response			25°C		30		ms
CIE Colo		Xw		0.27	0.31	0.35	
Coordin		Yw		0.32	0.36	0.40	
	Hor.	$ heta_{_{X+}}$	CR≥10 -		80		
Viewing	Hor.	$ heta_{_{X-}}$			80		Degree
Angle	Vor	$ heta_{_{Y+}}$	CK210		80		Degree
	Ver.	$ heta_{_{Y-}}$			80		
Uniform	nity			80			%





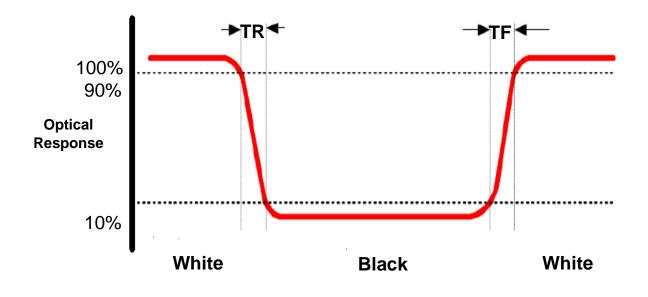
#### Note 1: Definition of Viewing Angle $\theta x$ and $\theta y$ :



#### Note 2: Definition of contrast ratio CR:

$$CR = \frac{Luminance of white state}{Luminance of black state}$$

Note 3: Definition of Response Time(Tr,Tf)



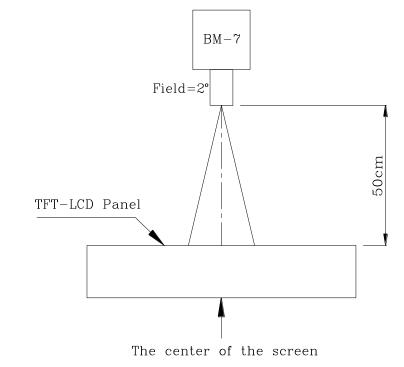




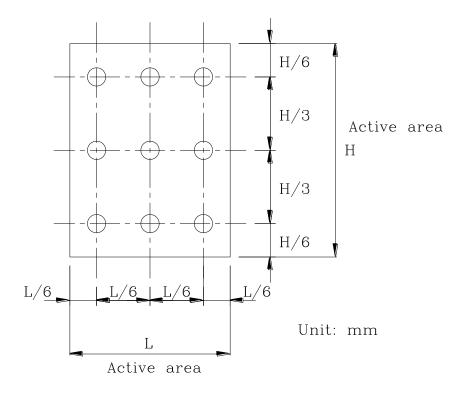
#### Note 4: Definition of Luminance

**(1)**The Brightness Test Equipment Setup

Field=2°(As measuring "black" image, field=2° is the best testing condition)



### (2) The Brightness Test Point Setup







### 8. TIMING CHARACTERISTICS

### **8.1 SPI INTERFACE CHARACTERISTICS**

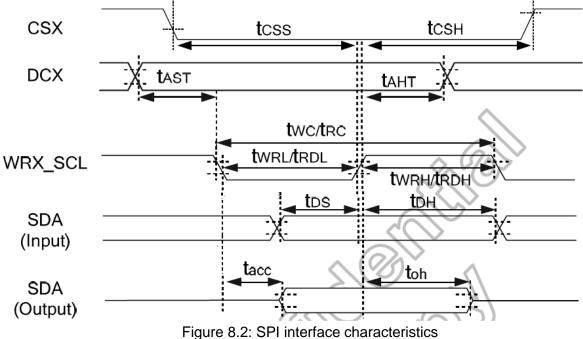


Figure 6.2. SFT interface characteristics

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
	tcss	Chip select setup time (Write)	15	-		
CSX	tcss	Chip select setup time (Read)	60	-	ns	_
007	tcsH	Chip select hold time (Write)	15	-	115	-
	<b>t</b> csн	Chip select hold time (Read)	65	-		
DCX	<b>t</b> ast	Address setup time	0	-	ns	
DCX		Address hold time (Write/Read)	10	-	115	-
WRX SCL	twc	Write cycle	66	-		
(Write)	twrn	Control pulse "H" duration	15	-	ns	-
(write)	twrl	Control pulse "L" duration	15	-		
WRX_SCL	tRC	Read cycle	150	-		
(Read)	trdh	Control pulse "H" duration	60	-	ns	-
(Iteau)	trol	Control pulse "L" duration	60	-		
SDA 🔿	tos	Data setup time	10	-	20	
(Input)	ton	Data hold time	10	-	ns	For maximum C∟=30pF
SDA	SDA tAcc Read access time		10	50	ns	For minimum C∟=8pF
(Output)	tон	Output disable time	15	50	115	

Table 8.2: SPI interface characteristics

**Note**: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.





#### **8.2 RGB INTERFACE CHARACTERISTICS**

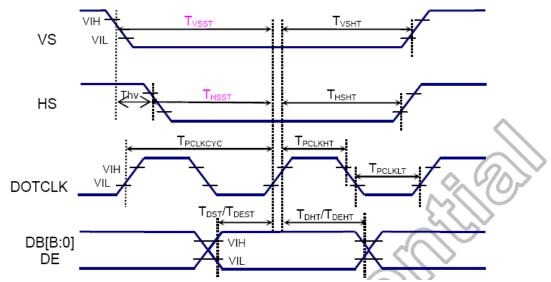


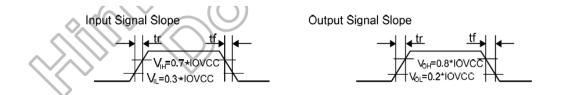
Figure 8.3: RGB interface characteristics

#### (GND=0V, IOVCC=1.8V, VCI=2.8V, TA=25°C, Sleep Out states)

ltem	Symbol	Condition			Unit	
Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Pixel low pulse width	T <sub>CLKLT</sub>	(S)	15 🦯	$\sum$	-	ns
Pixel high pulse width	T <sub>CLKHT</sub>		15		-	ns
Vertical Sync. Set-up time	T <sub>VSST</sub>		15	<b>&gt;</b> -	-	ns
Vertical Sync. Hold time	T <sub>VSHT</sub>		15	-	-	ns
Horizontal Sync. Set-up time	T <sub>HSST</sub>		15	-	-	ns
Horizontal Sync. Hold time	T <sub>HSHT</sub>	$\mathcal{I}$ - $\mathcal{I}$	15	-	-	ns
Data Enable set-up time	TDEST	2	15	-	-	ns
Data Enable hold time	TDEHT		15	-	-	ns
Data set-up time	T <sub>DST</sub>		15	-	-	ns
Data hold time	T <sub>DHT</sub>		15	-	-	ns
Phase difference of sync signal falling edge	PThv (	2	0	-	320	Dotclk

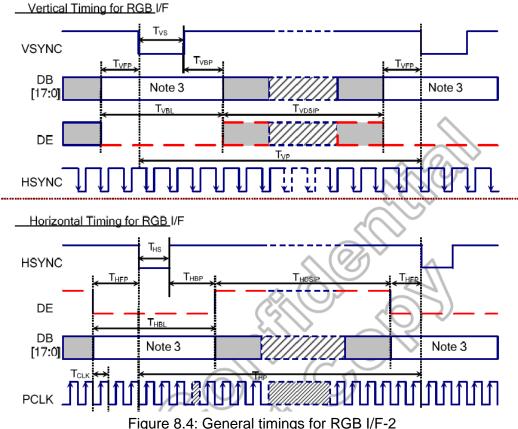
Table 8.3: RGB interface characteristics

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.









ltem	Symbol	Condition	S	Specificatio	n	Unit
item	Symbol	Condition	Min.	Тур.	Max.	
Vertical Timing						
Vertical cycle period	O T <sub>VP</sub>	<b>-</b>	486	-	-	HS
Vertical low pulse width	Tvs		2	-	-	HS
Vertical front porch	TVFP	)) -	2	-	-	HS
Vertical back porch	TVBP	-	2	-	-	HS
Vertical blanking period	T <sub>VBL</sub>	T <sub>VS</sub> + T <sub>VBP</sub> + T <sub>VFP</sub>	6	-	-	HS
			-		-	HS
Vertical active area	TVDISP	-	-	480	-	HS
	· ·		-		-	HS
Vertical refresh rate	T <sub>VRR</sub>	Frame rate	50	60	70	Hz
Horizontal Timing						
Horizontal cycle period	T <sub>HP</sub>	-	335	-	-	DOTCLK
Horizontal low pulse width	T <sub>HS</sub>	-	5	-	-	DOTCLK
Horizontal front porch	T <sub>HFP</sub>	-	5	-	-	DOTCLK
Horizontal back porch	T <sub>HBP</sub>	-	5	-	-	DOTCLK
Horizontal blanking period	T <sub>HBL</sub>	T <sub>HS</sub> +T <sub>HBP</sub> + T <sub>HFP</sub>	15	-	-	DOTCLK
Horizontal active area	T <sub>HDISP</sub>	-	-	320	-	DOTCLK
Pixel clock cycle TVRR=60Hz	fclkcyc	-	9	-	-	MHz

Table 8.4: RGB interface characteristics-2

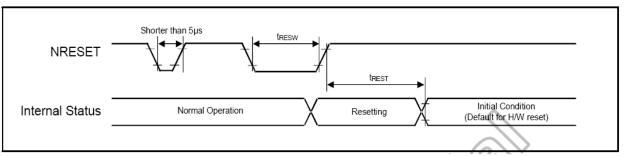
Note: (1) IOVCC=1.65 to 3.3V, VCI=2.3 to 3.3V, VSSA=VSSD=0V, Ta=-30 to 70°C (2) Data lines can be set to "High" or "Low" during blanking time – Don't care.

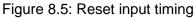
(3) HP is multiples of PCLK.





#### **8.3 RESET INPUT TIMING**





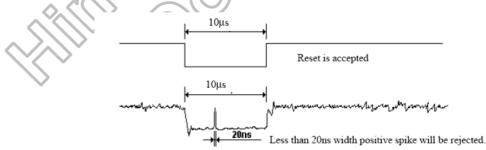
Symbol	Parameter	Related Spec.				Note	Unit
Symbol	Symbol Farameter		Min.	Тур.	Max.	Note	onit
tRESW	Reset low pulse width <sup>(1)</sup>	NRESET	10	-	~~	✓ -	μs
tREST	Reset complete time <sup>(2)</sup>	-	5	K	$\otimes$	When reset applied during SLPIN mode	ms
INEOT	Reset complete time	-	120	$\odot$		When reset applied during SLPOUT mode	ms

#### Table 8.5: Reset input timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
- (3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown as below:



01. It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.





## 9. PCAP TOUCHPANEL

	Table 9	
Item	Specification	Unit
Touch panel Size	3.5	inches
Active Area (Sensor)	49.0 (H) x 73.5 (V)	mm
Input type	Multi touch	
Controller	GT911	
Interface mode	I <sup>2</sup> C	
Normal mode operating current	Тур. 8	mA

### 9.1 TIMING SPECIFICATIONS FOR CTP

#### I<sup>2</sup>C Communication

This module provides standard I2C interface for communication. In the system, this module always works in slave mode, all communications are initiated by master, and the baud rate can be up to 400K bps. The definition of I<sup>2</sup>C timing is as following:

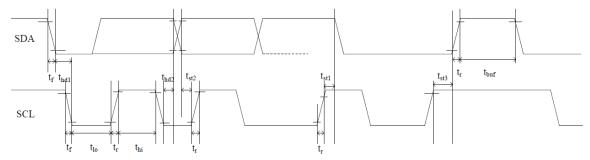


Fig.6 RGB Interface Timing Characteristics Test condition: 3.3V communication interface, 400Kbps, pull up resistor is 2K ohm

Parameter	Symbol	MIN.	Max.	Unit
SCL low period	t <sub>lo</sub>	0.9	-	us
SCL high period	t <sub>hi</sub>	0.8	-	us
SCL setup time for START condition	t <sub>st1</sub>	0.4	-	us
SCL setup time for STOP condition	t <sub>st3</sub>	0.4	-	us
SCL hold time for START condition	t <sub>hd1</sub>	0.3	-	us
SDA setup time	t <sub>st2</sub>	0.4	-	us
SDA hold time	t <sub>hd2</sub>	0.4	-	us

This module has 2 sets of slave address 0xBA/0xBB & 0x28/29. Master can control Reset & INT pin to configure the slave address in power on initial state like following:





#### Power on diagram:

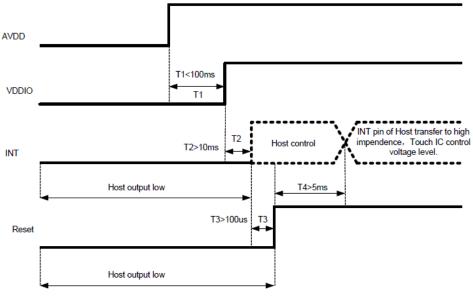


Fig.7 Power on diagram

#### Timing of setting slave address to 0x28/0x29:

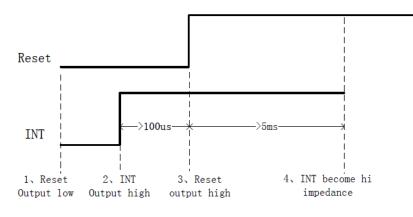
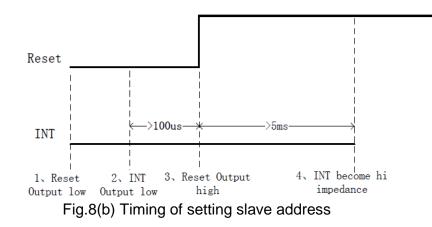


Fig.8(a) Timing of setting slave address

#### Timing of setting slave address to 0xBA/0xBB:









#### Data Transmission

(ex: slave address is 0xBA/0xBB)

Communication is always initiated by master, A high-to-low transition of SDA with SCL high is a start condition.

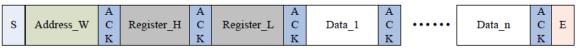
All addressing signal are serially transmitted to and from on bus in 8-bit word. This module sends a "0" to acknowledge when the addressing word is 0xBA/BB (or 0x28/0x29). This happens during the ninth clock cycle. If the slave address is not matched, this module will stay in idle state.

The data words are serially transmitted to and from in 9-bit formation: 8-bit data+1-bit ACK or NACK sent by module. Data changes during SCL low periods & keeps valid during SCL high.

A low-to-high transition of SDA with SCL high is a stop condition.

#### Write Data to module

(ex: slave address is 0xBA/0xBB)



Please check the above figure, master start the communication first, and then sends device address 0XBA preparing for a write operation.

After receiving ACK from module, master sends out 16-bit register address, and then the data word in 8-bit, which is going to be wrote into module.

The address pointer of module will automatically increase one after one byte writing, so master can sequentially write in one operation. When operation finished, master stop the communication.

#### Read Data from module

(ex: slave address is 0xBA/0xBB)

S Address_W	A C Register_H K	A C Register_L K	A C K	E	s	Address_R	A C K	Data_1	A C K		Data_n	N A C K	E
	→Set start register	address ┥						→ Re	ad dat	a ┥			

Please check the above figure, master start the communication first, and then sends device address 0xBA for a write operation.

After receiving ACK from module, master sends out 16-bit register address, to set the address pointer of module. After receiving ACK, master produce start signal once again & send device address 0xBB, then read data word from module in 8-bit.

Module also supports sequential read operation, and the default setting is sequential read mode. Master shall send out ACK after every byte reading successfully but NACK after the last one. Then sends stop signal to finish the communication.





#### 9.2 REGISTER INFORMATION

#### a) Real Time Order

(Write	Only)

Addr	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x8040	Command		aseline	update	read diff o 4: baselir t				

#### **b)** Configuration Information

(R/W)

	Config Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
0x8047	Config_ Version	Version of the configuration								
0x8048	X Output Max (Low Byte)				Posolutio	on of V avi	c .			
0x8049	X Output Max (High Byte)	Resolution of X axis								
0x804A	Y Output Max (Low Byte)									
0x804B	Y Output Max (High Byte)				Resolutio	on of Y axi	5			
0x804C	Touch Number		Res	erved			Touch nu	imber: 1~5		
0x804D	Module_ Switch1	Res	served	Streto	:h_rank	X2Y	Reser ved	INT trigger 00: risin trigg 01: fallin trigg	g edge jer ig edge	





								02: low level enquiry 03: high level enquiry
0x804E	Module_ switch2	Reserved						
0x804F	Shake_Count		Res	erved			Finger s	hake count
0x8050	Filter	First_	Filter	Nor	_	(filtering va ndow, coe		iginal coordinate is 1)
0x8051	Large_Touch			Nur	mber of tou	ich in large	e area	
0x8052	Noise_ Reduction		Res	erved		Value of		mination (coefficient , 0~15)
0x8053	Screen_ Touch_Level		Threshold of touch grow out of nothing					g
0x8054	Screen_ Leave_Level		Threshold of touch grow out of nothing					g
0x8055	Low_Power_ Control		Reserved				wer consumption ~15s)	
0x8056	Refresh_Rate		Reserved			Coordinate report rate (Cycle: 5+N ms)		
0x8057	x_threshold		Reserved					
0x8058	y_threshold							
0x8059	X_Speed_Limit				Res	erved		
0x805A	Y_Speed_Limit							
0x805B		Bla		of boarder		Blan		Boarder-bottom
	Space			ent is 32)		(coefficient is 32)		
0x805C		Bla		of boarder		Bla		of Boarder-right
0x805D	Stretch_Rate		(coefficient is 32) Reserved		(coefficient is 32) Level of weak stretch (Stretch X/16 Pitch) (beta version is valid, published version is not)		retch (Stretch X/16 itch) s valid, published	
0x805E	Stretch_R0	Interval 1 coefficient						
0x805F	Stretch_R1	Interval 2 coefficient						
0x8060	Stretch_R2	Interval 3 coefficient						
0x8061	Stretch_RM			A	II intervals	base num	ber	
0x8062	Drv_GroupA_ Num	All_Dr iving	Rese	erved		Driver_(	Group_A	_number
0x8063	Drv_GroupB_	l	Reserved	I		Driver_(	Group_B	number

DIS	PLAY
ELECTRON	IIC ASSEMBLY
<b>VIS</b>	IONS



	Num							
0x8064	Sensor_Num	Se	nsor_Group_B_Nu	mber	Ser	nsor_Grou	up_A_Number	
0x8065	FreqA factor	0	Driver frequency do	uble freque	ency coeffi	cient of D	river group A	
0,0005	rieqA_lactor		GroupA_Free	quence = N	Aultiplier fa	ctor * bas	eband	
0x8066	FreqB factor		Driver frequency do	uble freque	ency coeffi	cient of D	river group B	
0,0000	Treqb_lactor		GroupB_Free	quence = N	Aultiplier fa	ctor * bas	eband	
0x8067	Pannel_							
0,0001	BitFreqL		Baseband of Driver	aroup A\F	3 (1526HZ<	<baseban< td=""><td>d&lt;14600Hz)</td></baseban<>	d<14600Hz)	
0x8068	Pannel_			3				
	BitFreqH							
0x8069	Pannel_Sensor							
	_TimeL	Time	e interval of the neil	bouring tw	o driving si	gnal (Unit	: us), Reserved.	
0x806A	Pannel_Sensor							
	_TimeH					-		
				Pannel	Drv_outp	Pan	nel_DAC_Gain	
0x806B	Pannel_Tx_ Gain	Reserved			R		Sain maximum	
				4 gears		7: (	Gain minimum	
0x806C	Pannel_Rx_	Pann		Pannel_	Rx_Vcmi	Pannel_PGA_Gain		
UX806C	Gain	el_PG A_C	Pannel_PGA_R	(4 ge	ears)		(8 gears)	
	Pannel_Dump_	~_0			Magnifi	ication cor	efficient of original	
0x806D	Shift		Reserved		-		th power of 2)	
	Drv Frame	Reser			Van			
0x806E	Control	ved	Sub	Frame_Dr	vNum		Repeat_Num	
0x806F	NC			Res	served			
0x8070	NC			Res	served			
0x8071	NC			Res	served			
0.0070	Stylus_Tx_						0	
0x8072	Gain		Undefined	(invalid	when stylu	s_priority	=0)	
0.0070	Stylus_Rx_		11-1-5				0)	
0x8073	Gain		Undefined	(invalid	when stylu	s_priority	=0)	
0,2074	Stylus_Dump_	Marri	ifaction coefficient	of original	volue (The	Nith news	ar of 2) Bassaud	
0x8074	Shift	Magh	ification coefficient	oronginal	value (The	inter powe	er of 2), reserved	
0x8075	Stylus_Driver_T		Stylus effe	etive three	hold (drivin	a) Reserve	wed	
0x00/5	ouch_Level		Stylus effe	cave unes	noia (anvin	ig), Reser	ved	
0x8076	Stylus_Sensor_		Stylus effect	tive three	old (eeneir	na) Reco	nved	
0,0070	Touch_Level		Stylus ellet	are unesi	ioid (acrial	ng), nese		
0x8077	Stylus_	Pen mode escape time out period (Unit: Sec)					Sec)	
0,0011	Control		Fermode	cocape un	io out pent	ou (onic a		
0x8078	Base_reduce	S-	Style improve quan	tity		Rese	rved	
0x8079	NC			Res	served			





0x807A	Freq_Hopping_ Start	Frequency hopping start frequency (Unit: 2KHz, 50 means 100KHz)					
0x807B	Freq_Hopping_ End	Freque	Frequency hopping stop frequency (Unit: 2KHz, 150 means 300KHz)				
0x807C	Noise_Detect_T imes		Detect_Stay_Ti mes Detect_Confirm_Times				
0x807D	Hopping_Flag	Hoppi ng_E n	Reserved		Detect_Time_Out		
0x807E	Hoppging_ Threshold	Large_N	Large_Noise_Threshold Hopping_Hit_Threshold				
0x807F	Noise_ Threshold		Threshold of noise level				
0x8080	NC	Reserved					
0x8081	NC				Reserved		
0x8082	Hopping_seg1_ BitFreqL	Freque					
0x8083	Hopping_seg1_ BitFreqH	Freque	ancy no	pping segn	nent band 1 central frequency (for driver A/B)		
0x8084	Hopping_seg1_ Factor	Fr	requent	cy hopping	segment 1 central frequency coefficient		
0x8085	Hopping_seg2_ BitFreqL	Freque	ency ho	opina sean	nent band 2 central frequency (for driver A/B)		
0x8086	Hopping_seg2_ BitFreqH			ppg cog.			
0x8087	Hopping_seg2_ Factor	Fr	requent	cy hopping	segment 2 central frequency coefficient		
0x8088	Hopping_seg3_ BitFreqL	Freque	ency bo	nning segn	ent band 3 central frequency (for driver A/B)		
0x8089	Hopping_seg3_ BitFreqH	Frequency hopping segment band 3 central frequency (for driver A/B)					
0x808A	Hopping_seg3_ Factor	Frequency hopping segment 3 central frequency coefficient					
0x808B	Hopping_seg4_ BitFreqL	Freque	Frequency hopping segment band 4 central frequency (for driver A/B)				
0x808C	Hopping_seg4_						





	BitFreqH					
0x808D	Hopping_seg4_ Factor	Frequency hopping segment 4 central frequency coefficient				
0x808E	Hopping_seg5_ BitFreqL	Frequency hopping segment band 5 central frequency (for driver A/B)				
0x808F	Hopping_seg5_ BitFreqH		ia o contro	noquonoy (ioi anto: / co)		
0x8090	Hopping_seg5_ Factor	Frequency hopping segmer	nt 5 central	frequency coefficient		
0x8091	NC	Re	eserved			
0x8092	NC	Re	eserved			
0x8093	Key 1	Key 1 Position: 0-255 valid (0 mear key when 4 of the				
0x8094	Key 2	Key	2 position			
0x8095	Key 3	Key	3 position			
0x8096	Key 4	Key	4 position			
0x8097	Key_Area	Time limit for long press(1~16 s)	Touch valid interval setting: 0-15 valid			
0x8098	Key_Touch_Lev el	Key threshold of touch key				
0x8099	Key_Leave_Lev el	Key threshold of touch key				
0x809A	Key_Sens	KeySens_1(sensitivity coefficient of key 1, same below)	KeySens_2			
0x809B	Key_Sens	KeySens_3		KeySens_4		
0x809C	Key_Restrain	Finger from screen left after inhibition of key time(Unit:100ms,0 means 600ms)	The independent button pro key inhibition parameters			
0x809D	NC	Re	eserved			
0x809E	NC	Re	eserved			
0x809F	NC	Re	eserved			
0x80A0	NC	Re	eserved			
0x80A1	NC	Re	eserved			
0x80A2	Proximity_Drv_ Select	Drv_Start_Ch (start channel of driving direction) Drv_End_Ch (End channel				
0x80A3	Proximity_ Sens_Select	Sens_Start_Ch (start channel of sensing direction) Sens_End_Ch (End channel)				
0x80A4	Proximity_ Touch_Level	Proximity effective threshold value				
0x80A5	Proximity_ Leave_Level	Proximity ineffe	ctive thres	hold value		





	Drovinsity Comp	
0x80A6	Proximity_Samp le_Add_Times	Frequency multification of proximity sensing channel.
0x80A7	Proximity_Samp le_Dec_ValL	Sample value minus this value (16 bit), and accumulate, low byte.
0x80A8	Proximity_Samp le_Dec_ValH	Sample value minus this value (16 bit), and accumulate, high byte.
0x80A9	Proximity_Leav e_Shake_Count	exit proximity jitter count
0x80AA	Self_Cap_Tx_g ain	self-capacitance sends gains
0x80AB	Self_Cap_Rx_g ain	self-capacitance receive gains
0x80AC	Self_Cap_Dump _Shift	Magnification coefficient of original value of self-capacitance (The Nth power of 2)
0x80AD	SCap_Diff_Up_ Level_Drv	Self capacitance suppress floating rising threshold (driving direction)
0x80AE	Scap_Merge_T ouch_Level_Drv	Self-capacitance Touch Level (driving direction)
0x80AF	SCap_Pulse_Ti meL	Self-capacitance sampling time (low byte)
0x80B0	SCap_Pulse_Ti meH	Self-capacitance sampling time (high byte)
0x80B1	SCap_Diff_Up_ Level_Sen	Self capacitance suppress floating rising threshold (sensing direction)
0x80B2	Scap_Merge_T ouch_Level_Se n	Self-capacitance Touch Level (sensing direction)
0x80B3	NC	Reserved
0x80B4	NC	Reserved
0x80B5	NC	Reserved
0x80B6	NC	Reserved
0x80B7 ~ 0x80C4	Sensor_CH0~ Sensor_CH13	ITO Sensor corresponding chip channel number
0x80C5 ~ 0x80D4	NC	Reserved
0x80D5 ~ 0x80EE	Driver_CH0~ Driver_CH25	ITO Driver corresponding chip channel number
0x80EF ~	NC	Reserved





0x80FE					
0x80FF	Config_Chksum	configuration information verify (the complement number of total byte from 0x8047 to 0x80FE)			
0x8100	Config_Fresh	signal of updated configuration (the host writes)			

#### c) Coordinates Information

Addr	Access	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x8140	R			Produc	t ID (first b	yte, A	SCII)		
0x8141	R			Product	ID ( second	byte,	ASCI	)	
0x8142	R			Produc	t ID ( third b	yte, A	SCII)		
0x8143	R			Produc	t ID ( forth b	yte, A	SCII)		
0x8144	R			Firmwar	e version ( l	HEX.lov	w byte )	)	
0x8145	R			Firmware	version ( H	EX.hig	h byte )	)	
0x8146	R			x coordi	nate resoluti	ion ( lov	w byte )	)	
0x8147	R			x coordin	ate resoluti	on ( hig	ih byte	)	
0x8148	R			y coordir	nate resoluti	ion ( lov	w byte )	)	
0x8149	R			y coordin	ate resoluti	on ( hig	ih byte	)	
0x814A	R		Ve	ndor_id ( cu	rrent module	e optior	n inform	nation )	
0x814B	R				Reserve	ed			
0x814C	R				Reserve	ed			
0x814D	R				Reserve	ed			
0x814E	R/W	buffer status	large detect	Reserved		numb	er of to	uch point	5
0x814F	R				track is	1			
0x8150	R			point 1	x coordina	te (low	byte)		
0x8151	R			point 1	x coordinat	e (high	byte)		
0x8152	R			point 1	y coordina	te (low	byte)		
0x8153	R			point 1	y coordinat	e (high	byte)		
0x8154	R			Po	oint 1 size (le	ow byte	e)		
0x8155	R			ро	int 1 size (h	igh byte	e)		
0x8156	R				Reserve	ed			
0x8157	R		track id						
0x8158	R		point 2 x coordinate (low byte)						
0x8159	R		point 2 x coordinate (high byte)						
0x815A	R		point 2 y coordinate (low byte)						
0x815B	R		point 2 y coordinate (high byte)						
0x815C	R		point 2 size (low byte)						
0x815D	R			ро	int 2 size (h	igh byte	e)		
0x815E	R				Reserve	ed			





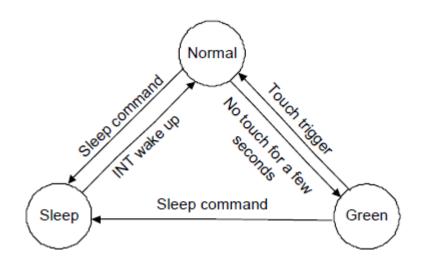
0x815F	R	track id
0x8160	R	point 3 x coordinate (low byte)
0x8161	R	point 3 x coordinate (high byte)
0x8162	R	point 3 y coordinate (low byte)
0x8163	R	point 3 y coordinate (high byte)
0x8164	R	point 3 size (low byte)
0x8165	R	point 3 size (high byte)
0x8166	R	Reserved
0x8167	R	track id
0x8168	R	point 4 x coordinate (low byte)
0x8169	R	point 4 x coordinate (high byte)
0x816A	R	point 4 y coordinate (low byte)
0x816B	R	point 4 y coordinate (high byte)
0x816C	R	point 4 size (low byte)
0x816D	R	point 4 size (high byte)
0x816E	R	Reserved
0x816F	R	track id
0x8170	R	point 5 x coordinate (low byte)
0x8171	R	point 5 x coordinate (high byte)
0x8172	R	point 5 y coordinate (low byte)
0x8173	R	point 5 y coordinate (high byte)
0x8174	R	point 5 size (low byte)
0x8175	R	point 5 size (high byte)
0x8176	R	Reserved
0x8177	R	Reserved
-		





9.3 FUNCTION MODE

Working Mode



#### a) Normal Mode

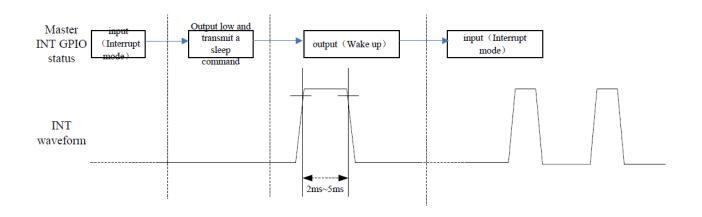
When module is in Normal mode, touch scanning period is about  $7ms \sim 10ms$  depending on the setting. The chip will automatically enter into Green mode if no touch for short time within  $0\sim15s$  depending on setting and the step is 1s.

#### b) Green Mode

In Green mode, the touch scanning cycle is fixed as 40ms. It will automatically enter into Normal mode if any touch is detected.

#### c) Sleep Mode

For a lower consumption, Master can ask module to enter Sleep mode through I2C command (before the command, please drive low to INT pin). Drive high to the INT pin of module 2~5ms will make module return back to normal mode.



#### Pulse Calling

Module will inform master to read coordinate information only when touch event happen, in order to lighten the burden of master CPU. The master CPU will set trigger mode by register "INT". "0" means rising edge trigger, in this mode module will output a rising edge hopping in INT, to inform CPU; "1" means falling edge trigger.







#### Sleep Mode

When the display is turned off or in any circumstance that operation of touch panel is not necessary, master can set module be in Sleep mode through I2C command. The master can wake up module by outputting high to INT pin & keeping 2-5ms.

#### Frequency Hopping Function

This module has very strong anti-interference hardware, when the driver spectrum of module overlaid with spectrum of noise signal, it can be switch to another frequency by self-adaption frequency hopping mechanism, to avoid interference.

Automatic Calibration

#### a) Initialization Calibration

Different temperature, humidity and physical structure will affect the sensor's baseline. According to environmental situation module will update the baseline automatically in initialized 200ms.

#### b) Automatic Temperature Drift

Slow change of temperature, humidity or dust and other environmental factors will also affect the sensor's baseline module calculates and analyses historical data, and compare to the current data variation. Base on this, the baseline will be calibration automatically.

For more information, refer to the data sheet GT911: https://www.lcd-module.de/fileadmin/eng/pdf/zubehoer/GT911%20Datasheet\_English%2020150625\_Rev10.pdf.



### **10. STANDARD SPECIFICATION FOR RELIABILITY**

### **10.1 STANDARD SPECIFICATION FOR RELIABILITY OF LCD MODULE**

NO.	ltem	Criterion	AQL				
01	Electrical Testing	<ul> <li>1.1 Missing vertical, horizontal segment, segment contrast defect.</li> <li>1.2 Missing character, dot or icon.</li> <li>1.3 Display malfunction.</li> <li>1.4 No function or no display.</li> <li>1.5 Current consumption exceeds product specifications.</li> <li>1.6 LCD viewing angle defect.</li> <li>1.7 Mixed product types.</li> <li>1.8 Flicker</li> </ul>					
02	Black or White spots or Bright spots or Color spots on LCD (Display only)	2.1 White and black or color spots on display $\leq 0.25$ mm, no more than Five spots. 2.2 Densely spaced: No more than three spots within 3mm. 3.1 Round type: As following drawing					
	LCD and Touch Panel black spots,	$\Phi = (X+Y) / 2$ $\boxed{\begin{array}{c c} Size(mm) & Acceptable Q'ty \\ \hline \Phi \leq 0.10 & Accept no dense \\ \hline 0.10 < \Phi \leq 0.20 & 2 \\ \hline 0.20 < \Phi \leq 0.25 & 2 \\ \hline 0.25 < \Phi \leq 0.30 & 1 \\ \hline 0.30 < \Phi & 0 \\ \end{array}}$ $\overrightarrow{A}$ $A$	1.5				
03	white spots, contamination (non – display)	3.2 Line type: (As following drawing) $ \begin{array}{c c c c c c c c c c c c c c c c c c c $	1.5				



NO.	Item	Criter	ion		AQL
04	Polarizer bubbles	If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction	Size Φ(mm)           Φ≦0.20           0.20< Φ≦0.50           0.50< Φ≦1.00           1.00< Φ           Total Q'ty	Acceptable Q'ty Accept no dense 3 2 0 3 3	1.5
05	Scratches	Follow NO.3 -2 Line Type.			
06	Chipped glass	Symbols: x: Chip length y: Chip width z: Chip k: Seal width t: Glass thickness a: LC L: Electrode pad length 6.1 General glass chip: 6.1.1 Chip on panel surface and crack bet $\overrightarrow{z}$ Chip thickness y: Chip width $\overrightarrow{Z} \leq 1/2t$ Not over viewing $1/2t < z \leq 2t$ Not exceed 1/3 $\odot$ Unit: mm $\bigcirc$ If there are 2 or more chips, x is the tot: 6.1.2 Corner crack: $\overrightarrow{z} \leq 1/2t$ Not over viewing $1/2t < z \leq 2t$ Not exceed 1/3 $\overbrace{z} = 1/2t$ Not over viewing $1/2t < z \leq 2t$ Not exceed 1/3 $\overbrace{z} = 1/2t$ Not over viewing $1/2t < z \leq 2t$ Not exceed 1/3 $\overbrace{z} = 1/2t$ Not over viewing $1/2t < z \leq 2t$ Not exceed 1/3 $\bigcirc$ Unit: mm $\bigcirc$ If there are 2 or more chips, x is the tot: 1/3 $\overbrace{z} = 1/2t$ Not over viewing $1/2t < z \leq 2t$ Not exceed 1/3 $\overbrace{z} = 1/2t$ Not exceed 1/3	ween panels: x: Chip lengt area $x \le 1/8a$ al length of each chip x: Chip lengt $x \le 1/8a$ $x \le 1/8a$ $x \ge 1/8a$	h	1.5





NO.	Item	Criterion	AQL				
		Symbols: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length 7.2 Protrusion over terminal: 7.2.1 Chip on electrode pad:					
		y: Chip width x: Chip length z: Chip thickness					
		y≦0.5mm x≦1/8a 0< z≦t					
		7.2.2 Non-conductive portion:					
07	Glass crack	y z z y z z z x	1.5				
		y: Chip width x: Chip length z: Chip thickness					
		y≦L x≦1/8a 0< z≦t					
		⊂ remai ⊙ If the mot b	<ul> <li>If there chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.</li> <li>If the product will be heat sealed by the customer, the alignment mark must mot be damaged.</li> <li>7.2.3 Substrate protuberance and internal crack</li> </ul>				
		y: width x: length					
		y≦1/3L X≦a					





NO.	ltem	Criterion	
08	Cracked glass	The LCD with any extensive crack is not acceptable.	
09	Backlight elements	<ul> <li>9.1 Illumination source flickers when lit.</li> <li>9.2 Spots or scratches that appear when lit must be judged. Using LCD spot, lines and contamination standards.</li> <li>9.3 Backlight doesn't light or color is wrong.</li> </ul>	
10	Bezel	Bezel must comply with product specifications.	
11	PCB、COB	<ul> <li>11.1 COB seal may not have pinholes larger than 0.2mm or contamination.</li> <li>11.2 COB seal surface may not have pinholes through to the IC.</li> <li>11.3 The height of the COB should not exceed the height indicated in the assembly diagram.</li> <li>11.4 There may not be more than 2mm of sealant outside the seal area on PCB. And there should be no more than three places.</li> <li>11.5 Parts on PCB must be the same as on the production characteristic chart, There should be no wrong parts, missing parts or excess parts.</li> <li>11.6 The jumper on the PCB should conform to the product characteristic chart.</li> </ul>	
12	FPC	12.1 FPC terminal damage $\leq 1/2$ FPC terminal width and can not affect the function , we judge accept. 12.2 FPC alignment hole damage $\leq 1/2$ alignment area and can not affect the function , we judge accept.	
13	Soldering	13.1 No cold solder joints, missing solder connections, oxidation or icicle. 13.2 No short circuits in components on PCB or FPC.	





14       Touch Panel Chipped glass       O Unit: mm O If there are 2 or more chips, x is the total length of each chip 14.1.2 Comer crack:       1.5         14       Touch Panel Chipped glass       Chip thickness       y: Chip width       x: Chip length         14       Touch Panel Chipped glass       O Unit: mm O If there are 2 or more chips, x is the total length of each chip       1.5	NO.	Item	Criterion			AQL
≦1/2 k and not over	1/		x: Chip lengthy: Chip widthz: Chip thicknessk: Seal widtht: Touch Panel Total thicknessa: LCD side length14.1 General glass chip:14.1.1 Chip on panel surface and crack between panels:Image: transform of the second			1.5
			z: Chip thickness z≦t		x: Chip length x≦1/8a	





NO.	ltem	Criterion	
	Touch	SIZE(mm)Acceptable Q'ty $\Phi \leq 0.2$ Accept no dense $0.2 < D \leq 0.4$ 5 $0.4 < D \leq 0.5$ 2 $0.5 < D$ 0	4.5
15	Panel(Fish eye、dent and bubble on film)		1.5
16	Touch Panel Newton ring	Newton ring dimension $\leq 1/2$ touch panel area and not affect font and line distortion( $\leq 2.5\%$ ), it is acceptable.	
17	Touch Panel Linearity	Less than 2.5% is acceptable.	
18	LCD Ripple	Touch the touch panel , can not see the LCD ripple. Pen: R 1.0mm silicon rubber. Operation Force: 80g	
19	General appearance	<ul> <li>19.1 Pin type must match type in specification sheet.</li> <li>19.2 LCD pin loose or missing pins.</li> <li>19.3 Product packaging must the same as specified on packaging specification sheet.</li> <li>19.4 Product dimension and structure must conform to product specification sheet.</li> </ul>	





#### **10.2 TESTING CONDITIONS AND INSPECTION CRITERIA**

For the final test, the testing sample must be stored at room temperature for 24 hours. After the tests listed in table below, standard specifications for reliability will be executed in order to ensure stability.

No.	ltem	Test Model	In section Criteria
01	Current Consumption	Refer to Specification	The current consumption should conform to the product specification.
02	Contrast	Refer to Specification	After the tests have been executed, the contrast must be larger than half of its initial value prior to the tests.
03	Appearance	Visual inspection	Defect free.

#### 10.3 MTBF

MTBF	Functions, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (25±5°C), normal humidity (50±10% RH), and in area not exposed to direct sun light.
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## **11. SPECIFICATION OF QUALITY ASSURANCE**

This standard of Quality Assurance confirms to the quality of LCD module products supplied by ELECTRONIC ASSEMBLY.

### 11.1 QUALITY TEST

Before delivering, the supplier should conduct the following tests to confirm the quality of products.

Electrical-Optical Characteristics: According to the individual specification to test the product.

Appearance Characteristics: According to the individual specification to test the product.

Reliability Characteristics: According to the definition of reliability on the specification for testing products.

### 11.2 DELIVERY TEST

Before delivering, the supplier should conduct the delivery test.

Test method: According to MIL-STD105E. General Inspection Level II take a single Time.

The defects classify of AQL as following:

Major defect: AQL = 0.65Minor defect: AQL = 1.5Total defects: AQL = 1.5

### 11.3 NON-CONFORMING ANALYSIS & DEAL WITH MANNERS 11.3.1 NON-CONFORMING ANALYSIS

Purchaser should provide the data detail of non-conforming sample and the non-conforming.

After receiving the data detail from purchaser, the analysis of non-conforming should be finished within two weeks.

If the analysis can't be finished on time, supplier must notice purchaser 3 days in advance.

### 11.3.2 DISPOSITION OF NON-CONFORMING

If any product defect be found during assembling, supplier must change the good for every defect after confirmation.

Both supplier and customer should analyze the reason and discuss the disposition of non-conforming when the reason of nonconforming is not sure.







### **11.4 AGREEMENT ITEMS**

Both parties should negotiate together when the following problems happen. There is any problem of standard of quality assurance, and both sides should agree that it must be modified.

There is any argument item which does not record in the standard of quality assurance.

Any other special problem.

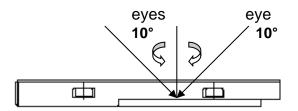
### 11.5 STANDARD OF THE PRODUCT APPEARANCE TEST 11.5.1 MANNER OF APPEARANCE TEST

The test must be under 20W × 2 or 40W fluorescent light, and the distance of view must be at  $30\pm5$ cm.

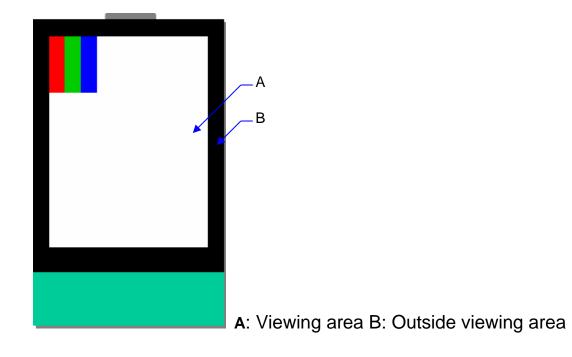
When test the model of transmissive product must add the reflective plate.

The test direction is base on around 10° of vertical line.

Temperature: 25±5°C Humidity: 60±10%RH



Definition of area:









### 11.5.2 BASIC PRINCIPLE

When the standard can not be described, AQL will be applied. The sample of the lowest acceptable quality level must be negotiated by both supplier and customer when any dispute happened. New item must be added on time when it is necessary.





### **12. HANDLING PRECAUTION**

### 12.1 HANDLING OF LCM

- Avoid external shock.
- Don't apply excessive force on the surface.
- Liquid in LCD is hazardous substance, do not lick or swallow. When the liquid is attaching to your hand, skin, cloth, etc., wash it thoroughly and immediately.
- Don't operate it above the absolute maximum rating.
- Don't disassemble the LCM.
- The operators should wear protections whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.
- The modules should be kept in antistatic bags or other containers resistant to static for storage.
- The module is coated with a film to protect the display surface, be careful when peeling off this protective film since static electricity may be generated.

### **12.2 STORAGE**

- Store it in an ambient temperature of 25±10°C, and in a relative humidity of 50±10% RH. Don't expose to sunlight or fluorescent light.
- Store it in a clean environment, free from dust, active gas, and solvent.
- Store it in anti-static electricity container.
- Store it without any physical load.

### **12.3 SOLDERING**

- Use only soldering irons with proper grounding and no leakage.
- Iron: not higher than 280±10°C and less than 3 sec during hand soldering.
- Rewiring: not more than 2 times.





### **13. INITIALISATION EXAMPLE RGB565**

SPI WriteComm(0x11)	; //Sleep Out
Delay(150);	
SPI_WriteComm(0xB9)	
SPI_WriteData(0xFF) SPI WriteData(0x83)	
SPI_WriteData(0x57)	
SPI WriteComm (0xB1)	
SPI WriteData (0x00)	
SPI WriteData (0x16)	; //
SPI_WriteData(0x1C)	
SPI_WriteData(0x1C)	
SPI WriteData(0xC3) SPI WriteData(0x5C)	
SFI_WIICEData (0x5C)	, //15 0244
SPI WriteComm (0xB3)	;
SPI_WriteData(0x43)	
SPI_WriteData(0x00)	
SPI_WriteData(0x06)	
SPI_WriteData(0x06)	;
SPI WriteComm(0xB4)	; //SETCYC
SPI WriteData (0x32)	
SPI_WriteData(0x40)	; //RTN
SPI_WriteData(0x00)	
SPI_WriteData (0x2A)	
SPI_WriteData(0x2A) SPI_WriteData(0x0D)	
SPI WriteData (0x78)	; //GDOFF
SPI WriteComm (0xB6)	
SPI_WriteData(0x3c)	;
SPI_WriteComm (0xB5)	
SPI_WriteData(0x0B)	
SPI_WriteData(0x0B)	;//08
SPI WriteComm (0xC0)	; //SETSTBA
SPI WriteData (0x70)	; //N OPON
SPI_WriteData(0x50)	; //I_OPON
SPI_WriteData(0x01)	
SPI_WriteData(0x3C)	
SPI_WriteData(0xC8) SPI WriteData(0x08)	
SPI WriteComm (0xCC)	
SPI_WriteData(0x0B)	
SPI_WriteComm(0xB6)	
SPI_WriteData(0x40)	; //0x40
SPI WriteComm(0xE0)	: //Set Gamma
SPI WriteData (0x02)	
SPI_WriteData(0x0A)	
SPI_WriteData(0x10)	
SPI_WriteData(0x1A) SPI WriteData(0x22)	
SPI_WriteData(0x22) SPI WriteData(0x34)	
SPI WriteData (0x41)	
SPI_WriteData(0x4A)	;
SPI WriteData (0x4D)	
SPI_WriteData (0x44)	
SPI_WriteData(0x3A) SPI WriteData(0x23)	
SPI WriteData (0x19)	
SPI WriteData (0x08)	
SPI WriteData(0x09)	
SPI_WriteData(0x03)	
SPI_WriteData(0x02)	
SPI_WriteData(0x0A) SPI WriteData(0x10)	
SPI_WriteData(0x10) SPI WriteData(0x1A)	
SPI WriteData (0x22)	
<pre>SPI_WriteData(0x34)</pre>	;
SPI_WriteData(0x41)	
SPI_WriteData(0x4A)	
SPI_WriteData(0x4D)	,







SPI WriteData(0x44); SPI\_WriteData(0x3A); SPI\_WriteData(0x23); SPI\_WriteData(0x19); SPI\_WriteData(0x08); SPI WriteData (0x09); SPI\_WriteData(0x03); SPI\_WriteData(0x00); SPI\_WriteData(0x01); SPI WriteComm(0xB4); //Display cycle register SPI\_WriteData(0x00); //Z-inversion disable, Cloumn inversion SPI WriteComm(0xB5); //SetBGP (TRI=0) SPI\_WriteData(0x03); //Vref = 4.4V
SPI\_WriteData(0x03); //nVREF = 4.4 V SPI WriteData (0x03); //VPP = 7.5 V, VDHS = 5.26 V SPI WriteComm (0xB6); SPI\_WriteData(0xB0); SPI\_WriteData(0x22); SPI WriteData (0x3B); SPI WriteComm(0x3A); //COLMOD SPI\_WriteData(0x55); //RGB565
SPI\_WriteComm(0x11); //Sleep out SPI WriteComm (0x13); //Normal display mode SPI WriteComm (0x29); //Display On