

Product Change Notification

(Notification - P1608044-DIGI) (CST-R2-AJ095) August 19, 2016

To: Our Valued Digi-Key, Inc. Customer

Overview: The purpose of this notification is to communicate a product change of select Renesas Electronics America, Inc. (REA) devices. These devices have suggested replacements.

Select SRAM products in SOP, μ TSOP, & BGA packages are undergoing a Speed and Temperature grade unification. Grades "-5SR", "-7SI", "-7SR" are being unified to single grade "-5SI".

There are no changes to reliability and quality levels. The replacement devices have superior electrical specifications, and also have the following changes (see Appendix for detailed changes)...

- 1. Final Test Site change from Renesas Semiconductor Beijing to Powertech Technology Inc.
- 2. Standardization of JEDEC trays and embossed tape.

Affected Products:

A review of our shipment records to your company indicate the attached list of products is affected by this notification.

Booking Part Number	Suggested Replacement Part Number
R1LP5256ESP-7SI#S0	R1LP5256ESP-5SI#S0
R1LV5256ESP-5SR#B0	R1LV5256ESP-5SI#B0
R1LV5256ESP-7SI#B0	R1LV5256ESP-5SI#B0

Part numbers given in this list are for active part numbers in REA database at the time of this notification.

Key Dates:

Final last time buy (LTB) orders of original part number placed to REA or to a franchised REA distributor.	Jun. 15 th , 2017
Planned date for last time shipment (LTS) of original part number from REA.	Dec 15 th , 2017

Response:

Please place last time buy (LTB) orders in a timely manner prior to the key dates listed to avoid product availability issues. If you anticipate volumes beyond your regular rate, please contact your REA sales representative with a forecast of your requirements. Shipments between the LTB and LTS dates are Non-Cancelable and Non-Returnable (NCNR).

Please contact your REA sales representative for any questions or comments.

Thank you for your attention.

Sincerely,

Renesas Electronics America, Inc.



Appendix A: Change Details

(1) 28pin-SOP 256Kb(5V) Part name: R1LP5256ESP

Item		Pre Change	Post Change
Orderable	part name	R1LP5256ESP-5SI/-5SR/-7SI/-7SR#B0 (Magazine packing)	R1LP5256ESP-5SI#B0 (Magazine packing)
Orderable part flame		R1LP5256ESP-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP5256ESP-5SI#S0 (Tape & Reel packing)
Assembly I	line	Renesas Semiconductor Beijing (China)	←
JEITA Pack	kage Code	P-SOP28-8.4x17.5-1.27	←
Package m		NUMBER N	RILP5256ESP Part name -5\$1 Electrical characteristics
	Lead frame	42Alloy	←
Assembly	material Lead plating	Sn-Cu	←
Assembly Material	Die bonding	Epoxy paste	←
rater rai	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	-
Final test li	ine	Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP024PC	←
Magazine packing	Storage number Number of	30pcs/magazine	←
	magazines (Max.) Inner box size	40 magazines	←
	(LxWxH) Packing	600mm x 172mm x 77mm	595mm x 170mm x 72mm
	specification Embossed	Current specification	New specification
Tano e.	tape	Emboss type name: MTE2416H-28P2W-C	←
Reel			
Reel	Storage number	1,000pcs/reel	←
Tape & Reel packing	Storage number Inner box size (LxWxH)	1,000pcs/reel 347mm x 368mm x 54mm	← 362mm x 340mm x 60mm
Reel	Storage number Inner box size (LxWxH) proof		



Appendix A (cont.): Change Details
(2) 28pin-SOP 256Kb(3V) Part name : R1LV5256ESP

Item		Pre Change	Post Change
Orderable	nart name	R1LV5256ESP-5SI/-5SR/-7SI/-7SR#B0 (Magazine packing)	R1LV5256ESP-5SI#B0 (Magazine packing)
Orderable part name		R1LV5256ESP-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LV5256ESP-5SI#S0 (Tape & Reel packing)
Assembly	line	Renesas Semiconductor Beijing (China)	←
JEITA Pac	kage Code	P-SOP28-8.4x17.5-1.27	←
Package n specification		NUMBER N	NOTION AND ALL CODE XXXXXXXX Part name Flectrical characteristics
	Lead frame material	42Alloy	←
Assembly	Lead plating	Sn-Cu	←
Material	Die bonding	Epoxy paste	÷
r racer rai	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-Included)	←
Final test I	line	Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Talwan)
	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP024PC	←
Magazine packing	Storage number Number of	30pcs/magazine	←
	magazines (Max.) Inner box size	40 magazines	←
	(LxWxH) Packing	600mm x 172mm x 77mm	595mm x 170mm x 72mm
	specification Embossed	Current specification	New specification
Tape & Reel	tape Storage	Emboss type name : MTE2416H-28P2W-C	←
packing	number Inner box size	1,000pcs/reel 347mm x 368mm x 54mm	← 362mm x 340mm x 60mm
Moisture-	(LxWxH) proof	347mm x 368mm x 54mm MSL 2	362mm x 340mm x 60mm ←
performar			
Shipping I	apel	Current specification	No change in format (Changes in Renesas internal code)



(3) 32pin-SOP 1Mb(5V) Part name: R1LP0108ESN

Item		Pre Change	Post Change
Ordorable	nart name	R1LP0108ESN-5SI/-5SR/-7SI/-7SR#B0 (Magazine packing)	R1LP0108ESN-5SI#B0 (Magazine packing)
Orderable part name		R1LP0108ESN-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP0108ESN-5SI#S0 (Tape & Reel packing)
Assembly	line	Renesas Semiconductor Beijing (China)	←
JEITA Pac	kage Code	P-SOP32-11.4x20.75-1.27	←
Package n specificati	on	XXXXXXXX	XXXXXXXX Date code R1LP0108ESN Date rode Part name Electrical characteristics
	Lead frame material	Cu	←
Assembly	Lead plating	Sn (pure tin)	←
Material	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test I	line	Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Talwan)
	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP525PC	←
Magazine packing	number	25pcs/magazine	←
	Number of magazines (Max.) Inner box size	36 magazines	←
	(LxWxH) Packing	600mm x 172mm x 77mm	595mm x 170mm x 72mm
	specification Embossed	Current specification	New specification
Tape & Reel	tape Storage	Emboss type name : MTE3216H-32P2M-A	←
packing	number Inner box size	1,000pcs/reel	←
Moisture-	(LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
performar		MSL 3	←
Shipping I	abel	Current specification	No change in format (Changes in Renesas internal code)



(4) 32pin-SOP 1Mb(3V) Part name: R1LV0108ESN

Item		Pre Change	Post Change
Oudamble		R1LV0108ESN-5SI/-5SR/-7SI/-7SR#B0 (Magazine packing)	R1LV0108ESN-5SI#B0 (Magazine packing)
Orderable part name		R1LV0108ESN-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LV0108ESN-5SI#S0 (Tape & Reel packing)
Assembly	line	Renesas Semiconductor Beijing (China)	←
JEITA Pac	kage Code	P-SOP32-11.4x20.75-1.27	←
Package n specificati	on	XXXXXXXX	NAXXXXXXX Date code R1LV0108ESN Part name -5S1 Electrical characteristics
	Lead frame material	Cu	←
Assembly	Lead plating	Sn (pure tin)	←
Material	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test I	line	Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Talwan)
	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP525PC	←
Magazine packing	Storage number Number of	25pcs/magazine	←
	magazines (Max.) Inner box size	36 magazines	←
	(LxWxH) Packing	600mm x 172mm x 77mm	595mm x 170mm x 72mm
	specification Embossed	Current specification	New specification
Tape & Reel	tape Storage	Emboss type name : MTE3216H-32P2M-A	←
packing	number Inner box size	1,000pcs/reel	←
Moisture-	(LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
performar		MSL 3	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)



(5) 32pin-SOP 4Mb(5V) Part name: R1LP0408DSP

Item		Pre Change	Post Change
O-do-bloo		R1LP0408DSP-5SI/-5SR/-7SI/-7SR#B0 (Magazine packing)	R1LP0408DSP-5SI#B0 (Magazine packing)
Orderable part name		R1LP0408DSP-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP0408DSP-5SI#S0 (Tape & Reel packing)
Assembly Ii	ine	Renesas Semiconductor Beijing (China)	←
JEITA Packa	age Code	P-SOP32-11.4x20.75-1.27	←
Package ma specification		RILPO408DSP O -5SI UUUUUUUUUUUUUUUUUUU nnnnnnnnnnnnn XXXXXXXX	XXXXXXXX Date code R1LP0408DSP Part name -5SI Electrical characteristics
	Lead frame material	Cu	←
	Lead plating	Sn (pure tin)	←
,	Die bonding	Epoxy paste	←
i 1	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test lin	ne	Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP525PC	←
packing	Storage number	25pcs/magazine	←
	Number of magazines (Max.)	36 magazines	←
	Inner box size (LxWxH)	600mm x 172mm x 77mm	595mm x 170mm x 72mm
	Packing specification	Current specification	New specification
Tape &	Embossed tape	Emboss type name : MTE3216H-32P2M-A	←
packing	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
	,		
Moisture-pr performance	roof	MSL 3	←



(6) 32pin-SOP 4Mb(3V) Part name : RMLV0408EGSP

Item		Pre Change	Post Change
		RMLV0408EGSP-4S2#CA0 (Magazine packing)	←
Orderable part name		RMLV0408EGSP-4S2#HA0 (Tape & Reel packing)	←
Assembly I	line	Renesas Semiconductor Beijing (China)	←
JEITA Pack	rage Code	P-SOP32-11.4x20.75-1.27	←
Package marking specification		NUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUU	No change
	Lead frame material	Cu	←
Assembly	Lead plating	Sn (pure tin)	←
Material	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test I	ine	Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP525PC	←
Magazine packing	Storage number	25pcs/magazine	←
	Number of magazines (Max.)	36 magazines	←
	Inner box size (LxWxH)	600mm x 172mm x 77mm	595mm x 170mm x 72mm
	Packing specification	Current specification	New specification
Tape &	Embossed tape	Emboss type name : MTE3216H-32P2M-A	-
Reel packing	Storage number	1,000pcs/reel	
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
Moisture-p performan		MSL 3	-
Shipping la	abel	Current specification	No change in format (Changes in Renesas internal code)



(7) 48ball-FBGA 4Mb(3V) Part name: RMLV0416EGBG

Item		Pre Change	Post Change
Orderable part name		RMLV0416EGBG-4S2#AC0 (Tray packing)	←
Orderable part flame		RMLV0416EGBG-4S2#KC0 (Tape & Reel packing)	←
Assembly	line	J-Devices Kumamoto District (Japan)	←
JEITA Pac	kage Code	P-TFBGA48-7.5x8.5-0.75	←
Package n specification	on	RMLV0416EG BG-4S2 XXXXXXXX Date code	No change
	Substrate material	Glass epoxy	←
Assembly	Solder ball	Sn-Ag-Cu	←
Material	Die bonding	Epoxy paste	÷
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test I	line	Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-45)	4
Tray	Storage number	253pcs/tray	4
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	9 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
	Packing specification	Current specification	New specification
Tape & Reel packing	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	-
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-performar		MSL 3	←
Shipping I	abel	Current specification	No change in format (Changes in Renesas internal code)



(8) 48ball-FBGA 8Mb(3V) Part name: RMLV0816BGBG

Item		Pre Change	Post Change
Orderable part name		RMLV0816BGBG-4S2#AC0 (Tray packing)	←
Orderable part name		RMLV0816BGBG-4S2#KC0 (Tape & Reel packing)	←
Assembly	line	J-Devices Kumamoto District (Japan)	←
JEITA Pac	kage Code	P-TFBGA48-7.5x8.5-0.75	←
Package n specification		RMLV0816BG BG-4S2 XXXXXXXX Date code	No change
	Substrate	Glass epoxy	←
	material Solder ball	So An Co	+
Assembly		Sn-Ag-Cu	+
Material	Die bonding	Epoxy paste	
	Wire bonding Mold	Au Engage (Valence forc)	÷
Final test I		Epoxy resin (Halogen-free) Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Talwan)
rinal cesci	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name: L196-45)	←
Tray	Storage number	253pcs/tray	←
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	9 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
	Packing specification	Current specification	New specification
Tape & Reel packing	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-p performan		MSL 3	←
Shipping I	abel	Current specification	No change in format (Changes in Renesas internal code)



(9) 48ball-FBGA 16Mb(3V) Part name: R1LV1616HBG

Item		Pre Change	Post Change
Ordorable	nart name	R1LV1616HBG-4SI/-5SI#B0 (Tray packing)	←
Orderable part name		R1LV1616HBG-4SI/-5SI#S0 (Tape & Reel packing)	←
Assembly I	line	J-Devices Kumamoto District (Japan)	←
JEITA Pack	rage Code	P-TFBGA48-8x9.5-0.75	←
Package m specification		R1LV1616H BG-4SI XXXXXXXX R1LV1616H BG-5SI XXXXXXXX Date code	No change
	Substrate	Glass epoxy	←
	material Solder ball	Sn-Aq-Cu	+
Assembly Material	Die bonding	Epoxy film	÷
Plater lai	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	÷
Final test I		Renesas Semiconductor Beljing (China)	Powertech Technology Inc. (Taiwan)
	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name: PTA71C)	←
Tray	Storage number	264pcs/tray	←
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	9 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
	Packing specification	Current specification	New specification
Tape & Reel	Embossed tape	Current specification	No change
packing	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-p performan		MSL 3	←
Shipping la	abel	Current specification	No change in format (Changes in Renesas internal code)

• Regarding R1LV1616HBG, laser marking on the package's surface is processed at final test site.



(10) 48ball-FBGA 16Mb(3V) Part name: RMLV1616AGBG

Item		Pre Change	Post Change
Orderable part name		RMLV1616AGBG-5S2#AC0 (Tray packing)	←
Orderable part flame		RMLV1616AGBG-5S2#KC0 (Tape & Reel packing)	←
Assembly	line	J-Devices Kumamoto District (Japan)	←
JEITA Pac	kage Code	P-TFBGA48-7.5x8.5-0.75	←
Package r specificati	ion	RMLV1616AG BG-5S2 XXXXXXXX Date code	No change
	Substrate material	Glass epoxy	-
Assembly	Solder ball	Sn-Ag-Cu	+
Material	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Talwan)
	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-45)	←
Tray	Storage number	253pcs/tray	←
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	9 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
	Packing specification	Current specification	New specification
Tape & Reel packing	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture- performa		MSL 3	←
Shipping	label	Current specification	No change in format (Changes in Renesas internal code)



Appendix A (cont.): Change Details
(11) 48ball-FBGA 32Mb(3V) Part name : RMWV3216AGBG

Item		Pre Change	Post Change	
Orderable part name		RMWV3216AGBG-5S2#AC0 (Tray packing)	←	
		RMWV3216AGBG-5S2#KC0 (Tape & Reel packing)	←	
Assembly line		J-Devices Kumamoto District (Japan)	←	
JEITA Package Code Package marking specification		P-TFBGA48-7.5x8.5-0.75	+	
		RMWV3216AG Part name, Electrical characteristics BG-5S2 XXXXXXXXX Date code	No change	
	Substrate material	Glass epoxy	-	
Assembly	Solder ball	Sn-Ag-Cu	←	
Material	Die bonding	Epoxy film	←	
	Wire bonding	Au	+	
	Mold	Epoxy resin (Halogen-free)	←	
Final test I		Renesas Semiconductor Beljing (China)	Powertech Technology Inc. (Taiwan)	
	Packing specification	Current specification	New specification	
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-45)	←	
Tray	Storage number	253pcs/tray	←	
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←	
	Number of trays (Max.)	9 trays + 1 tray (cover)	10 trays + 1 tray (cover)	
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm	
	Packing specification	Current specification	New specification	
Tape &	Embossed tape	Current specification	No change	
packing	Storage number	1,000pcs/reel	←	
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm	
Moisture-performar		MSL 3	t =	
Shipping I	abel	Current specification	No change in format (Changes in Renesas internal code)	



(12) 48ball-FBGA 64Mb(3V) Part name: R1WV6416RBG

Item		Pre Change	Post Change		
Orderable part name		R1WV6416RBG-5SI#B0 (Tray packing)	+		
		R1WV6416RBG-5SI#S0 (Tape & Reel packing)	←		
Assembly line		J-Devices Kumamoto District (Japan)	←		
Assembly line JEITA Package Code Package marking specification		P-TFBGA48-8.5x11-0.75	←		
		R1WV6416RBG — Part name JAPAN -5SI — Electrical characteristics XXXXXXXX Date code Index mark Country of origin (Back-End Line: Assembly)	No change		
	Substrate material	Glass epoxy	+		
Assembly	Solder ball	Sn-Ag-Cu	←		
Material	Die bonding	Epoxy film	←		
	Wire bonding	Au	←		
	Mold	Epoxy resin (Halogen-included)	←		
Final test	line	Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)		
	Packing specification	Current specification	New specification		
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-121)	←		
Tray	Storage number	242pcs/tray	←		
packing	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)		
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)		
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm		
	Packing specification	Current specification	New specification		
Tape &	Embossed tape	Current specification	No change		
packing	Storage number	1,000pcs/reel	←		
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm		
Moisture- performar		MSL 3	-		
Shipping I	label	Current specification	No change in format (Changes in Renesas internal code)		



(13) 52pin-µTSOP 8Mb(3V) Part name: RMLV0816BGSD

Item		Pre Change	Post Change		
Orderable part name		RMLV0816BGSD-4S2#AC0 (Tray packing)	←		
		RMLV0816BGSD-4S2#HC0 (Tape & Reel packing)	←		
Assembly line		Renesas Semiconductor Beijing (China)	←		
Assembly line JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	-		
Package marking specification		RMLV0816BG Part name, Electrical characteristics XXXXXXXXX Date code	No change		
	Lead frame material	42Alloy	←		
Assembly	Lead plating	Sn-Cu	+		
Material	Die bonding	Epoxy film	↓		
	Wire bonding	Au	←		
	Mold	Epoxy resin (Halogen-Included)	←		
Final test		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)		
	Packing specification	Current specification	New specification		
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-24)	←		
Tray	Storage number	230pcs/tray	4		
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	4		
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)		
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm		
	Packing specification	Current specification	New specification		
Tape &	Embossed tape	Current specification	No change		
packing	Storage number	1,000pcs/reel	←		
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm		
Moisture- performar		MSL 2	←		
Shipping I	label	Current specification	No change in format (Changes in Renesas internal code)		



(14) 52pin-µTSOP 16Mb(3V) Part name : RMLV1616AGSD

Item		Pre Change	Post Change		
Orderable part name		RMLV1616AGSD-5S2#AC0 (Tray packing)	←		
		RMLV1616AGSD-5S2#HC0 (Tape & Reel packing)	←		
Assembly line		Renesas Semiconductor Beijing (China)	←		
JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	←		
Package marking specification		RMLV1616AG SD-5S2 XXXXXXXXX Index mark Dete code	No change		
	Lead frame	42Alloy	+		
	material				
Assembly	Lead plating	Sn-Cu	←		
Material	Die bonding	Epoxy film	÷		
	Wire bonding	Au	←		
	Mold	Epoxy resin (Halogen-included)	←		
Final test line		Renesas Semiconductor Beljing (China)	Powertech Technology Inc. (Taiwan)		
	Packing specification	Current specification	New specification		
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-24)	←		
Tray	Storage number	230pcs/tray	4		
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←		
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)		
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm		
	Packing specification	Current specification	New specification		
Tape &	Embossed tape	Current specification	No change		
packing	Storage number	1,000pcs/reel	4		
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm		
Moisture-p performan		MSL 2	←		
Shipping I	abel	Current specification	No change in format (Changes in Renesas internal code)		



(15) 52pin-µTSOP 32Mb(3V) Part name : R1LV3216RSD

Item		Pre Change	Post Change		
Orderable part name		R1LV3216RSD-5SI#B0 (Tray packing)	←		
		R1LV3216RSD-5SI#S0 (Tape & Reel packing)	←		
Assembly line		Renesas Semiconductor Beijing (China)	←		
JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	-		
Package marking specification		R1LV3216R SD-5SI Characteristics XXXXXXXXX Dete code	No change		
	Lead frame material	42Alloy	←		
Assembly		Sn-Cu	+		
Material	Die bonding	Epoxy film	÷		
1-later lai	Wire bonding	Au	+		
	Mold	Epoxy resin (Halogen-included)	←		
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)		
	Packing specification	Current specification	New specification		
	Tray	JEDEC Tray with Renesas Logo (Tray type name: L196-24)	←		
Tray	Storage number	230pcs/tray	←		
packing	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)		
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)		
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm		
	Packing specification	Current specification	New specification		
Tape &	Embossed tape	Current specification	No change		
packing	Storage number	1,000pcs/reel	-		
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm		
Moisture-performan		MSL 2	4		
Shipping I	abel	Current specification	No change in format (Changes in Renesas internal code)		



(16) 52pin-µTSOP 64Mb(3V) Part name: R1WV6416RSD

Item		Pre Change	Post Change	
Orderable part name		R1WV6416RSD-5SI#B0 (Tray packing)	←	
		R1WV6416RSD-5SI#S0 (Tape & Reel packing)	↓	
Assembly line		Renesas Semiconductor Beijing (China)	←	
JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	+	
Package marking specification		R1WV6416R SD-5SI Characteristics XXXXXXXXX Date code	No change	
	Lead frame	42Alloy	←	
	material			
Assembly		Sn-Cu	←	
Material	Die bonding	Epoxy film	←	
	Wire bonding	Au	÷	
Final test I	Mold	Epoxy resin (Halogen-Included) Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)	
rinai test ii	Packing specification	Current specification	New specification	
	Tray	JEDEC Tray with Renesas Logo (Tray type name: L196-24)	¢	
Tray	Storage number	230pcs/tray	←	
packing	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's comer is bottom left.)	
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)	
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm	
	Packing specification	Current specification	New specification	
Tape &	Embossed tape	Current specification	No change	
Reel packing	Storage number	1,000pcs/reel	←	
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm	
Moisture-p performan		MSL 2		
Shipping I	abel	Current specification	No change in format (Changes in Renesas internal code)	



Appendix B: Temperature Grade Unification

	Memory		Pre Change			Post Change		
Package Type	Cap., Supply Voltage	bit	Orderable Part Name	Access time	Operation Temp.	Orderable Part Name	Access time	Operation Temp.
28pin-	256Kb 5V	x8	R1LP5256ESP-5SI#B0		-40℃			
SOP			R1LP5256ESP-5SI#S0	55ns	~85℃			
			R1LP5256ESP-5SR#B0	33113	-0℃			
			R1LP5256ESP-5SR#S0		~70℃	R1LP5256ESP-5SI#B0	55ns	-40℃
			R1LP5256ESP-7SI#B0		-40℃	R1LP5256ESP-5SI#S0		~85℃
			R1LP5256ESP-7SI#S0	70ns	~85℃			
			R1LP5256ESP-7SR#B0	70113	0℃			
			R1LP5256ESP-7SR#S0		~70℃			
	256Kb 3V	x8	R1LV5256ESP-5SI#B0		-40℃			
			R1LV5256ESP-5SI#S0	55ns	~85℃			
			R1LV5256ESP-5SR#B0	00113	-0℃			
			R1LV5256ESP-5SR#S0		~70℃	R1LV5256ESP-5SI#B0	55ns	-40℃
			R1LV5256ESP-7SI#B0		-40℃	R1LV5256ESP-5SI#S0	00.1.5	~85℃
			R1LV5256ESP-7SI#S0	70ns	~85℃			
			R1LV5256ESP-7SR#B0	, 0,13	0℃			
			R1LV5256ESP-7SR#S0		~70℃			
32pin-	1Mb 5V	x8	R1LP0108ESN-5SI#B0		-40℃			
SOP			R1LP0108ESN-5SI#S0	55ns	~85℃		55ns	-40℃
			R1LP0108ESN-5SR#B0		-0℃			
			R1LP0108ESN-5SR#S0		~70℃	R1LP0108ESN-5SI#B0 R1LP0108ESN-5SI#S0		
			R1LP0108ESN-7SI#B0		-40℃			~85℃
			R1LP0108ESN-7SI#S0	70ns	~85℃			
			R1LP0108ESN-7SR#B0		0℃			
			R1LP0108ESN-7SR#S0		~70℃		-	
	1Mb 3V	x8	R1LV0108ESN-5SI#B0		-40℃			
			R1LV0108ESN-5SI#S0	55ns	~85℃			
			R1LV0108ESN-5SR#B0		-0℃ ~70℃			
			R1LV0108ESN-5SR#S0			R1LV0108ESN-5SI#B0	55ns	-40℃
			R1LV0108ESN-7SI#B0		-40℃	R1LV0108ESN-5SI#S0		~85℃
			R1LV0108ESN-7SI#S0	70ns	~85℃			
			R1LV0108ESN-7SR#B0		0℃ ~70℃			
	43.41 53.4	_	R1LV0108ESN-7SR#S0			<u> </u>	-	
	4Mb 5V	x8	R1LP0408DSP-5SI#B0		-40℃ ~85℃			
			R1LP0408DSP-5SI#S0	55ns		1		
			R1LP0408DSP-5SR#B0		-0℃ ~70℃			
			R1LP0408DSP-5SR#S0			R1LP0408DSP-5SI#B0	55ns	-40℃
			R1LP0408DSP-7SI#B0		-40℃ ~85℃	R1LP0408DSP-5SI#S0		~85℃
			R1LP0408DSP-7SI#S0	70ns		1		
			R1LP0408DSP-7SR#B0		0℃ ~70℃			
			R1LP0408DSP-7SR#S0		.~/UC	l		

^{• #}B0: Magazine packing, #S0: Tape & Reel packing



(1)-a. Electrical characteristics (DC): 256Kb(5V) R1LP5256ESP

Products

Item	Pre Change	Post Change	
Orderable part name	R1LP5256ESP-5SI, -5SR, -7SI, -7SR#B0	R1LP5256ESP-5SI#B0	
Orderable part name	R1LP5256ESP-5SI, -5SR, -7SI, -7SR#S0	R1LP5256ESP-5SI#S0	

DC conditions

Item	Symbol	F	re Change	Symbol	Post Change			
Supply voltage	Vcc	4.5V~5.5V		4.5V~5.5V		4.5V~5.5V Vcc		←
Operation townswature range	Ta	5SR, 7SR	0°C to 70°C	Ta	-40°C to 85°C			
Operating temperature range		5SI, 7SI	-40°C to 85°C	la la	-40°C to 85°C			
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)		VIH	←			
Input low voltage	VIL	-0.3V(min.) / 0.8V(max.)		VIL	←			

DC characteristics

DC CHaracteristics						
Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc1(TTL, Min.Cycle)	35mA(n	nax.) / 25mA(typ.)	Icc1(TTL, Min.Cycle)		←
Operating Current	Icc2(MOS, Cycle=1us)	4mA(n	nax.) / 2mA(typ.)	Icc2(MOS, Cycle=1us)		←
	ISB(TTL)		3mA(max.)	ISB(TTL)		←
		~25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	~25℃	←
Standby current	ISB1(MOS)	~40°C	3uA(max.)		~40℃	←
Surroy Current		~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	←
Outrook blok outbook	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	←
Output high voltage	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change	
Input capacitance	C in	6pF(max.)	C in	←	
Input/Output capacitance	C I/O	8pF(max.)	C I/O	←	

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
		~25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	~25℃	←
		~40°C	3uA(max.)		~40°C	←
Data retention current	IccDR(Vcc=3.0V)	~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	←
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	



(1)-b. Electrical characteristics (AC): 256Kb(5V) R1LP5256ESP

Products

Item	Pre Change	Post Change
Orderable part name	R1LP5256ESP-5SI, -5SR, -7SI, -7SR#B0	R1LP5256ESP-5SI#B0
	R1LP5256ESP-5SI, -5SR, -7SI, -7SR#S0	R1LP5256ESP-5SI#S0

AC characteristics

D	03	vel.	\sim	100	-
P.	CO	u	<u></u>		c

Item	Symbol		Pre Change	Symbol	Post Change	
Dond and time	*50	5SI, 5SR	55ns(min.)	+D.C	EFordada N	
Read cycle time	tRC	7SI, 7SR	70ns(min.)	tRC	55ns(min.)	
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)	
Address access time	DV	7SI, 7SR	70ns(max.)	DVA	sons(max.)	
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)	
chip select access time	DACS	7SI, 7SR	70ns(max.)	DACS	SSIIS(IIIAX.)	
5. do. d	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)	
Output enable to output valid		7SI, 7SR	35ns(max.)		Sons(max.)	
Output hold from address	tOH	5SI, 5SR	10ns(min.)	tOH	-	
change		7SI, 7SR	10ns(min.)			
Chip select to output in low-Z	tCLZ	5SI, 5SR	5ns(min.)	tCLZ	<u></u>	
crip seect to output in low-2	ICLZ	7SI, 7SR	5ns(min.)	ICLZ	_	
Output enable to output in	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←	
low-Z	TOLZ	7SI, 7SR	5ns(min.)	TOLZ	-	
Chip deselect to output in	tCHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tCHZ	One(min) / 20ne/may)	
high-Z	tt.HZ	7SI, 7SR	Ons(min.) / 25ns(max.)	6CHZ	Ons(min.) / 20ns(max.)	
Output disable to output in	IOH7	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	One(min) / 20ne/may)	
high-Z	tOHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	BONZ	Ons(min.) / 20ns(max.)	

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change	
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)	
write cycle time	twc	7SI, 7SR	70ns(min.)	twc	SSIIS(IIIII.)	
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	Effection)	
Address valid to end of write	DAVA	7SI, 7SR	65ns(min.)	DAW	50ns(min.)	
Chin calculations disformity	tCW	5SI, 5SR	50ns(min.)	LCIII.	FO-data \	
Chip select to end of write	tcw	7SI, 7SR	65ns(min.)	tCW	50ns(min.)	
111.7	tWP	5SI, 5SR	40ns(min.)	tWP	40-4-4-3	
Write pulse width	twp	7SI, 7SR	50ns(min.)	twP	40ns(min.)	
Address set of News	tAS	5SI, 5SR	Ons(min.)		-	
Address setup time	DAS	7SI, 7SR	Ons(min.)	tAS	_	
Melto many time	tWR	5SI, 5SR	Ons(min.)	tWR	←	
Write recovery time		7SI, 7SR	Ons(min.)		-	
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	3Englaria)	
Data to write time overlap	LDW	7SI, 7SR	30ns(min.)	tDW	25ns(min.)	
Data hold from write time	tDH	5SI, 5SR	Ons(min.)	tDH	←	
Data noid from write time	ton.	7SI, 7SR	Ons(min.)	ton.	_	
Output enable from end of	tOW	5SI, 5SR	5ns(min.)	tOW	←	
write	LOW	7SI, 7SR	5ns(min.)		_	
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	One(min) / 20ne/may)	
high-Z	tonz.	7SI, 7SR	Ons(min.) / 25ns(max.)	tonz	Ons(min.) / 20ns(max.)	
Write to output in high-Z	tWHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	NWH7	One(min) / 20ne/may)	
write to output in high-Z	WHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	tWHZ	0ns(min.) / 20ns(max.)	



(2)-a. Electrical characteristics (DC): 256Kb(3V) R1LV5256ESP

Products

Floudus									
Item Pre Change		Post Change							
Orderable part name	R1LV5256ESP-5SI, -5SR, -7SI, -7SR#B0	R1LV5256ESP-5SI#B0							
	R1LV5256ESP-5SI, -5SR, -7SI, -7SR#S0	R1LV5256ESP-5SI#S0							

DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	2.7V~3.6V		Vcc	←
Operating temperature range	Та	5SR, 7SR	0°C to 70°C	Tá	-40°C to 85°C
		5SI, 7SI	-40°C to 85°C		
Input high voltage	VIH	2.0V(min.) / Vcc+0.3V(max.)		VIH	-
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)		VIL	←

DC characteristics

a direction of the control of the co						
Item	Symbol	Pre Change		Symbol	Post Change	
	Icc1(TTL, Min.Cycle)	25mA(n	nax.) / 14mA(typ.)	Icc1(TTL, Min.Cycle)	←	
Operating Current	Icc2(MOS, Cycle=1us)	5mA(n	nax.) / 2mA(typ.)	Icc2(MOS, Cycle=1us)		←
	ISB(TTL)	0.	33mA(max.)	ISB(TTL)		←
	ISB1(MOS)	~25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	~25℃	←
Standby current		~40℃	3uA(max.)		~40℃	←
surreit		~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	←
	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
Output high voltage	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=1mA	0.4V(max.)	VOL	IOL=1mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	6pF(max.)	C in	←
Input/Output capacitance	C I/O	8pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
		~25℃	2uA(max.) / 0.6uA(typ.)		~25℃	←
		~40°C	3uA(max.)	IccDR(Vcc=3.0V)	~40°C	←
Data retention current	IccDR(Vcc=3.0V)	~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	←
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	



Appendix C (cont.): Electrical Characteristics (2)-b. Electrical characteristics (AC): 256Kb(3V) R1LV5256ESP

Products

Item	Pre Change	Post Change
Orderable part name	R1LV5256ESP-5SI, -5SR, -7SI, -7SR#B0	R1LV5256ESP-5SI#B0
	R1LV5256ESP-5SI, -5SR, -7SI, -7SR#S0	R1LV5256ESP-5SI#S0

AC characteristics

Item	Symbol		Pre Change	Symbol	Post Change
Sand auda tima	+0.0	5SI, 5SR	55ns(min.)	*50	FF-sf-sin \
Read cycle time	tRC	7SI, 7SR	70ns(min.)	tRC	55ns(min.)
Address access time	tAA	5SI, 5SR	55ns(max.)	AAt	55ns(max.)
Address access time	DV	7SI, 7SR	70ns(max.)	DVA	SSHS(max.)
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)
chip select access time	U/C3	7SI, 7SR	70ns(max.)	UNCO	SSHS(Hax.)
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)
	to L	7SI, 7SR	35ns(max.)		
Output hold from address	tOH	5SI, 5SR	10ns(min.)	tOH	←
change		7SI, 7SR	10ns(min.)		
Chip select to output in low-Z	tCLZ	5SI, 5SR	5ns(min.)	tCLZ	-
one seem to suput in lon 2		7SI, 7SR	5ns(min.)		
Output enable to output in	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←
low-Z	TOLE.	7SI, 7SR	5ns(min.)	TOLZ	
Chip deselect to output in	tCHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tCHZ	Ons(min.) / 20ns(max.)
high-Z	UCHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	UCIZ	ons(min.)/ zons(max.)
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	Ons(min.) / 20ns(max.)
high-Z		7SI, 7SR	Ons(min.) / 25ns(max.)	UNZ	ons(mm.)/ zons(max.)

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change	
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)	
write cycle time	twc	7SI, 7SR	70ns(min.)	twc	SSIIS(IIIII.)	
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)	
Address valid to end or write	DAW	7SI, 7SR	65ns(min.)	DAW	Sons(min.)	
China adapt to and affects	LCIU.	5SI, 5SR	50ns(min.)	15111	FO-vi-i-)	
Chip select to end of write	tCW	7SI, 7SR	65ns(min.)	tCW	50ns(min.)	
Mile the modern and this		5SI, 5SR	40ns(min.)		40-4-4-3	
Write pulse width	tWP	7SI, 7SR	50ns(min.)	tWP	40ns(min.)	
Add and a star time		5SI, 5SR	Ons(min.)	tAS	-	
Address setup time	tAS	7SI, 7SR	Ons(min.)		_	
	tWR	5SI, 5SR	Ons(min.)	tWR		
Write recovery time		7SI, 7SR	Ons(min.)		←	
Data to unito timo quarlan	tDW	5SI, 5SR	25ns(min.)	tDW	DEnc/min)	
Data to write time overlap	LDW	7SI, 7SR	30ns(min.)	LDW	25ns(min.)	
Data hold from write time	tDH	5SI, 5SR	Ons(min.)	tDH	←	
Data noid from write time	ton	7SI, 7SR	Ons(min.)	ton.	_	
Output enable from end of	tow	5SI, 5SR	5ns(min.)	tOW	←	
write	LOW	7SI, 7SR	5ns(min.)	LOW	_	
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	One(min) / 20ne(may)	
high-Z	tOHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	tonz.	Ons(min.) / 20ns(max.)	
Write to output in high 7	tWHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tWHZ	One(min) / 20ne(may)	
Write to output in high-Z	WHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	WHZ	0ns(min.) / 20ns(max.)	



(3)-a. Electrical characteristics (DC): 1Mb(5V) R1LP0108ESN

Products

Item	Pre Change	Post Change
Orderable part name	R1LP0108ESN-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESN-5SI#B0
	R1LP0108ESN-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESN-5SI#S0

DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	4.5V~5.5V		Vcc	←
Operating temperature range	-	5SR, 7SR	0°C to 70°C		4005 1- 0505
	Ta	5SI, 7SI	-40°C to 85°C	-40°C to 85°C	
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)		VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.8V(max.)		VIL	←

DC characteristics

DC Characteristics						
Item	Symbol	F	Pre Change		Post Change	
Oti Ot	Icc1(TTL, Min.Cycle)	35mA(n	nax.) / 25mA(typ.)	Icc1(TTL, Min.Cycle)		←
Operating Current	Icc2(MOS, Cycle=1us)	5mA(n	nax.) / 2mA(typ.)	Icc2(MOS, Cycle=1us)		←
Standby current	ISB(TTL)		3mA(max.)	ISB(TTL)		←
		~25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	~25℃	←
	ISB1(MOS)	~40°C	3uA(max.)		~40°C	←
Suraby Current		~70°C	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	←
	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	←
Output high voltage	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current		~25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	~25℃	←
	IccDR(Vcc=3.0V)	~40°C	3uA(max.)		~40°C	←
		~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	←
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	



(3)-b. Electrical characteristics (AC): 1Mb(5V) R1LP0108ESN

Products

Item	Pre Change	Post Change
Orderable part name	R1LP0108ESN-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESN-5SI#B0
	R1LP0108ESN-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESN-5SI#S0

AC characteristics

Item	Symbol		Pre Change	Symbol	Post Change	
Dood out a Nove	*85	5SI, 5SR	55ns(min.)	+0.0	EFooderin A	
Read cycle time	tRC	7SI, 7SR	70ns(min.)	tRC	55ns(min.)	
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)	
Address access time	DV	7SI, 7SR	70ns(max.)	DAA	sons(max.)	
Chip select access time	tACS1 / tACS2	5SI, 5SR	55ns(max.)	tACS1 / tACS2	55ns(max.)	
chip select access time	DICST / DICS2	7SI, 7SR	70ns(max.)	DICSI / DICS2	oons(max.)	
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)	
Output enable to output valid	102	7SI, 7SR	35ns(max.)	IOE	Julis(Illax.)	
Output hold from address	tOH	5SI, 5SR	5ns(min.)	tOH	5ns(min.)	
change	ton	7SI, 7SR	10ns(min.)	ton	Sits(iiiii.)	
Chip select to output in low-Z	tCLZ1 / tCLZ2	5SI, 5SR	5ns(min.)	tCLZ1 / tCLZ2	5ns(min.)	
crip select to dampat in low-2	101217 10122	7SI, 7SR	10ns(min.)	tolzi / tolzz	aris(min.)	
Output enable to output in	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←	
low-Z	1012	7SI, 7SR	5ns(min.)	1012	-	
Chip deselect to output in	tCHZ1 / tCHZ2	5SI, 5SR	Ons(min.) / 20ns(max.)	tCHZ1 / tCHZ2	Ons(min.) / 20ns(max.)	
high-Z	tichzi / tichzz	7SI, 7SR	Ons(min.) / 25ns(max.)	conzi / conzi	ons(mm.) / zons(max.)	
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	Ons(min.) / 20ns(max.)	
high-Z	tonz	7SI, 7SR	Ons(min.) / 25ns(max.)	SON2	oris(min.)/ Zoris(max.)	

Write Cycle

Item	Symbol Pre Change		Symbol	Post Change		
Weite and time		5SI, 5SR	55ns(min.)	tWC		
Write cycle time	tWC	7SI, 7SR	70ns(min.)	twc	55ns(min.)	
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	FOnedonia 3	
Address valid to end or write	DAW	7SI, 7SR	55ns(min.)	DAW	50ns(min.)	
Chic and set to and affective	15111	5SI, 5SR	50ns(min.)	LCIU.	50 metanta h	
Chip select to end of write	tCW	7SI, 7SR	55ns(min.)	tCW	50ns(min.)	
Market and a suidable		5SI, 5SR	45ns(min.)		45-d-i- \	
Write pulse width	tWP	7SI, 7SR	50ns(min.)	tWP	45ns(min.)	
Address sets of Mary	tAS	5SI, 5SR	Ons(min.)		←	
Address setup time	UAS	7SI, 7SR	Ons(min.)	tAS	-	
	tWR	5SI, 5SR	Ons(min.)	tWR	←	
Write recovery time		7SI, 7SR	Ons(min.)		←	
Data to veito time eventos	tDW	5SI, 5SR	25ns(min.)	·DW	35neferio 3	
Data to write time overlap	tow	7SI, 7SR	30ns(min.)	tDW	25ns(min.)	
Data hold from write time	tDH	5SI, 5SR	Ons(min.)	tDH	←	
Data noid from write time	ton	7SI, 7SR	Ons(min.)	ton.	-	
Output enable from end of	tOW	5SI, 5SR	5ns(min.)	tOW	←	
write	tow	7SI, 7SR	5ns(min.)	tow	←	
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	IOU7	One(min) / 20ne(may)	
high-Z	tonz	7SI, 7SR	Ons(min.) / 25ns(max.)	tOHZ	Ons(min.) / 20ns(max.)	
Melto to output in high 7	10017	5SI, 5SR	Ons(min.) / 20ns(max.)	tWHZ	One(min) / 20ne(max)	
Write to output in high-Z	tWHZ	7SI, 7SR	Ons(min.) / 25ns(max.)		Ons(min.) / 20ns(max.)	



(4)-a. Electrical characteristics (DC): 1Mb(3V) R1LV0108ESN

Products

	TTOWAGES		
	Item	Pre Change	Post Change
	Orderable part name	R1LV0108ESN-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESN-5SI#B0
		R1LV0108ESN-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESN-5SI#S0

DC conditions

DC CONDICIONS						
Item	Symbol	Pre Change		Symbol	Post Change	
Supply voltage	Vcc	2.7V~3.6V		Voc	←	
Operating temperature range	-	5SR, 7SR	0°C to 70°C		400C to 050C	
	Ta	5SI, 7SI	-40°C to 85°C	Та	-40°C to 85°C	
Input high voltage	VIH	2.0V(min.) / Vcc+0.3V(max.)		VIH	←	
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)		VIL	←	

DC characteristics

DC CHaracteristics						
Item	Symbol	F	Pre Change		Post Change	
	Icc1(TTL, Min.Cycle)	25mA(n	25mA(max.) / 15mA(typ.)			←
Operating Current	Icc2(MOS, Cycle=1us)	5mA(n	nax.) / 2mA(typ.)	Icc2(MOS, Cycle=1us)		←
	ISB(TTL)	0.	33mA(max.)	ISB(TTL)		←
Standby current		~25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	~25℃	←
	ISB1(MOS)	~40°C	3uA(max.)		~40℃	←
Surrey Corre		~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	←
Output high voltage	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	Cin	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	~25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	~25℃	←
		~40°C	3uA(max.)		~40°C	←
		~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	+
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	



(4)-b. Electrical characteristics (AC): 1Mb(3V) R1LV0108ESN

Products

Item	Pre Change	Post Change
Orderable part page	R1LV0108ESN-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESN-5SI#B0
Orderable part name	R1LV0108ESN-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESN-5SI#S0

AC characteristics

Item	Symbol		Pre Change	Symbol	Post Change	
Read cycle time	100	5SI, 5SR	55ns(min.)	+0.0		
	tRC	7SI, 7SR	70ns(min.)	tRC	55ns(min.)	
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)	
Address access time	box	7SI, 7SR	70ns(max.)	DV	SSIIS(Max.)	
Chip select access time	tACS1 / tACS2	5SI, 5SR	55ns(max.)	tACS1 / tACS2	55ns(max.)	
Criip select access time	OICSI / OICS2	7SI, 7SR	70ns(max.)	OICSI / OICS2		
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)	
	to E	7SI, 7SR	35ns(max.)	IOE		
Output hold from address	tOH	5SI, 5SR	5ns(min.)	tOH	5ns(min.)	
change		7SI, 7SR	10ns(min.)	tori	Jis(iiii.)	
Chip select to output in low-Z	tCLZ1 / tCLZ2	5SI, 5SR	5ns(min.)	tCLZ1 / tCLZ2	5ns(min.)	
crip seect to dapat in low-2		7SI, 7SR	10ns(min.)	totzi / totzz		
Output enable to output in	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	+	
low-Z	tol	7SI, 7SR	5ns(min.)	1012		
Chip deselect to output in	tCHZ1 / tCHZ2	5SI, 5SR	Ons(min.) / 20ns(max.)	tCHZ1 / tCHZ2	Ons(min.) / 20ns(max.)	
high-Z	tichzi / tichzz	7SI, 7SR	Ons(min.) / 25ns(max.)	tonzi / tonzz	ons(min.) / zons(max.)	
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	Ons(min.) / 20ns(max.)	
high-Z	UNZ	7SL 7SR	Ons(min.) / 25ns(max.)	Onz		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change	
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)	
Write cycle diffe		7SI, 7SR	70ns(min.)	twc	SSIIS(IIIII.)	
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	Effection)	
Address valid to end of write	DAW	7SI, 7SR	55ns(min.)	DAW	50ns(min.)	
Ship adapt to and after the	LCIII.	5SI, 5SR	50ns(min.)	LCIII.	FO-data)	
Chip select to end of write	tCW	7SI, 7SR	55ns(min.)	tCW	50ns(min.)	
Marke and as well the		5SI, 5SR	45ns(min.)		4Fd-d- 3	
Write pulse width	tWP	7SI, 7SR	50ns(min.)	tWP	45ns(min.)	
Address selve bless		5SI, 5SR	Ons(min.)	tAS	_	
Address setup time	tAS	7SI, 7SR	Ons(min.)		←	
	tWR	5SI, 5SR	Ons(min.)	tWR	_	
Write recovery time		7SI, 7SR	Ons(min.)		←	
Data to units time questo	.5	5SI, 5SR	25ns(min.)	tDW	2Factoria)	
Data to write time overlap	tDW	7SI, 7SR	30ns(min.)	tow	25ns(min.)	
Data hold from write time	tDH	5SI, 5SR	Ons(min.)	tDH		
Data noid from write time	tDH	7SI, 7SR	Ons(min.)	ton.	-	
Output enable from end of	tow	5SI, 5SR	5ns(min.)	tow	_	
write	tow	7SI, 7SR	5ns(min.)	tow	←	
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	1017	Oneferin \ / 20neferay \	
high-Z	tOHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	tOHZ	Ons(min.) / 20ns(max.)	
Mello to output in high 7		5SI, 5SR	Ons(min.) / 20ns(max.)		2006min 3 / 2006mm 3	
Write to output in high-Z	tWHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	tWHZ	Ons(min.) / 20ns(max.)	



(5)-a. Electrical characteristics (DC): 4Mb(5V) x8 R1LP0408DSP

Products

110000		
Item	Pre Change	Post Change
Orderable part page	R1LP0408DSP-5SI, -5SR, -7SI, -7SR#B0	R1LP0408DSP-5SI#B0
Orderable part name	R1LP0408DSP-5SI, -5SR, -7SI, -7SR#S0	R1LP0408DSP-5SI#S0

DC conditions

DC CONTRICTORS							
Item	Symbol	Pre Change		Pre Change		Symbol	Post Change
Supply voltage	Vcc	4.5V~5.5V		Vcc	←		
Operating temperature range	-	5SR, 7SR	0°C to 70°C	Та	-40°C to 85°C		
	Та	5SI, 7SI	-40°C to 85°C				
Input high voltage	VIH	2.2V(min.) / Voc+0.3V(max.)		VIH	+		
Input low voltage	VIL	-0.3V(min.) / 0.8V(max.)		VIL	+		

DC characteristics

Item	Symbol	Pre Change		Symbol	Po	st Change
	Icc(TTL)	10mA	(max.) / 5mA(typ.)	Icc(TTL)	←	
Operating Current	Icc1(TTL, Min.Cycle)	25mA(max.) / 15mA(typ.)	Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	5mA(max.) / 3mA(typ.)		Icc2(MOS, Cycle=ius)		←
Standby current	ISB(TTL)	0.5mA(max.) / 0.1mA(typ.)		ISB(TTL)	←	
		~25℃	2.5uA(max.) / 0.8uA(typ.)	ISB1(MOS)	~25℃	←
		~40°C	3uA(max.) / 1uA(typ.)		~40℃	←
	ISB1(MOS)	~70°C	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	+
Output high voltage	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	←
Output high voltage	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	←
Output low voltage	VOL	IOL=2.1mA	0.4V(max.)	VOL	IOL=2.1mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	~25℃	2.5uA(max.) / 0.8uA(typ.)	IccDR(Vcc=3.0V)	~25℃	←
		~40℃	3uA(max.) / 1uA(typ.)		~40℃	←
		~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	←
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	



(5)-b. Electrical characteristics (AC): 4Mb(5V) x8 R1LP0408DSP

D-v		

Item	Pre Change	Post Change
Orderable part same	R1LP0408DSP-5SI, -5SR, -7SI, -7SR#B0	R1LP0408DSP-5SI#B0
Orderable part name	R1LP0408DSP-5SI, -5SR, -7SI, -7SR#S0	R1LP0408DSP-5SI#S0

AC characteristics

Re	au	Cy	/u	е

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SI, 5SR	25ns(max.)	tOE	25ns(max.)
		7SI, 7SR	35ns(max.)		
Chip select to output in low-Z	tCLZ	5SI, 5SR	10ns(min.)	tCLZ	+
		7SI, 7SR	10ns(min.)		
Output enable to output in low-Z	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	+
		7SI, 7SR	5ns(min.)	tol2	
Chip deselect to output in high-Z	tCHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tCHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	Ons(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	Ons(min.) / 25ns(max.)		
Output hold from address change	tOH	5SI, 5SR	10ns(min.)	tOH	←
		7SI, 7SR	10ns(min.)		

Write Cycle

Item	Symbol		Pre Change	Symbol	Post Change
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Chip select to end of write	tcw	5SI, 5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	60ns(min.)		
Address setup time	tAS	5SI, 5SR	Ons(min.)	tAS	←
		7SI, 7SR	Ons(min.)		
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	60ns(min.)		
Write pulse width	tWP	5SI, 5SR	40ns(min.)	tWP	40ns(min.)
		7SI, 7SR	50ns(min.)		
Write recovery time	tWR	5SI, 5SR	Ons(min.)	tWR	←
		7SI, 7SR	Ons(min.)		
Write to output in high-Z	tWHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tWHZ	Ons(min.) / 20ns(max.)
		7SI, 7SR	Ons(min.) / 25ns(max.)		
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	30ns(min.)		
Data hold from write time	tDH	5SI, 5SR	Ons(min.)	tDH	←
		7SI, 7SR	Ons(min.)		
Output enable from end of write	tOW	5SI, 5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	Ons(min.) / 20ns(max.)
		7SI, 7SR	Ons(min.) / 25ns(max.)		



Appendix D: Packaging Specification Change

- Regarding R1LV3216RSD-5SI, R1WV6416RSD-5SI and R1WV6416RBG-5SI, laying direction of ICs on a tray is to be changed (see below).
- No change in other products, because the direction is already same as the "Post Change" as shown below.

	Pre Change	Post Change		
Laying direction of ICs on a tray	Direction 1	Direction		
Orderable part name	R1LV3216RSD-5SI#B0 R1WV6416RSD-5SI#B0 R1WV6416RBG-5SI#B0	R1LV3216RSD-5SI#B0 R1WV6416RSD-5SI#B0 R1WV6416RBG-5SI#B0		