CHANGE NOTIFICATION

LINEAR TECHNOLOGY | NOW PART OF **ANALOG DEVICES**

Analog Devices, Inc.
1630 McCarthy Blvd., Milpitas CA
(408) 432-1900

May 31, 2017

Dear Sir/Madam: PCN# 053117

Subject: Notification of Change to LTC4040 Datasheet

Please be advised that Analog Devices, Inc. Milpitas, California has made a minor change to the LTC4040 product datasheet to facilitate improvement in our manufacturing capability. The changes are shown on the attached page of the marked up datasheet. There was no change in form, fit, function, quality or reliability of the product. The product shipped after July 31, 2017 will be tested to the new limits.

Should you have any concerns, please contact me before July 31, 2017, at which time we will consider this change to be approved. Should you have any questions or concerns please contact your local Analog Devices sales person or you may contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@ANALOG.COM.

Sincerely,

Jason Hu
Quality Assurance Engineer

LTC4040

ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3) $V_{IN} = 5V$, $V_{BAT} = 3.6V$, $R_{PROG} = 2k$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NTC							
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising Voltage Threshold / Hysteresis		75.0	76.5 / 1.5	78	%V_{IN} / %V_{IN}
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling Voltage Threshold / Hysteresis		33.4	34.9 / 1.73	36.4	%V_{IN} / %V_{IN}
V_{DIS}	NTC Disable Threshold Voltage	Falling Threshold / Hysteresis		0.7	1.7 / 50	2.7	%V_{IN} / mV
I_{NTC}	NTC Leakage Current			−20		20	nA
Backup Mode Boost Switching Regulator							
V_{BSTFB}	BSTFB Reference Voltage		●	0.78	0.8	0.82	V
I_{BSTFB}	BSTFB Input Bias Current			−20		20	nA
V_{SYS}	Step-up (Boost) Converter Output Voltage Range			3.5		5	V
f_{OSCBST}	Step-Up Converter Switching Frequency	Backup Mode ($V_{PFI} < 1.17V$)		0.98	1.125	1.33	MHz
I_{LIMBST}	NMOS Switch Current Limit			5.5	6.5	7.5	A
R_{PBST}	Boost High Side Switch On-Resistance				75		mΩ
R_{NBST}	Boost Low Side Switch On-Resistance				70		mΩ
V_{OVSD}	V_{SYS} Overvoltage Shutdown Threshold	V_{SYS} Rising		5.3	5.5	5.7	V
	Overvoltage Shutdown Hysteresis				100		mV
V_{UVLO}	BAT Pin Undervoltage Lockout	V_{BAT} Falling			2.45	2.6	V
	BAT Pin Undervoltage Lockout Hysteresis				150		mV
D_{MAX}	Maximum Boost Duty Cycle				88 93 ~~91~~		%
	NMOS Switch Leakage	BSTOFF = 1, CHGOFF = 1			1		µA
	PMOS Switch Leakage	BSTOFF = 1, CHGOFF = 1			1		µA
Reset Comparator							
	RSTFB Threshold (Falling)		●	0.72	0.74	0.76	V
	RSTFB Hysteresis				20		mV
	RSTFB Pin Leakage Current	$V_{RSTFB} = 0.9V$		−50		50	nA
	$\overline{RST}$ Delay (RSTFB Rising)				232		ms
Power-Fail Comparator							
	PFI Input Threshold (Falling Edge)	Initiates Backup Mode	●	1.17	1.19	1.21	V
	PFI Input Hysteresis				30		mV
	PFI Pin Leakage Current	$V_{PFI} = 1.3V$		−100		100	nA
	PFI Delay to $\overline{PFO}$	PFI Falling			0.5		µs
	$\overline{PFO}$ Pin Leakage Current	$V_{\overline{PFO}} = 5V$			10		µA
	$\overline{PFO}$ Pin Output Low Voltage	$I_{\overline{PFO}} = 5mA$			65		mV
Logic Input (CHGOFF, BSTOFF, F0, F1, F2)							
V_{IL}	Logic Low Input Voltage		●			0.4	V
V_{IH}	Logic High Input Voltage		●	1.2			V
I_{IL}	Logic Low Input Leakage			−1		1	µA
I_{IH}	Logic High Input Leakage			−1		1	µA

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