

# **DPDT SWITCH GaAs MMIC**

## **■FEATURES**

- Low control voltage
- Low current consumption 0.1µA typ.
- Low insertion loss

0.1µA typ. 0.45dB tyr

1.8V min.

- s 0.45dB typ. @f=920MHz
- High isolation

30dB typ. @f=920MHz

- P<sub>-0.1dB</sub> +30dBm typ. @f=920MHz
- Small package 1.6 x 1.6mm, t=0.397mm
- RoHS compliant and Halogen Free, MSL1

# ■GENERAL DESCRIPTION

The NJG1813KG1 is a 2bit control DPDT switch IC suited for LPWA applications.

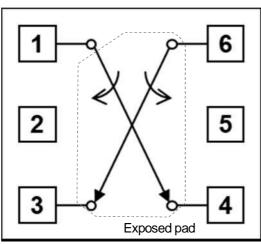
The NJG1813KG1 is compatible with 1.8 V low control voltage and features low current consumption important for LPWA applications.

The small and thin ESON6-G1 package is adopted.

# ■APPLICATION

- LPWA (SIGFOX, LoRaWAN, Wi-SUN) applications
- •Antenna switching, path switching, general purpose switching applications

# **BLOCK DIAGRAM** (ESON6-G1)



# **■FUNCTIONAL DESCRIPTION**

"H"=V<sub>CTL(H)</sub>, "L"=V<sub>CTL(L)</sub>

通過経路	VCTL1	VCTL2
ANT1-OUT2 ANT2-OUT1	Н	L
ANT1-OUT1 ANT2-OUT2	L	н

# ■PIN CONFIGURATION

PIN NO.	SYMBOL	DESCRIPTION	
1	ANT2	RF terminal	
2	VCTL2	Control signal input terminal	
3	OUT2	RF terminal	
4	OUT1	RF terminal	
5	VCTL1	Control signal input terminal	
6	ANT1	RF terminal	
Exposed pad	GND	Ground terminal	

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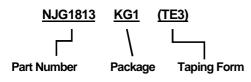
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(Top view)



## PRODUCT NAME INFORMATION



#### ORDERING INFORMATION

	PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN- FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs.)
_	NJG1813KG1	ESON6-G1	Yes	Yes	Sn-Bi	1813	3.5	3,000

## ■ ABSOLUTE MAXIMUM RATINGS

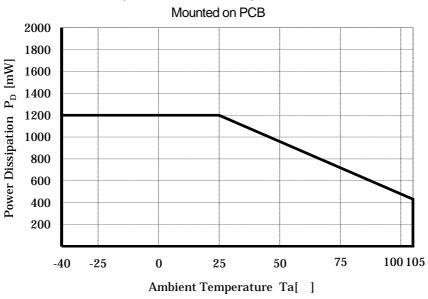
		T <sub>a</sub> =2	5°C, Z <sub>s</sub> =Z <sub>I</sub> =50Ω
PARAMETER	SYMBOL	RATINGS	UNIT
Control Voltage	V <sub>CTL</sub>	4.5	V
RF Input Power	P <sub>IN</sub>	+33	dBm
Power Dissipation <sup>(1)</sup>	P <sub>D</sub>	1200	mW
Operating Temperature	T <sub>opr</sub>	-40 to +105	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

(1): Mounted on four-layer FR4 PCB with through-hole (101.5  $\times$  114.5 mm), T<sub>i</sub> = 150°C

#### ■ POWER DISSIPATION VS.AMBIENT TEMPERATURE

Please, refer to the following Power Dissipation and Ambient Temperature.

(Please note the surface mount package has a small maximum rating of Power Dissipation  $[P_D]$ , a special attention should be paid in designing of thermal radiation.)



#### **Power Dissipation - Ambient Temperature Characteristic**

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# ■ ELECTRICAL CHARACTERISTICS (DC CHARACTERISTICS)

		$V_{CTL(H)}=3.0V, V_{CTL(L)}=0V, I_{a}=25^{\circ}C$	5, Z <sub>s</sub> =Z <sub>I</sub> =5	$50\Omega$ , with	applicati	on circuit
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Control Voltage (HIGH)	V <sub>CTL(H)</sub>		1.8	3.0	4.0	V
Control Voltage (LOW)	V <sub>CTL(L)</sub>		-0.2	-	0.2	V
Control Current	I <sub>CTL</sub>	RF OFF, $V_{CTL(H)}$ =3.0V, $V_{CTL(L)}$ =0V	-	0.1	2.5	μA

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# ■ ELECTRICAL CHARACTERISTICS (RF CHARACTERISTICS)

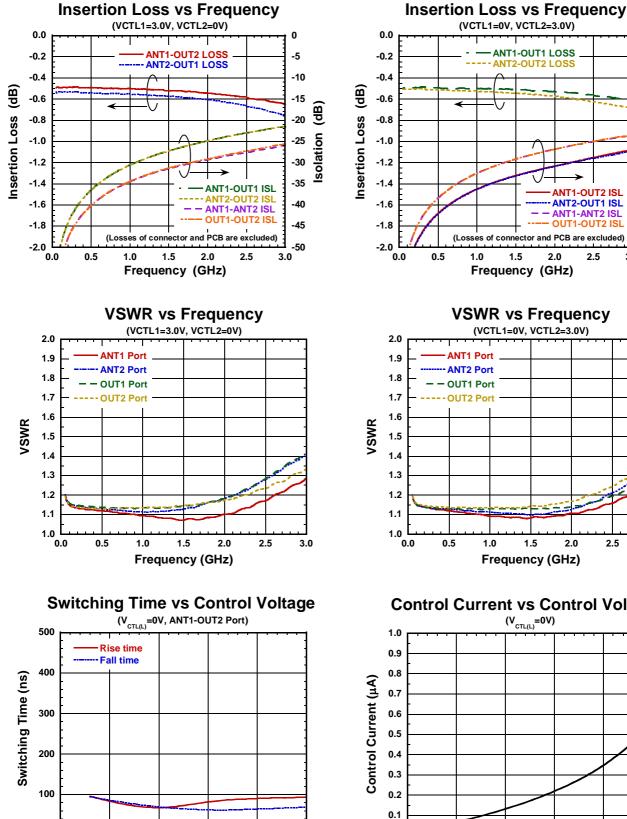
	$V_{CTL(H)}=3.0V, V_{CTL(L)}=0V, T_a=25^{\circ}C, Z_s=Z_l=50\Omega$ , with application circu					
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Insertion loss	LOSS	f=920MHz	-	0.45	0.68	dB
Isolation1	ISL1	f=920MHz, ANT1/2 to OUT1/2	26	30	-	dB
Isolation2	ISL2	f=920MHz, ANT1 to ANT2, OUT1 to OUT2	26	30	-	dB
Input power at 0.1dB compression point	P <sub>-0.1dB</sub>	f=920MHz	+27	+30	-	dBm
VSWR	VSWR	f=920MHz	-	1.1	1.5	-
Switching time	T <sub>SW</sub>	50% VCTL to 10%/90% RF	-	100	300	ns

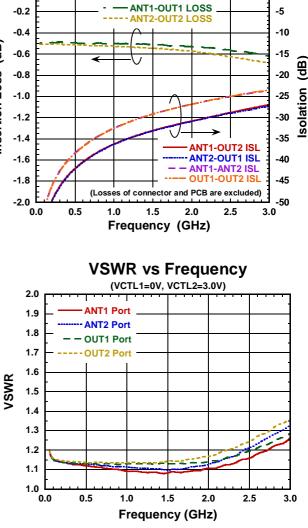
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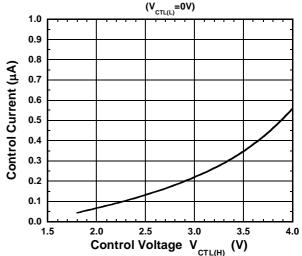
#### ELECTRICAL CHARACTERISTICS





(VCTL1=0V, VCTL2=3.0V)

**Control Current vs Control Voltage** 



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4.0

0

1.5

2.0

2.5

Control Voltage V

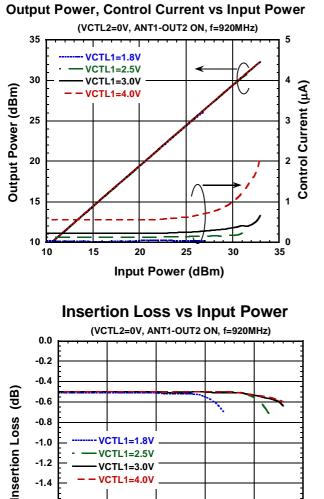
3.0

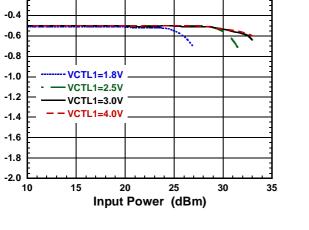
3.5

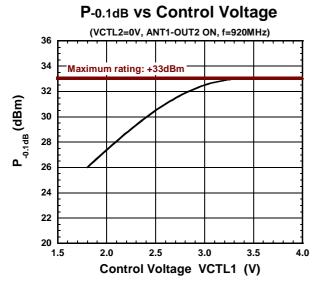
(V)

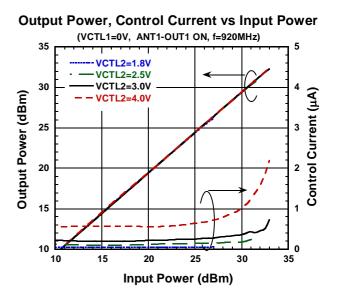


## ELECTRICAL CHARACTERISTICS

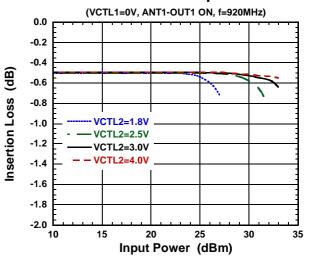


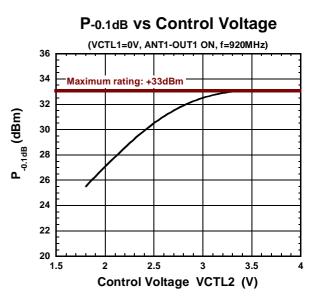






**Insertion Loss vs Input Power** 



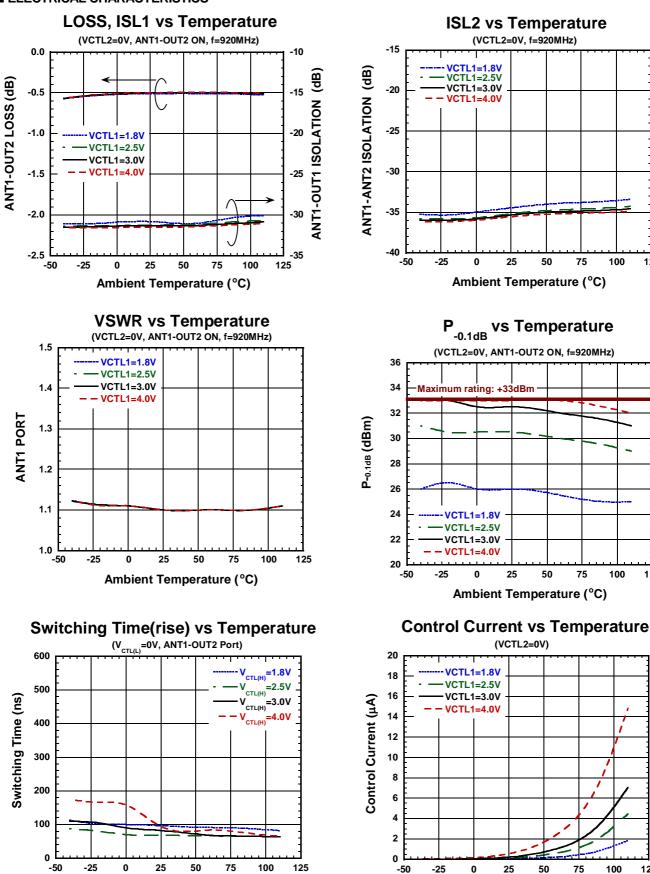


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125

125





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Ambient Temperature (°C)

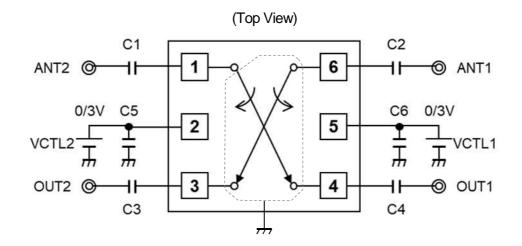
125

Ambient Temperature (°C)

http://www.njr.com/



# ■ APPLICATION CIRCUIT

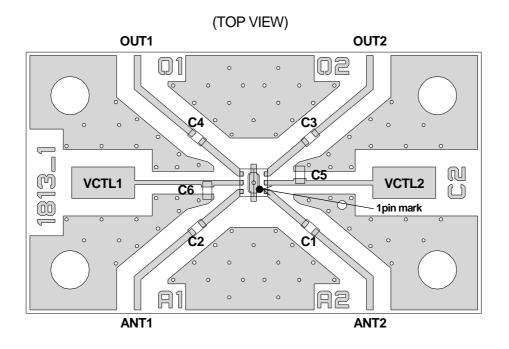


## ■ PARTS LIST

Part ID	Value	Notes
C1 to C4	1000pF	MURATA (GRM15)
C5 to C6	10pF	MURATA (GRM15)

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# EVALUATION BOARD



#### Losses of PCB and connectors, Ta=+25°C

Frequency (MHz)	Loss (dB)
420	0.21
920	0.29
2000	0.48
2400	0.53
2700	0.56

PCB: FR-4 t=0.2mm MICROSTRIP LINE WIDTH: 0.4mm (Zo=50Ω) PCB SIZE: 26.0 x 15.0mm

## ■ PRECAUTIONS

- [1] The DC blocking capacitors (C1, C2, C3, C4) should be placed at RF terminals. Please choose appropriate capacitance value at the application frequency.
- [2] For avoiding the degradation of RF performance, the bypass capacitors (C5, C6) should be placed as close as possible to VCTL terminals.
- [3] For good RF performance, exposed pad should be connected to PCB ground plane of substrate, and through –holes should be placed near the IC.

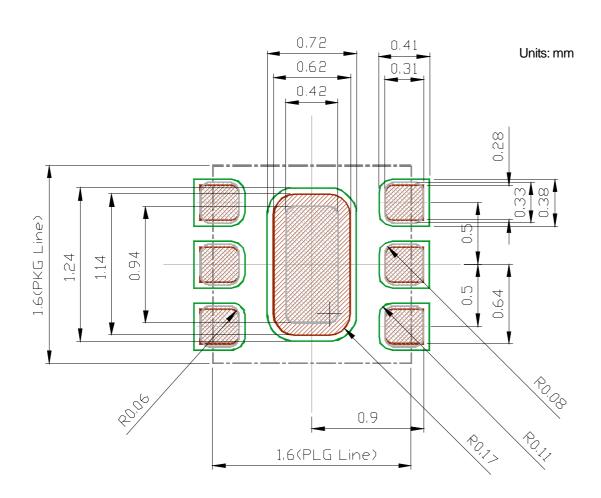
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## ■ RECOMMENDED FOOTPRINT PATTERN (ESON6-G1)



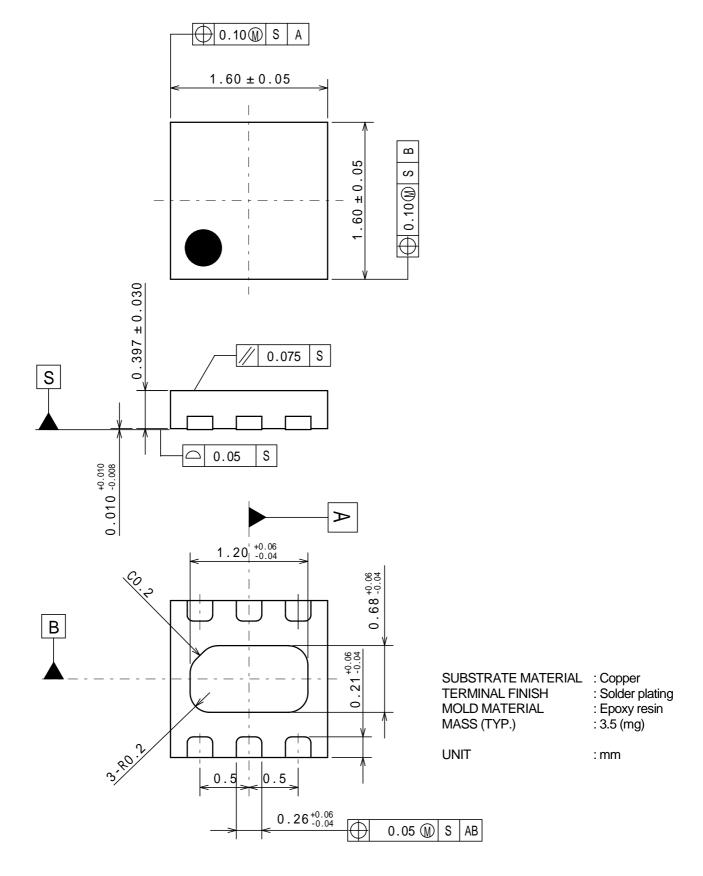
: Land : Mask (Open area) \*Metal mask thickness : 100µm : Resist (Open area)



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# ■ PACKAGE OUTLINE



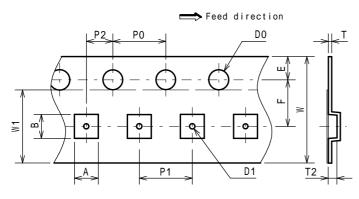
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UNIT: mm

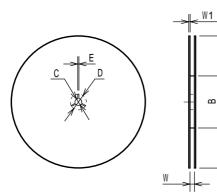
## PACKING SPECIFICATION

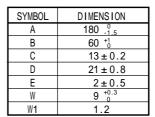
#### TAPING DIMENSION



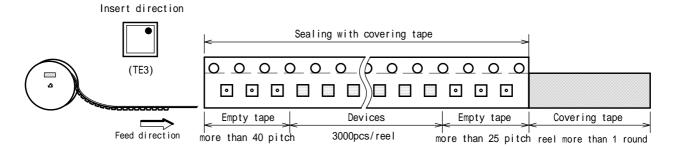
SYMBOL DIMENSION REMARKS А  $1.85 \pm 0.05$ BOTTOM DIMENSION В  $1.85 \pm 0.05$ BOTTOM DIMENSION  $1.5 \frac{+0.1}{0}$  $0.5 \pm 0.1$ DO D1 Е  $1.75 \pm 0.1$ F  $3.5 \pm 0.05$ P0  $4.0 \pm 0.1$ P1  $4.0 \pm 0.1$ P2  $2.0 \pm 0.05$ Т  $0.25 \pm 0.05$ T2  $0.65 \pm 0.05$ W 8.0±0.2 W1 THICKNESS 0.1max 5.5

**REEL DIMENSION** 



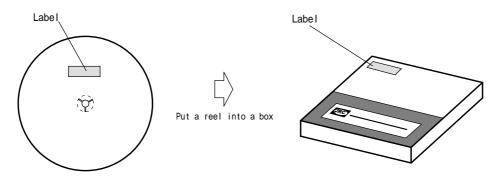


TAPING STATE



4

PACKING STATE



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