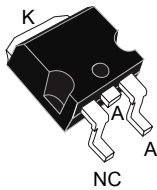


1200 V, 20 A, silicon carbide power Schottky diode


 D²PAK HV

Product label



Product status link

[STPSC20H12G2-TR](#)

Product summary

$I_{F(AV)}$	20 A
V_{RRM}	1200 V
T_j (max.)	175 °C
V_F (typ.)	1.35 V

Features

- No or negligible reverse recovery
- Switching behavior independent of temperature
- Robust high voltage periphery
- Operating T_j from -40 °C to 175 °C
- Low V_F
- D²PAK HV creepage distance (anode to cathode) = 5.38 mm min.
- ECOPACK2 compliant

Applications

- EV Charging station
- DC/DC
- PFC

Description

This 20 A, 1200 V SiC diode is an ultra-high performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 1200 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature.

Housed in D²PAK HV, this diode is perfectly suited for a usage in PFC applications, in charging station, DC/DC, easing the compliance to IEC-60664-1.

The [STPSC20H12G2-TR](#) will boost performances in hard switching conditions. Its high forward surge capability ensures good robustness during transient phases.

1 Characteristics

Table 1. Absolute ratings (limiting values at 25 °C, unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage ($T_j = -40\text{ °C}$ to $+175\text{ °C}$)		1200	V
$I_{F(RMS)}$	Forward rms current		38	A
$I_{F(AV)}$	Average forward current	$T_c = 155\text{ °C}$, DC current	20	A
I_{FRM}	Repetitive peak forward current	$T_c = 155\text{ °C}$, $T_j = 175\text{ °C}$, $\delta = 0.1$	78	A
I_{FSM}	Surge non repetitive forward current	$t_p = 10\text{ ms}$ sinusoidal, $T_c = 25\text{ °C}$	140	A
		$t_p = 10\text{ ms}$ sinusoidal, $T_c = 150\text{ °C}$	120	
T_{stg}	Storage temperature range		-65 to +175	°C
T_j	Operating junction temperature ⁽¹⁾		-40 to +175	°C

1. $(dP_{tot}/dT_j) < (1/R_{th(j-a)})$ condition to avoid thermal runaway for a diode on its own heatsink.

Table 2. Thermal resistance parameters

Symbol	Parameter	Value		Unit
		Typ.	Max.	
$R_{th(j-c)}$	Junction to case	0.30	0.45	°C/W

Table 3. Static electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_R ⁽¹⁾	Reverse leakage current	$T_j = 25\text{ °C}$	$V_R = V_{RRM}$	-	10	120	μA
		$T_j = 150\text{ °C}$		-	60	800	
V_F ⁽²⁾	Forward voltage drop	$T_j = 25\text{ °C}$	$I_F = 20\text{ A}$	-	1.35	1.50	V
		$T_j = 150\text{ °C}$		-	1.75	2.25	

1. Pulse test: $t_p = 5\text{ ms}$, $\delta < 2\%$

2. Pulse test: $t_p = 500\text{ }\mu\text{s}$, $\delta < 2\%$

To evaluate the conduction losses, use the following equation:

- $P = 1.07 \times I_{F(AV)} + 0.059 \times I_{F(RMS)}^2$

For more information, please refer to the following application notes related to the power losses:

- AN604: Calculation of conduction losses in a power rectifier
- AN4021: Calculation of reverse losses on a power diode

Table 4. Dynamic electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$Q_{Cj}^{(1)}$	Total capacitive charge	$V_R = 800 \text{ V}$	-	129	-	nC
C_j	Total capacitance	$V_R = 0 \text{ V}, T_c = 25 \text{ }^\circ\text{C}, F = 1 \text{ MHz}$	-	1650	-	pF
		$V_R = 800 \text{ V}, T_c = 25 \text{ }^\circ\text{C}, F = 1 \text{ MHz}$	-	110	-	

1. Most accurate value for the capacitive charge: $Q_{Cj}(V_R) = \int_0^{V_R} C_j(V) dV$

1.1 Characteristics (curves)

Figure 1. Forward voltage drop versus forward current (typical values)

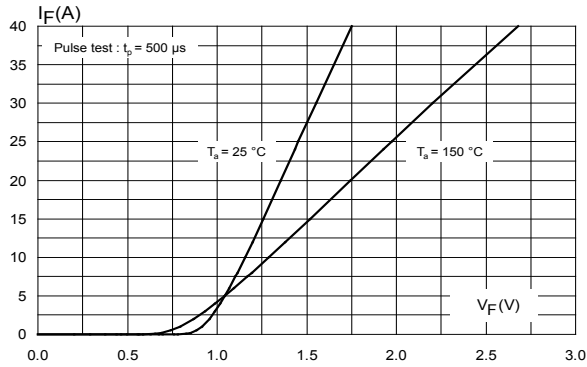


Figure 2. Reverse leakage current versus reverse voltage applied (typical values)

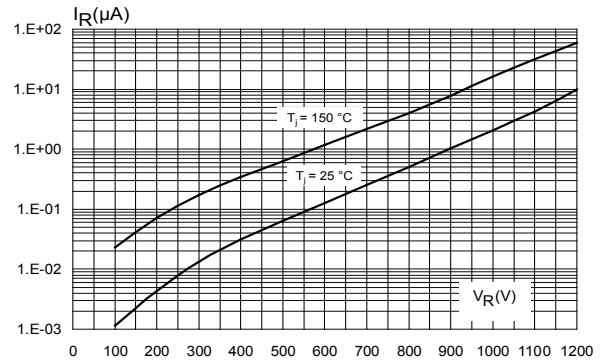


Figure 3. Peak forward current versus case temperature

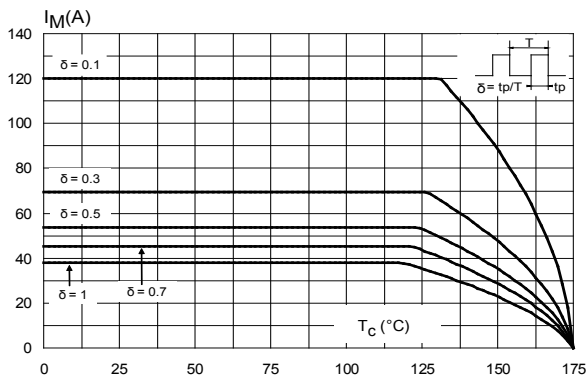


Figure 4. Junction capacitance versus reverse voltage applied (typical values)

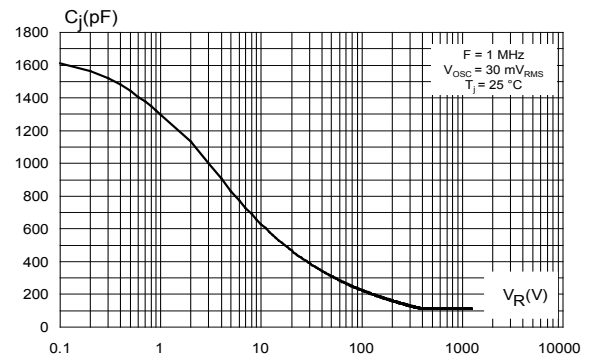


Figure 5. Relative variation of thermal impedance junction to case versus pulse duration

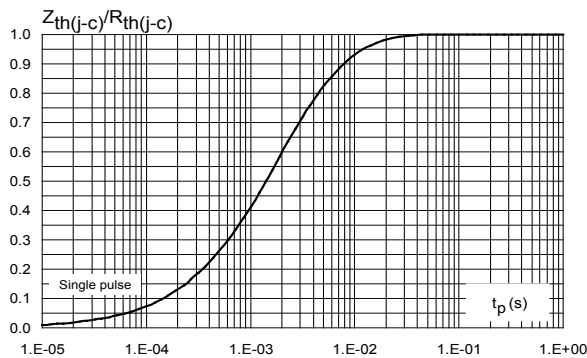


Figure 6. Non-repetitive peak surge forward current versus pulse duration (sinusoidal waveform)

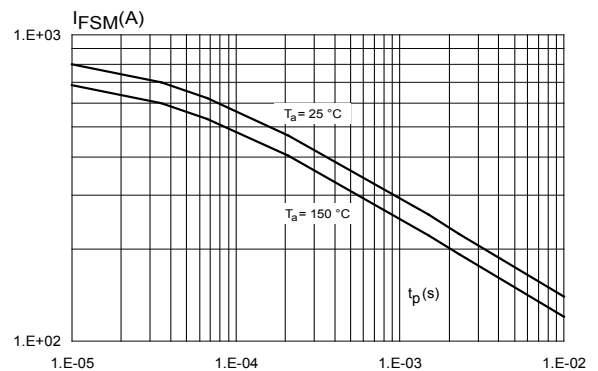


Figure 7. Total capacitive charges versus reverse voltage applied (typical values)

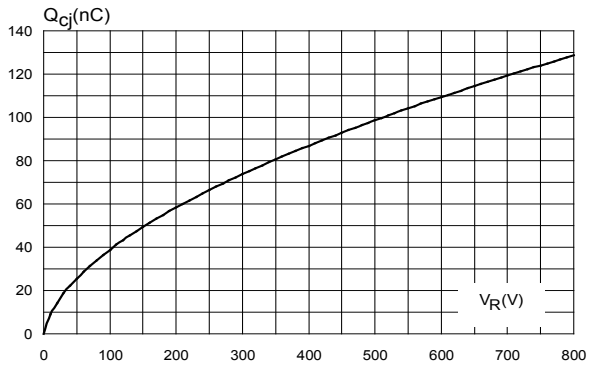
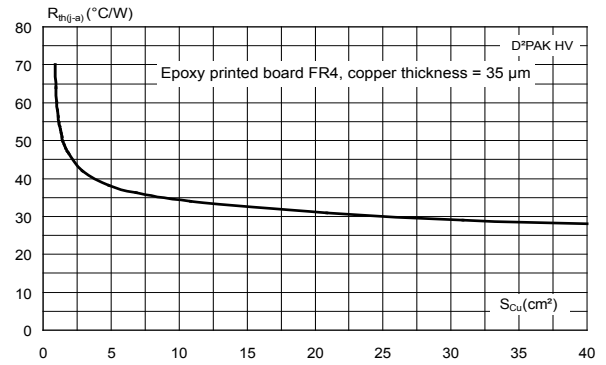


Figure 8. Thermal resistance junction to ambient versus copper surface under tab for D²PAK package (typical values)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 D²PAK high voltage package information

- Epoxy meets UL94, V0

Figure 9. D²PAK high voltage package outline

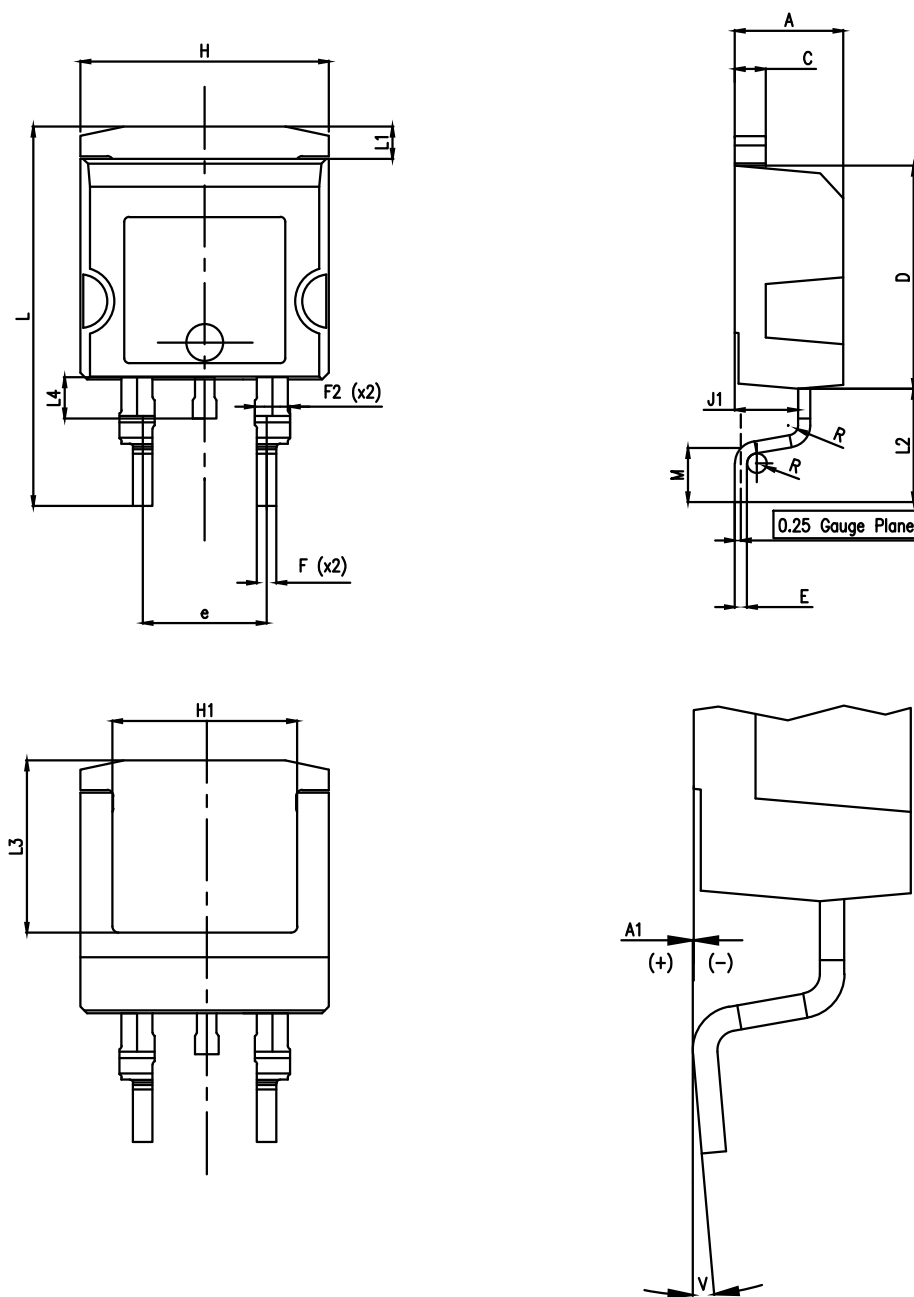
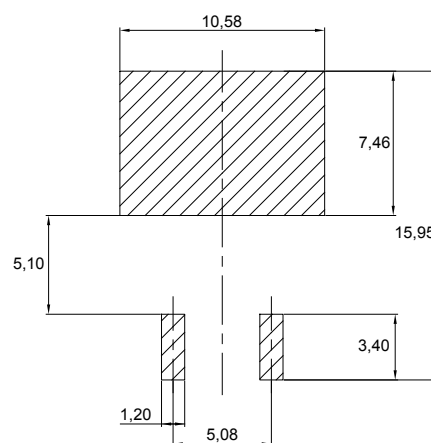


Table 5. D²PAK high voltage package mechanical data

Ref.	Dimensions																																																	
	Min.	Typ.	Max.																																															
A	4.30	-	4.70																																															
A1	0.03	-	0.20																																															
C	1.17	-	1.37																																															
D	8.95	-	9.35																																															
e	4.98	-	5.18																																															
E	0.50	-	0.90																																															
F	0.78	- </tr <tr> <td>F2</td> <td>1.14</td> <td>-</td> <td>1.70</td> </tr> <tr> <td>H</td> <td>10.00</td> <td>-</td> <td>10.40</td> </tr> <tr> <td>H1</td> <td>7.40</td> <td>-</td> <td>7.80</td> </tr> <tr> <td>J1</td> <td>2.49</td> <td>-</td> <td>2.69</td> </tr> <tr> <td>L</td> <td>15.30</td> <td>-</td> <td>15.80</td> </tr> <tr> <td>L1</td> <td>1.27</td> <td>-</td> <td>1.40</td> </tr> <tr> <td>L2</td> <td>4.93</td> <td>-</td> <td>5.23</td> </tr> <tr> <td>L3</td> <td>6.85</td> <td>-</td> <td>7.25</td> </tr> <tr> <td>L4</td> <td>1.5</td> <td>-</td> <td>1.7</td> </tr> <tr> <td>M</td> <td>2.6</td> <td>-</td> <td>2.9</td> </tr> <tr> <td>R</td> <td>0.20</td> <td>-</td> <td>0.60</td> </tr> <tr> <td>V</td> <td>0°</td> <td>-</td> <td>8°</td> </tr>	F2	1.14	-	1.70	H	10.00	-	10.40	H1	7.40	-	7.80	J1	2.49	-	2.69	L	15.30	-	15.80	L1	1.27	-	1.40	L2	4.93	-	5.23	L3	6.85	-	7.25	L4	1.5	-	1.7	M	2.6	-	2.9	R	0.20	-	0.60	V	0°	-	8°
F2	1.14	-	1.70																																															
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R	0.20	-	0.60																																															
V	0°	-	8°																																															

Figure 10. D²PAK high voltage footprint in mm



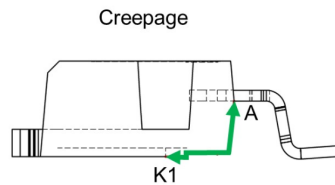
2.1.1 Creepage distance between Anode and Cathode

Table 6. Creepage distance between anode and cathode

Symbol	Parameter		Value	Unit
Cd _{A-K1}	Minimum creepage distance between A and K1 (with top coating)	D ² PAK HV	5.38	mm
Cd _{A-K2}	Minimum creepage distance between A and K2 (without top coating)		3.48	

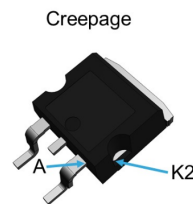
Note: D²PAK HV creepage distance (anode to cathode) = 5.38 mm min. (refer to IEC 60664-1)

Figure 11. Creepage with top coating



Minimum distance between A & K1 = 5.38 mm (with top coating)

Figure 12. Creepage without top coating



Minimum distance between A & K2 = 3.48 mm (without top coating)

3 Ordering information

Table 7. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
STPSC20H12G2-TR	SC20H12G2	D ² PAK HV	1.48 g	1000	Tape and reel

Revision history

Table 8. Document revision history

Date	Revision	Changes
31-Aug-2020	1	First issue.

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