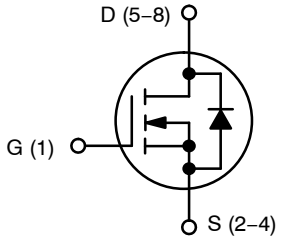
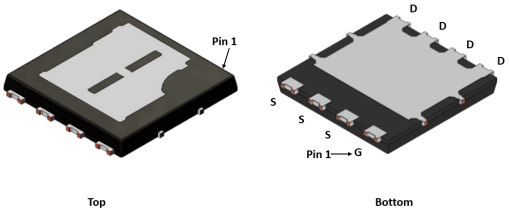
MOSFET - Power, Single N-Channel, TDFNW8
100 V, 4.2 mΩ, 178 A
NTMTSC4D2N10G

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
100 V	4.2 mΩ @ 10 V	178 A



N–CHANNEL MOSFET



TDFNW8
DUAL COOL
CASE 507AS

Features

- Wide SOA for Linear Mode Operation
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- High Peak UIS Current Capability for Ruggedness
- Small Footprint (8x8 mm) & Top Metal Cooling
- These Devices are Pb–Free, Halogen–Free / BFR–Free and are RoHS Compliant

Typical Applications

- 48 V Hot Swap System, Load Switch, Soft–Start, E–Fuse

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	100	V
Gate–to–Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	178	A
		T_C = 100°C		125	
Power Dissipation $R_{\theta JC}$ (Note 2)		T_C = 25°C	P_D	267	W
		T_C = 100°C		133	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	21	A
		T_A = 100°C		15	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.9	W
		T_A = 100°C		1.9	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	2558	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	222	A
Single Pulse Drain–to–Source Avalanche Energy ($I_{L(pk)}$ = 100 A, L = 0.1 mH)			E_{AS}	506	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

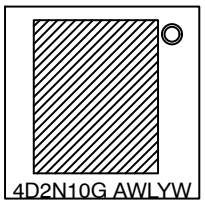
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction–to–Case – Steady State (Note 2)	$R_{\theta JC}$	0.56	°C/W
Junction–to–Top Source – Steady State (Note 2)	$R_{\theta JC}$	0.86	
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	38	

1. Surface–mounted on FR4 board using a 1 in^2, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

MARKING DIAGRAM



4D2N10G = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

© Semiconductor Components Industries, LLC, 2020

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		100			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			84.1		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	T_J = 25°C			1.0	μA
			T_J = 150°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 450 μA		2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 450 μA, ref to 25°C			−9.24		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 88 A		2.9	4.2	mΩ
Forward Transconductance	g_{FS}	V_{DS} =5 V, I_D = 88 A			61		S
Gate Resistance	R_G	T_A = 25°C			0.9		Ω
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 50 V			10450		pF
Output Capacitance	C_{OSS}				1050		
Reverse Transfer Capacitance	C_{RSS}				158		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 50 V; I_D = 88 A			159		nC
Threshold Gate Charge	$Q_{G(TH)}$				27.7		
Gate−to−Source Charge	Q_{GS}				61		
Gate−to−Drain Charge	Q_{GD}				38		
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 88 A, R_G = 4.7 Ω			40		ns
Rise Time	t_r				36		
Turn−Off Delay Time	$t_{d(OFF)}$				76		
Fall Time	t_f				26		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 88 A	T_J = 25°C		0.82	1.2	V
			T_J = 125°C		0.70		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 300 A/μs, I_S = 44 A			46.7		ns
Reverse Recovery Charge	Q_{RR}				224		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 1000 A/μs, I_S = 44 A			46.1		ns
Reverse Recovery Charge	Q_{RR}				595		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

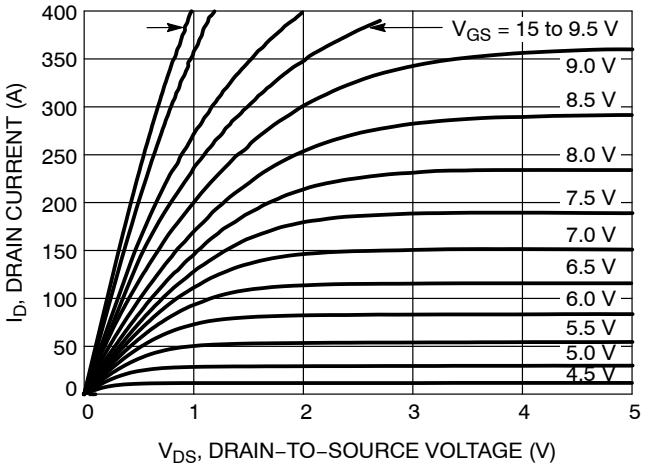


Figure 1. On−Region Characteristics

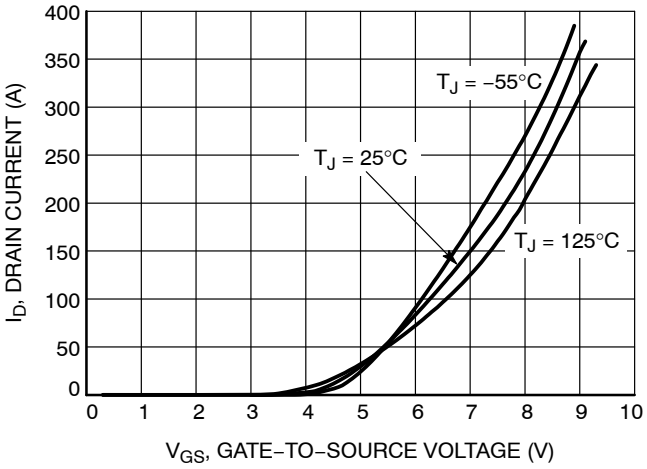


Figure 2. Transfer Characteristics

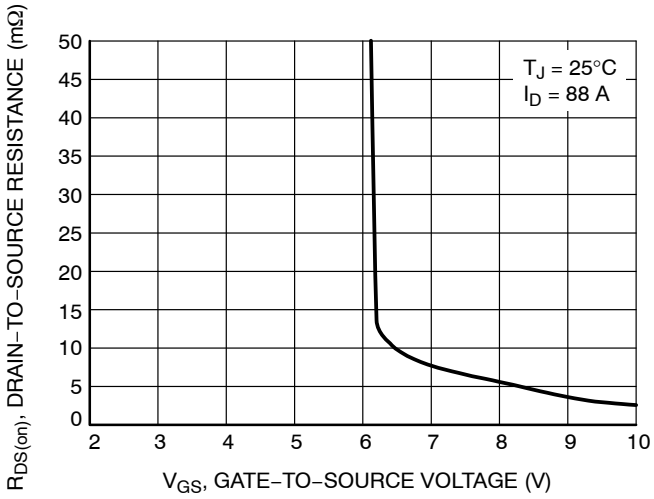


Figure 3. On−Resistance vs. Gate−to−Source Voltage

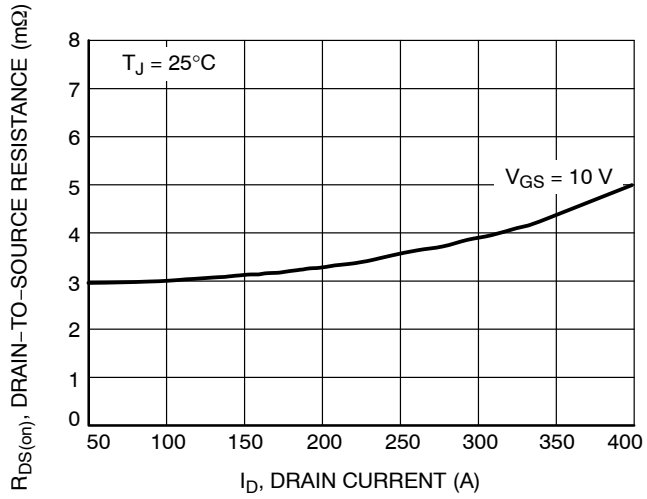


Figure 4. On−Resistance vs. Drain Current

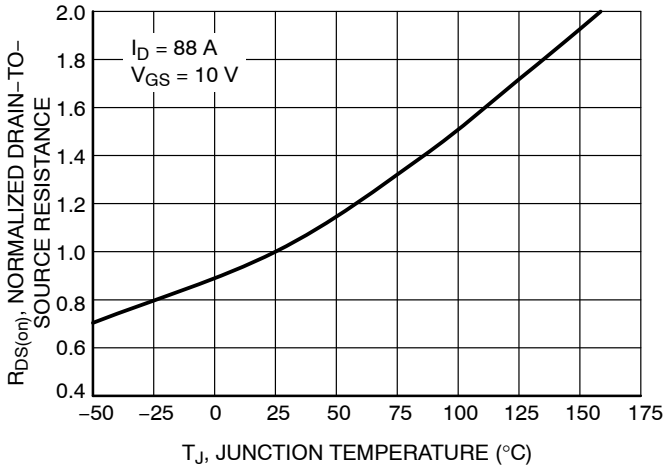


Figure 5. On−Resistance Variation with Temperature

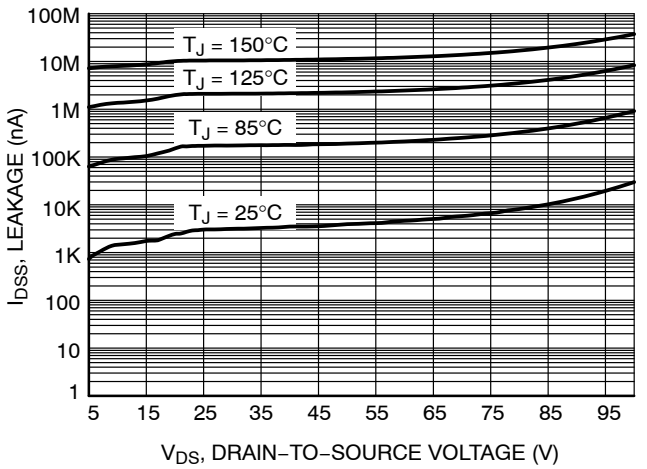


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

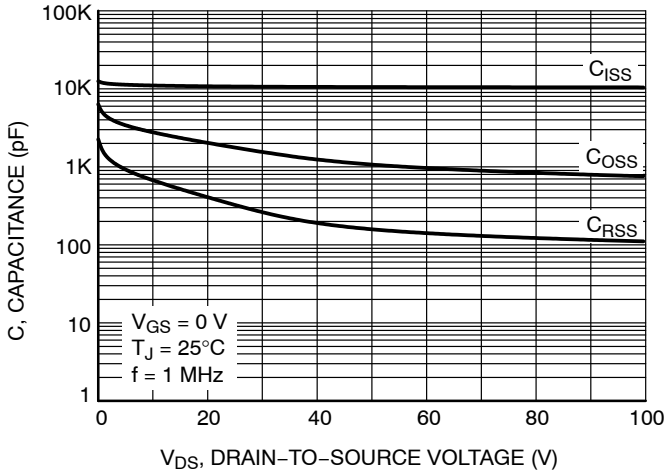


Figure 7. Capacitance Variation

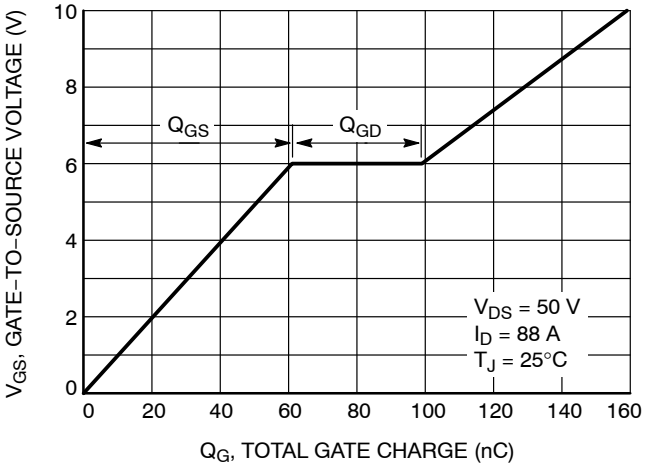


Figure 8. Gate−to−Source Voltage vs. Total Charge

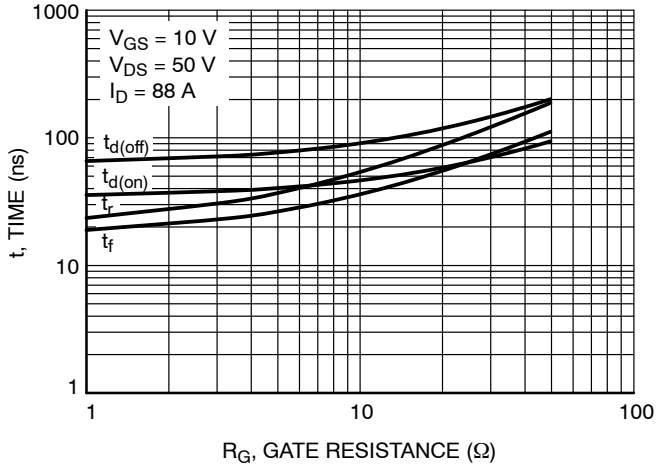


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

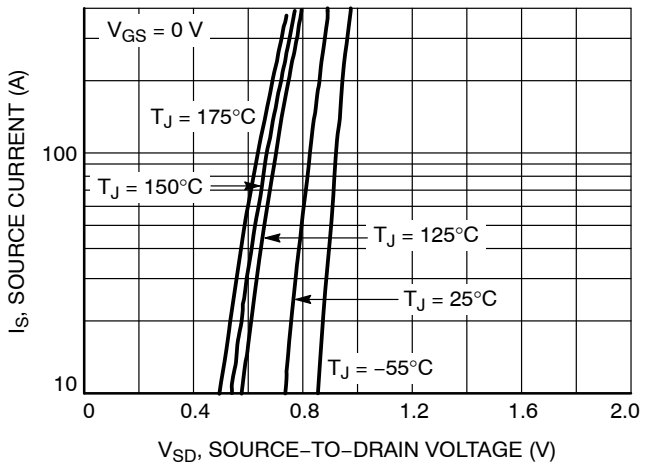


Figure 10. Diode Forward Voltage vs. Current

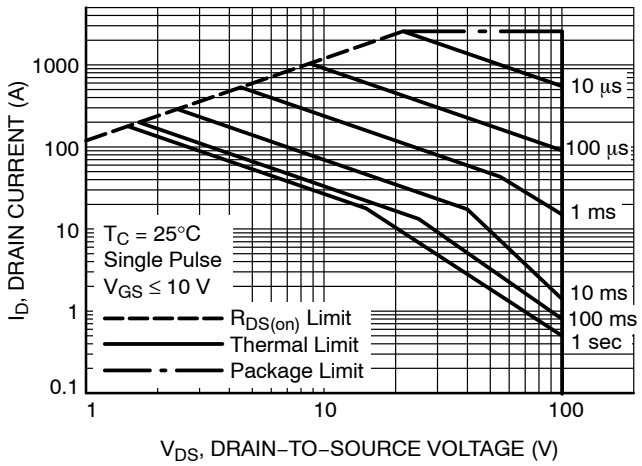


Figure 11. Maximum Rated Forward Biased Safe Operating Area

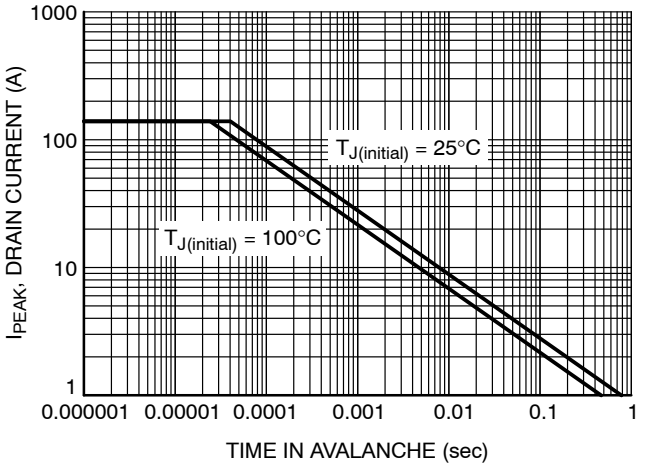


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

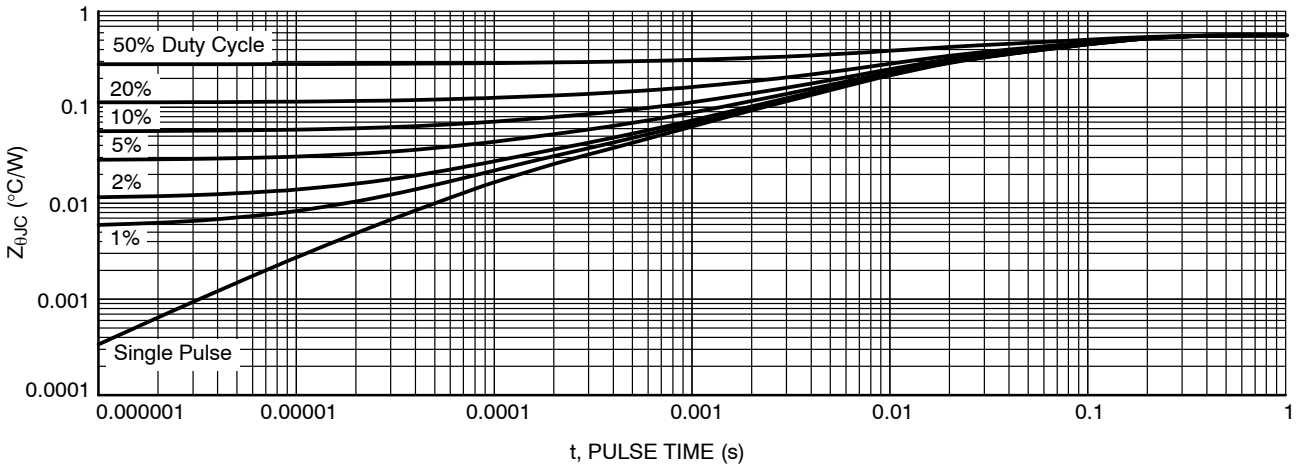


Figure 13. Junction−to−Ambient Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMTSC4D2N10G	4D2N10G	TDFNW8 (Pb−Free)	3000 / Tape & Reel

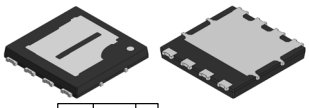
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

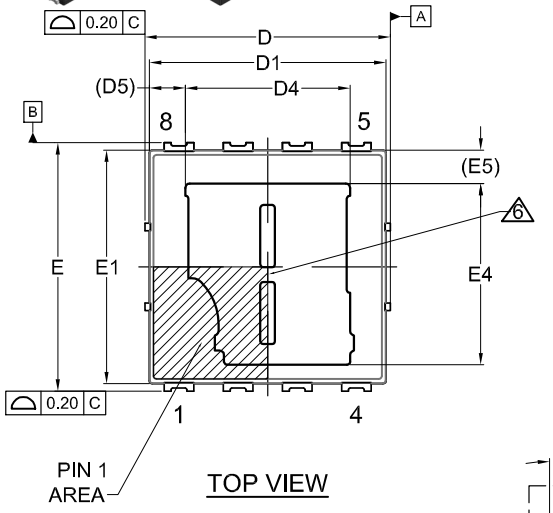
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

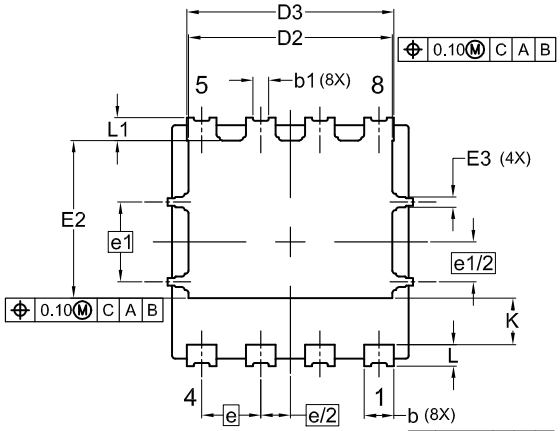
ON Semiconductor®

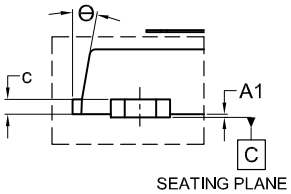
TDFNW8 8.3x8.4, 2P, DUAL COOL, OPTION 3
CASE 507AS
ISSUE B

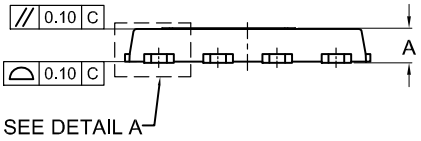
DATE 29 MAR 2021



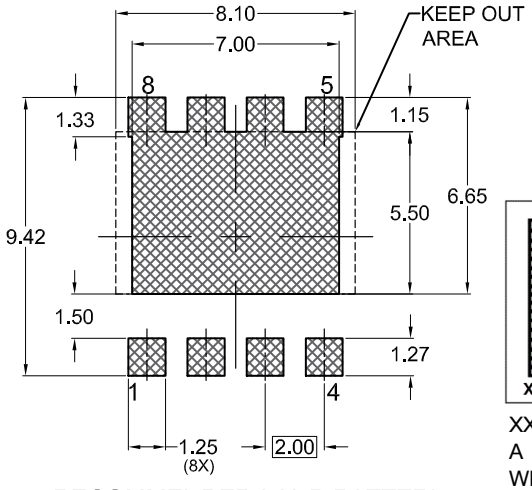








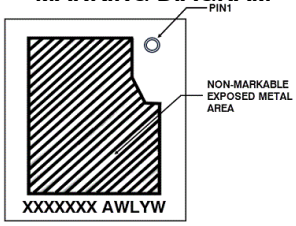
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. SLOT PARTITION IS OPTIONAL.



RECOMMENDED LAND PATTERN

(For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.)

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.82	0.92	1.02
A1	0.00	---	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
D4	5.52	5.67	5.82
D5	1.16 REF		
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
E4	6.08	6.23	6.38
E5	1.13 REF		
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	---	12°

DOCUMENT NUMBER:	**98AON95716G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**TDFNW8 8.3x8.4, 2P, DUAL COOL, OPTION 3**		**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2018

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales