

Notification Number:	20190807001	Notification Date:	Sept. 4, 2019
Title:	Data Sheet for DLPC3430 and DLPC3435		
Customer Contact:	Dlp-pcn-team@list.ti.com	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part Number Change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product data sheet(s) is being updated as summarized below.

Input frame rate capability increased from 120 Hz to 240 Hz when used with firmware v7.3.2 or greater. Additionally, the following data sheet revision change history provides further details.

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2019) to Revision E	Page
• General datasheet formatting and ordering refresh	1
• Deleted mention of mirror parking time from PARKZ pin description and moved to a specification table.....	7
• Changed JTAG pin names from Reserved to proper names	7
• Deleted support for adjustable DATAEN_CMD polarity	8
• Deleted mention of a specific 3D command	8
• Deleted support for adjusting PCLK capture edge in software	8
• Changed the description of how to use the CMP_OUT pin and corrected how the comparator must use GPIO_10 (RC_CHARGE) instead of CMP_PWM	10
• Deleted support for CMP_PWM	10
• Added note about VCC_INTF power up recommendations if slave devices are on the I ² C bus	10
• Deleted mention of unsupported keypad inputs	11
• Corrected optional MTR_SENSE support to GPIO_18 instead of GPIO_19	11
• Deleted mention of unsupported light sensor on GPIO_13 and GPIO_12	11
• Deleted reference of the RC_CHARGE circuit being used for the light sensor and added reference of it being used for the thermistor	11

Revision History (continued)

• Deleted reference of the LS_PWR circuit being used for the light sensor	11
• Deleted mention of the unsupported LABB output sample and hold sensor control signal	11
• Deleted misleading note about GPIO pins defaulting to inputs	11
• Clarified GPIO_03 - GPIO_01 pins are required to be used as a SPI1 port	12
• Corrected how pins are mentioned that are only available on the DLPC3435	13
• Added missing I/O definition 10	14
• Deleted unneeded VCC_INTF and VCC_FLSH absolute maximum values	15
• Added high voltage tolerant note to Absolute Maximum Ratings table	15
• Changed incorrect pin tolerance	16
• Changed Power Electrical Characteristics table to reflect updated power measurement values and techniques	17
• Deleted reference to unsupported IDLE mode	17
• Added note that the power numbers vary depending on the utilized software	17
• Changed and fixed incorrect test conditions for current drive strengths	18
• Deleted redundant $ V_{OD} $ specification which is referenced in later sections	18
• Added minimum and maximum values for V_{OH} for I/O type 4	18
• Added minimum and maximum values for V_{OL} for I/O type 4	18
• Deleted incorrect reference to 2.5V, 24mA drive	18
• Corrected I ² C buffer test conditions	18
• Deleted incorrect steady-state common mode voltage reference	18
• Changed high voltage tolerant I/O note to only refer to the I ² C buffer and changed VCC to VCC_INTF	18
• Added $ V_{OD} $ minimum and maximum values, and changed the typical value	21
• Added high-level output voltage minimum and maximum values for the sub-LVDS DMD interface, deleted redundant mention of specification, and changed the typical value	21
• Added low-level output voltage minimum and maximum values for the sub-LVDS DMD interface, deleted redundant mention of specification, and changed the typical value	21
• Corrected the name of the DMD Low-Speed signals from inputs to outputs	22
• Deleted $V_{OH(DC)}$ maximum and $V_{OL(DC)}$ minimum values	22
• Added note about DMD input specs being met if a proper series termination resistor is used	22
• Deleted reference of selecting unsupported oscillator frequency	23
• Corrected system oscillator clock period to match clock frequency	23
• Changed pulse duration percent spec from a maximum to a minimum	23
• Added condition for VDD rise time	23
• Deleted the incorrect part of the $t_{p_{TV0}}$ definition	24
• Changed minimum total vertical blanking equation	24
• Increased maximum PCLK from 150MHz to 155MHz	25
• Deleted reference to various signal's active edges being configurable	25
• Changed the minimum flash SPI_CLK frequency	27
• Corrected flash interface clock period to match clock frequency	27
• Added Other Timing Requirements section to more clearly list signal transition time requirements	27
• Changed DMD HS Clock switching rate from maximum to nominal and added accompanying clock specification	28
• Added DMD Parking Switching Characteristics section	28
• Added the Chipset Component Usage Specification section to clarify chipset support requirements	28
• Changed how chipset support is mentioned in the Detailed Description section	29
• Increased maximum frame rate from 122 Hz to 242 Hz	30
• Deleted support for 3D video over DSI	30
• Deleted reference to internal software tools and clarified how firmware affects the supported resolution and frame	

Revision History (continued)

rates	30
• Added note stating bits per pixel limitation at 120 Hz with DSI input	30
• Added note that up to four DSI lanes may be required to fully utilize the bandwidth	30
• Deleted mention of sequencer sync mode as its generally assumed to be auto	30
• Clarified note about VSYNC_WE needing to remain active	31
• Deleted support for changing the clock active edge and clarified support of changing the sync active edge	31
• Changed the DATAEN_CMD signal to not be optional	31
• Added note that LP mode is required during vertical time for DSI	33
• Changed requirement related to DSI initialization	33
• Deleted incorrect DSI data type; see software programmers guide instead	34
• Added information that the parallel interface isn't ready to accept data until the auto-initialization process is completed ..	35
• Changed how the 500 ms startup time is described	35
• Changed SPI flash key timing parameter access frequency minimum and maximum values	35
• Added a new maximum frequency requirement for the SPI flash.	37
• Changed maximum flash size supported from 16Mb to 64Mb	37
• Deleted SPI signal routing section	37
• Deleted support for a light sensor integrated with the DLPC34xx controller	39
• Added missing timing definitions	40
• Clarified that the mentioned SDR clock speed is the typical value	43
• Changed how the DMD Sub-LVDS Interface requirements are mentioned	43
• Deleted DMD Interface stack-up image	43
• Deleted equation concerning DMD interface system timing margin	43
• Changed the description of how PROJ_ON affects the power supplies	46
• Changed which signals are listed as tri-stated at power up and which signals are pulled low	51
• Changed 1-oz copper plane recommendation	53
• Deleted reference to unsupported option of variable frequency reference clock	54
• Added additional DMD data and DMD clock signal matching requirements	57
• Changed maximum mismatch from $\pm 0.1''$ to $\pm 1.0''$	57
• Changed incorrect signal matching requirement table note	57
• Added missing DMD HS layout signal requirements	58
• Changed differential signal layer change to a recommendation	59
• Changed wording requiring no more than two vias on certain DMD signals	59
• Changed device markings image and definitions	61

The data sheet number will be changing.

Change From:	Change To:
DLPS038D	DLPS038E

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/lit/ds/symlink/dlpc3430.pdf
http://www.ti.com/lit/ds/symlink/dlpc3435.pdf

Reason for Change:

To accurately reflect device characteristics while increasing frame rate capability from 120 Hz to 240 Hz when used with firmware v7.3.2 or greater.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact except enabling increased input frame rate functionality. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this notification:

None

Product Affected:
DLPC3430CZVBR, DLPC3435ZEZ, DLPC3435CZEZ

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

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