

MJB44H11 (NPN), NJVMJB44H11 (NPN), MJB45H11 (PNP), NJVMJB45H11 (PNP)



ON Semiconductor®

<http://onsemi.com>

Complementary Power Transistors

D²PAK for Surface Mount

Complementary power transistors are for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

Features

- Low Collector–Emitter Saturation Voltage – $V_{CE(sat)} = 1.0 \text{ V (Max) @ } 8.0 \text{ A}$
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs
- Epoxy Meets UL 94 V–0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
Machine Model, C > 400 V
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- Pb–Free Packages are Available

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current – Continuous – Peak	I_C	10 20	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	50 0.4	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0 0.016	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	$^\circ\text{C}$

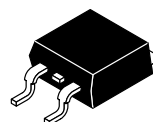
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	75	$^\circ\text{C/W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**SILICON POWER
TRANSISTORS
10 AMPERES,
80 VOLTS, 50 WATTS**

MARKING DIAGRAM



**D²PAK
CASE 418B
STYLE 1**



x = 4 or 5
A = Assembly Location
Y = Year
WW = Work Week
G = Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping [†]
MJB44H11G	D ² PAK (Pb–Free)	50 Units/Rail
MJB44H11T4G	D ² PAK (Pb–Free)	800/Tape & Reel
NJVMJB44H11T4G	D ² PAK (Pb–Free)	800/Tape & Reel
MJB45H11G	D ² PAK (Pb–Free)	50 Units/Rail
MJB45H11T4G	D ² PAK (Pb–Free)	800/Tape & Reel
NJVMJB45H11T4G	D ² PAK (Pb–Free)	800/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (I _C = 30 mA, I _B = 0)	V _{CEO(sus)}	80	-	-	Vdc
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , V _{BE} = 0)	I _{CES}	-	-	10	μA
Emitter Cutoff Current (V _{EB} = 5 Vdc)	I _{EBO}	-	-	50	μA

ON CHARACTERISTICS

Collector-Emitter Saturation Voltage (I _C = 8 Adc, I _B = 0.4 Adc)	V _{CE(sat)}	-	-	1.0	Vdc
Base-Emitter Saturation Voltage (I _C = 8 Adc, I _B = 0.8 Adc)	V _{BE(sat)}	-	-	1.5	Vdc
DC Current Gain (V _{CE} = 1 Vdc, I _C = 2 Adc)	h _{FE}	60	-	-	-
DC Current Gain (V _{CE} = 1 Vdc, I _C = 4 Adc)		40	-	-	-

DYNAMIC CHARACTERISTICS

Collector Capacitance (V _{CB} = 10 Vdc, f _{test} = 1 MHz)	C _{cb}	MJB44H11, NJVMJB44H11	-	130	-	pF
		MJB45H11, NJVMJB45H11	-	230	-	
Gain Bandwidth Product (I _C = 0.5 Adc, V _{CE} = 10 Vdc, f = 20 MHz)	f _T	MJB44H11, NJVMJB44H11	-	50	-	MHz
		MJB45H11, NJVMJB45H11	-	40	-	

SWITCHING TIMES

Delay and Rise Times (I _C = 5 Adc, I _{B1} = 0.5 Adc)	t _d + t _r	MJB44H11, NJVMJB44H11	-	300	-	ns
		MJB45H11, NJVMJB45H11	-	135	-	
Storage Time (I _C = 5 Adc, I _{B1} = I _{B2} = 0.5 Adc)	t _s	MJB44H11, NJVMJB44H11	-	500	-	ns
		MJB45H11, NJVMJB45H11	-	500	-	
Fall Time (I _C = 5 Adc, I _{B1} = I _{B2} = 0.5 Adc)	t _f	MJB44H11, NJVMJB44H11	-	140	-	ns
		MJB45H11, NJVMJB45H11	-	100	-	

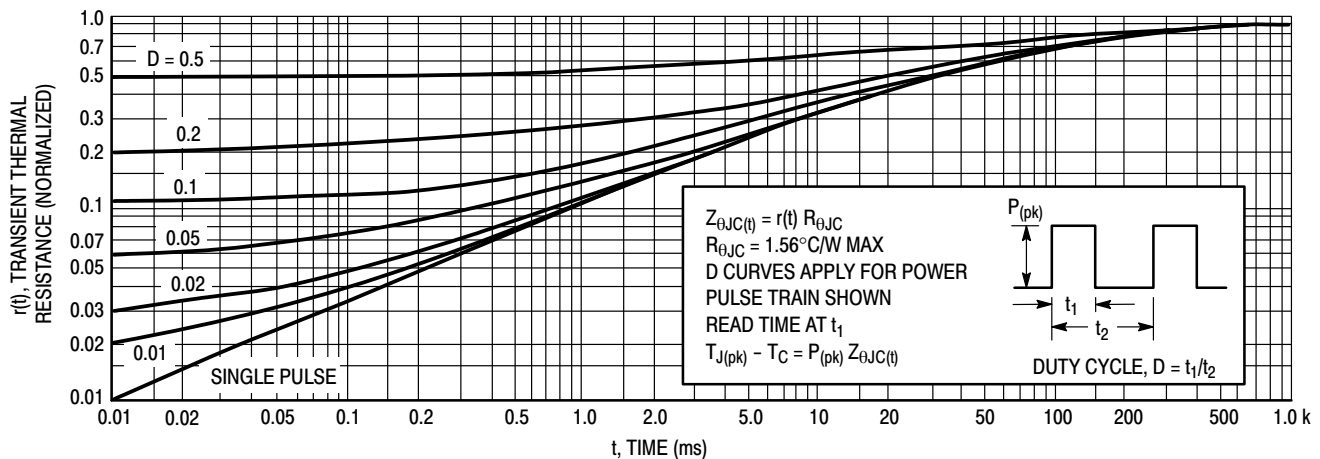


Figure 1. Thermal Response

MJB44H11 (NPN), NJVMJB44H11 (NPN), MJB45H11 (PNP), NJVMJB45H11 (PNP)

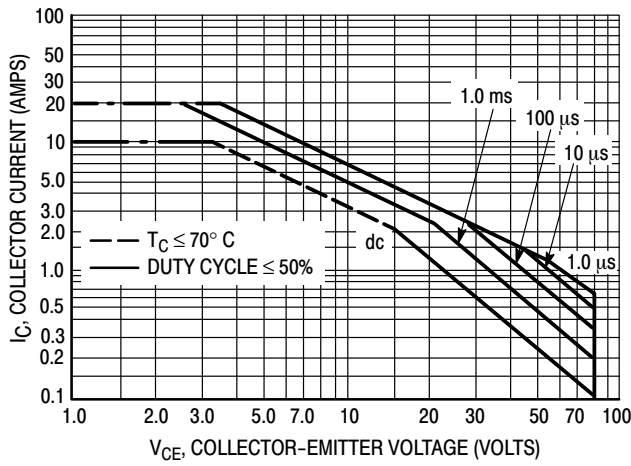


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

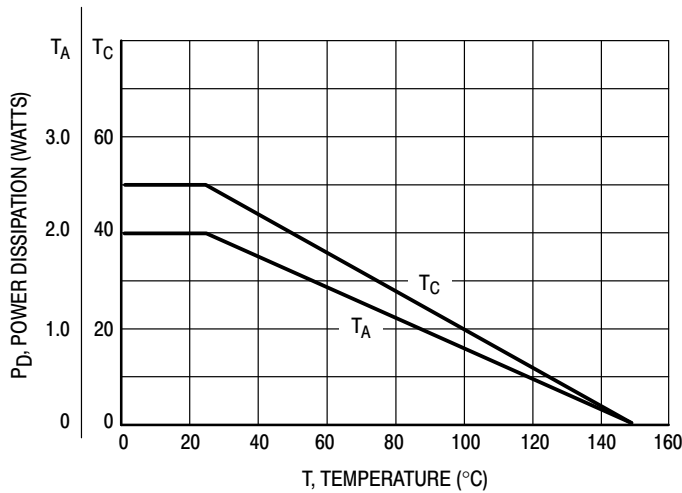


Figure 3. Power Derating

MJB44H11 (NPN), NJVMJB44H11 (NPN), MJB45H11 (PNP), NJVMJB45H11 (PNP)

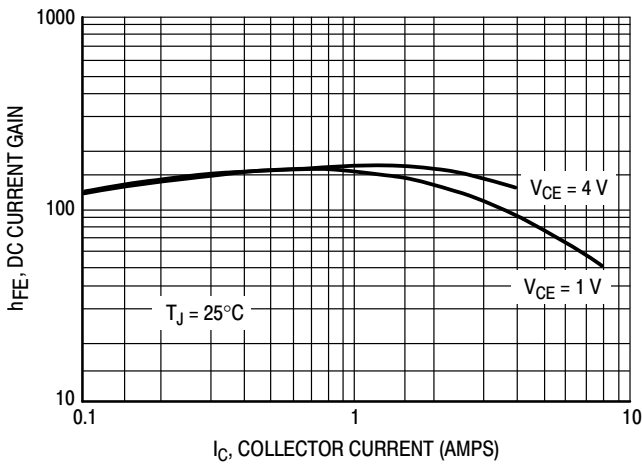


Figure 4. MJB44H11 DC Current Gain

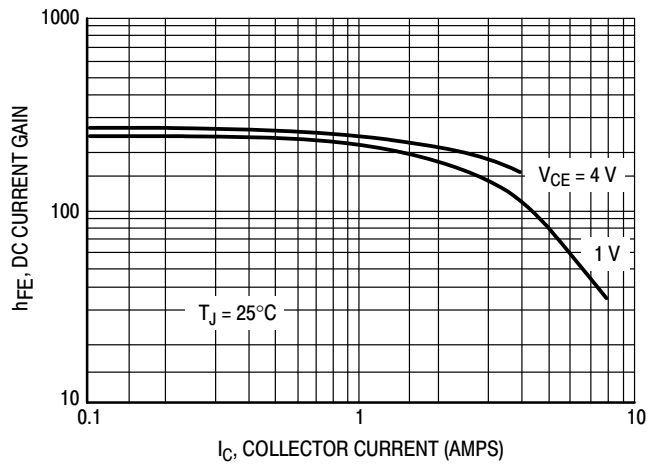


Figure 5. MJB45H11 DC Current Gain

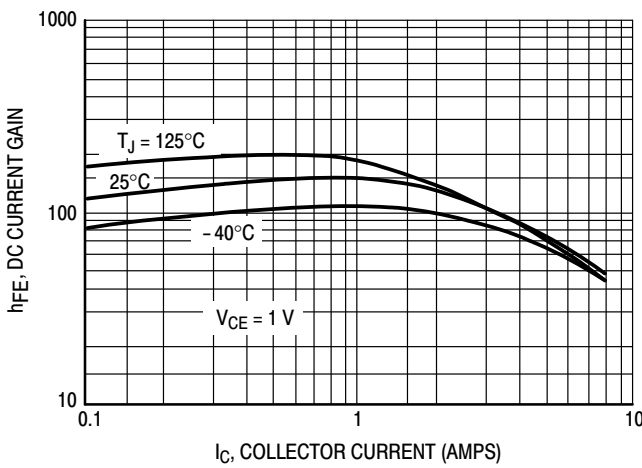


Figure 6. MJB44H11 Current Gain versus Temperature

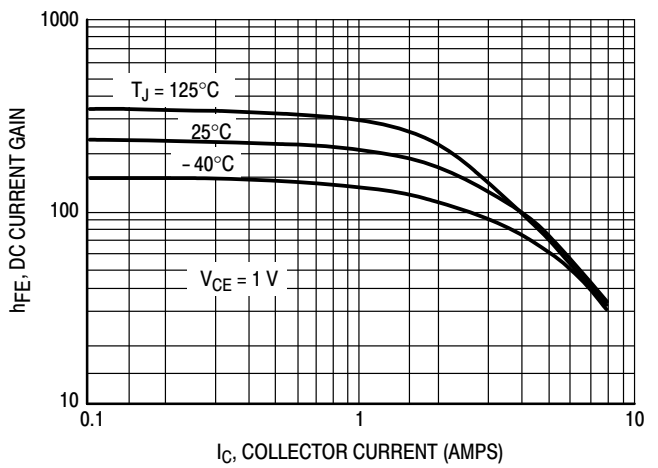


Figure 7. MJB45H11 Current Gain versus Temperature

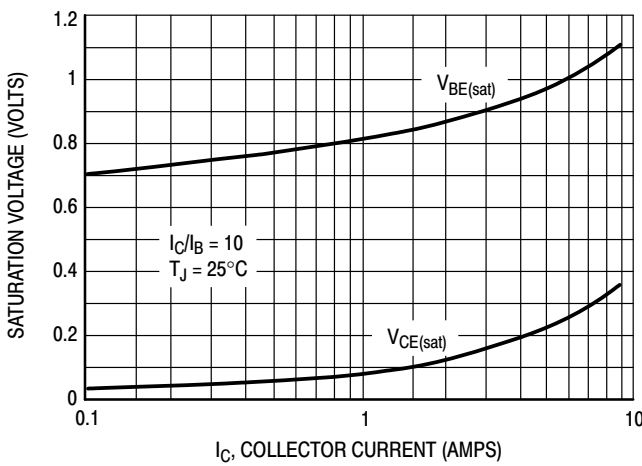


Figure 8. MJB44H11 On-Voltages

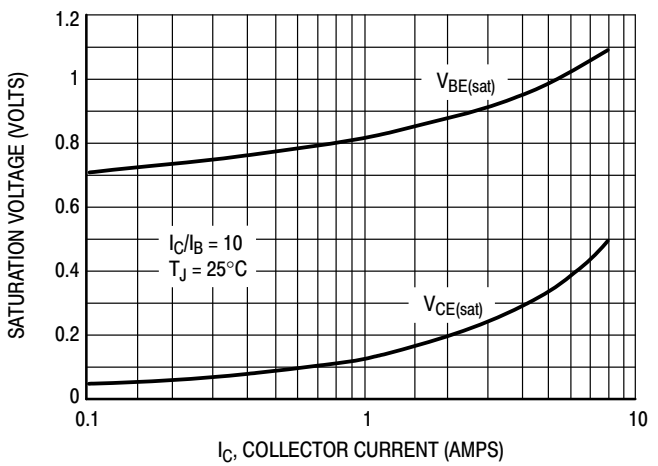


Figure 9. MJB45H11 On-Voltages

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

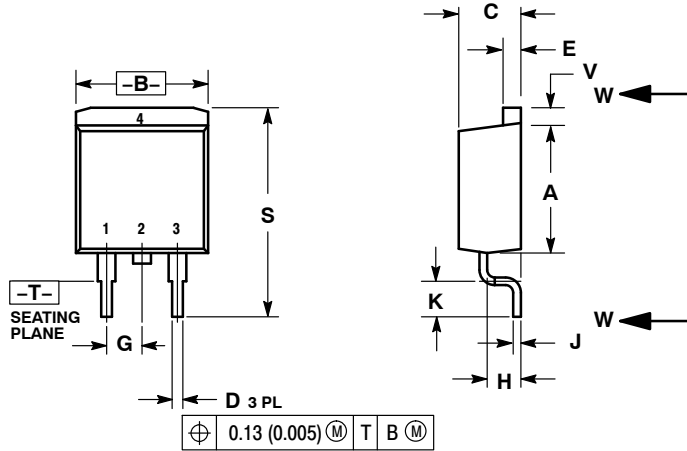
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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

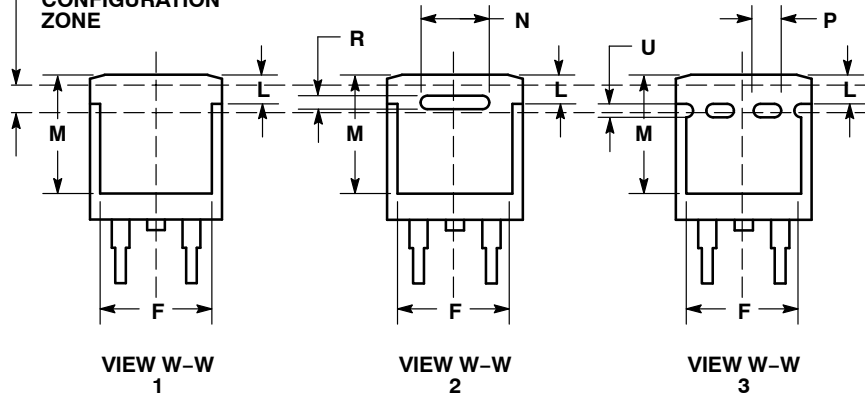


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE CONFIGURATION ZONE



- | | | | | | |
|--|---|---|--|---|--|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE | STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE |
|--|---|---|--|---|--|

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

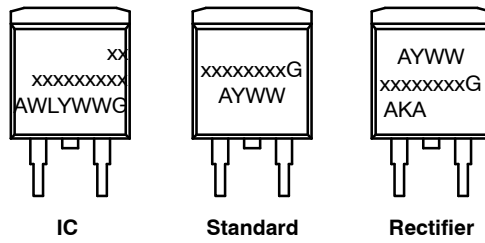
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ISSUE L

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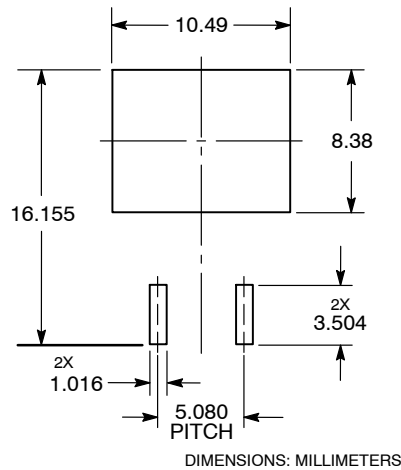
**GENERIC
MARKING DIAGRAM***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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