

# EiceDRIVER™

## 2EDN753x/2EDN853x/2EDN743x

**Dual-channel low-side 5 A gate driver ICs with low output resistance and excellent timing accuracy**

### Description

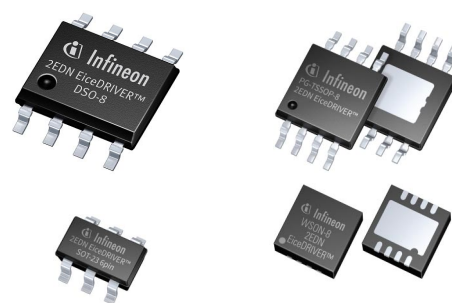
The EiceDRIVER™ 2EDN family is offered in 8-pin DSO, TSSOP and WSON packages as well as in small and versatile 6-pin SOT23 package. High output current capability together with active output voltage clamping, tight timing specifications, and optimized start-up and shut-down times, make the 2EDN family the first choice for many fast-switching applications.

#### Product features

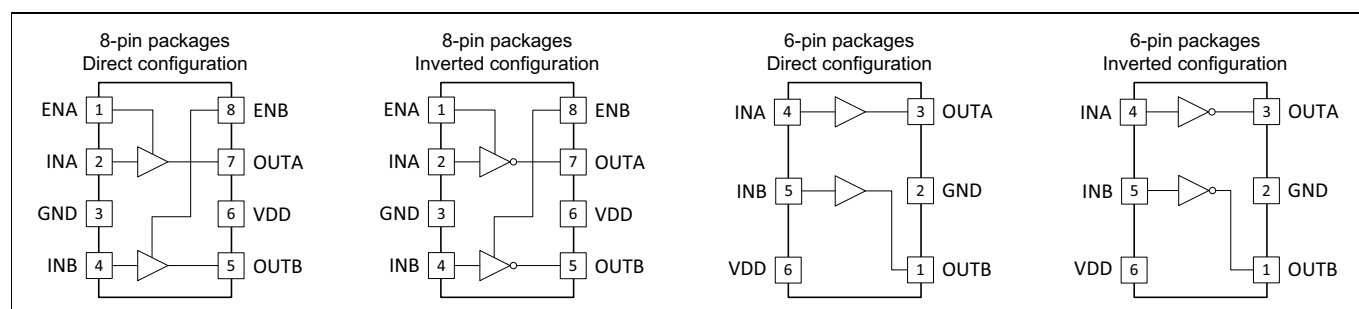
- $\pm 5$  A source/sink currents
- 19 ns typ. propagation delay
- +6/-4 ns propagation delay accuracy
- 1.8  $\mu$ s output start-up time
- 500 ns output shut-down time
- Active output voltage clamping
- -12 V input robustness
- 5 A reverse current robustness
- 4 V and 8 V UVLO options
- Package options:
  - 8-pin DSO, TSSOP, WSON
  - 6-pin SOT23
- Fully qualified for industrial applications according to JEDEC

#### Applications

- Switch-mode power-supplies
- DC-DC power converters
- Synchronous rectification stages
- Power factor correction systems



#### Available device configurations



Peak output current	Inputs	8-pin DSO		8-pin TSSOP		8-pin WSON	6-pin SOT23
		4V UVLO	8V UVLO	4V UVLO	8V UVLO	4V UVLO	4V UVLO
5 A	direct	2EDN7534F	2EDN8534F	2EDN7534R	2EDN8534R	2EDN7534G	2EDN7534B
	inverting	2EDN7533F	2EDN8533F	2EDN7533R	2EDN8533R	–	2EDN7533B
4 A	direct	2EDN7434F	–	2EDN7434R	–	–	–

**Table of Contents**

**Table of Contents**

	<b>Description</b> .....	<b>1</b>
	<b>Table of Contents</b> .....	<b>2</b>
<b>1</b>	<b>Product versions</b> .....	<b>3</b>
1.1	Logic configuration versions .....	3
1.2	Package versions .....	4
<b>2</b>	<b>Pin configuration and description</b> .....	<b>5</b>
2.1	Input configuration for PG-DSO-8 package .....	5
2.2	Input configuration for PG-TSSOP-8 package .....	6
2.3	Input configuration for PG-WSON-8 package .....	7
2.4	Input configuration for PG-SOT23-6 package .....	8
<b>3</b>	<b>Block diagram</b> .....	<b>9</b>
<b>4</b>	<b>Functional description</b> .....	<b>11</b>
4.1	Introduction .....	11
4.2	Supply voltage .....	11
4.3	Undervoltage lockout (UVLO) function .....	11
4.4	Input configurations .....	11
4.5	Driver outputs .....	12
4.6	Active output voltage clamping .....	12
<b>5</b>	<b>Electrical characteristics</b> .....	<b>13</b>
5.1	Absolute maximum ratings .....	13
5.2	Thermal characteristics .....	13
5.3	Operating range .....	15
5.4	General electrical characteristics .....	15
<b>6</b>	<b>Timing diagrams</b> .....	<b>18</b>
<b>7</b>	<b>Typical characteristics</b> .....	<b>21</b>
<b>8</b>	<b>Application and implementation</b> .....	<b>25</b>
<b>9</b>	<b>Package outlines</b> .....	<b>26</b>
9.1	Device numbers and markings .....	26
9.2	PG-DSO-8 .....	28
9.3	PG-TSSOP-8 .....	30
9.4	PG-WSON-8 .....	32
9.5	PG-SOT23-6 .....	33
<b>10</b>	<b>Revision history</b> .....	<b>35</b>

**Product versions**

# 1 Product versions

The EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x are available in two different logic configurations (direct and inverting), two different undervoltage lockout levels (4 V and 8 V) and four package versions.

## 1.1 Logic configuration versions

The two input logic configurations are identified by the "x" variable in the product code EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x:

- x = 3: inverting input logic
- x = 4: non-inverting/direct input logic

**Table 1** and **Table 2** describe the logic dependence of the output state from undervoltage lockout (UVLO), enable and input pins for the 8-pin and 6-pin variants respectively. If the enable pin ENA (or ENB) is either driven high or left open, the associated gate driver output depends on the respective input pin. If the enable pin ENA (or ENB) is low, the associated OUT pin is low, independent of the input signal. If a UVLO event is triggered, both OUTA and OUTB are kept in a low state, regardless of the input and enable pins status.

The functional description is in **Chapter 3 (Block diagram)** and **Chapter 4 (Functional description)**.

**Table 1 Logic table for DSO-8, TSSOP-8, WSON-8 pin packages**

Inputs					Inverting output		Direct output	
ENA	ENB	INA	INB	UVLO <sup>1)</sup>	OUTA	OUTB	OUTA	OUTB
x	x	x	x	active	L	L	L	L
L	L	x	x	inactive	L	L	L	L
H	L	L	x	inactive	H	L	L	L
H	L	H	x	inactive	L	L	H	L
L	H	x	L	inactive	L	H	L	L
L	H	x	H	inactive	L	L	L	H
H	H	L	L	inactive	H	H	L	L
H	H	H	L	inactive	L	H	H	L
H	H	L	H	inactive	H	L	L	H
H	H	H	H	inactive	L	L	H	H

1) Inactive UVLO:  $V_{DD}$  is above  $UVLO_{ON}$  voltage threshold and control logic drives the output stage.

Active UVLO: an undervoltage lockout event has been triggered

**Table 2 Logic table for SOT23-6 pin package**

Inputs			Inverting output		Direct output	
INA	INB	UVLO <sup>1)</sup>	OUTA	OUTB	OUTA	OUTB
x	x	active	L	L	L	L
L	L	inactive	H	H	L	L
H	L	inactive	L	H	H	L
L	H	inactive	H	L	L	H
H	H	inactive	L	L	H	H

1) Inactive UVLO:  $V_{DD}$  is above  $UVLO_{ON}$  voltage threshold and control logic drives the output stage.

Active UVLO: an undervoltage lockout event has been triggered

## Product versions

### 1.2 Package versions

The EiceDRIVER™ 2EDN family is available in four different package versions. The package type is identified by the last character in the product code:

- the standard PG-DSO-8 is designated by “F” (e.g. 2EDN753xF)
- the small leaded PG-TSSOP-8 is designated by “R” (e.g. 2EDN753xR)
- the leadless PG-WSON-8 is designated by “G” (e.g. 2EDN753xG)
- the ultra tiny PG-SOT23-6 is designated by “B” (e.g. 2EDN753xB)

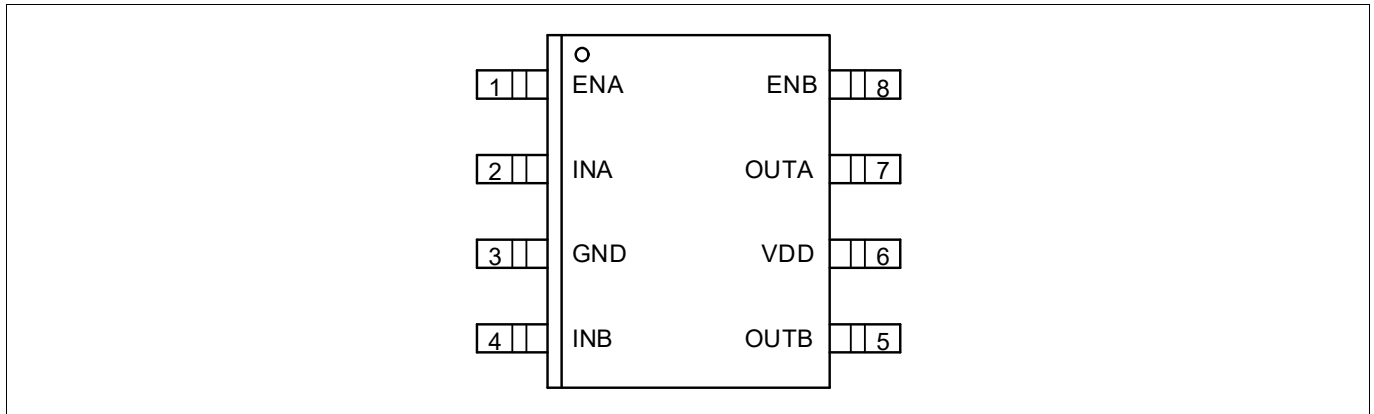
Package drawings are available in [Chapter 9 \(Package outlines\)](#).

**Pin configuration and description**

**2 Pin configuration and description**

**2.1 Input configuration for PG-DSO-8 package**

The pin configuration for all input versions of EiceDRIVER™ 2EDN7534F, 2EDN7434F, 2EDN7533F, 2EDN8534F and 2EDN8533F in the PG-DSO-8 package is shown in **Figure 1**. Diagrams can be viewed in **Chapter 9.2 (PG-DSO-8)**.



**Figure 1 Pin configuration PG-DSO-8, top view**

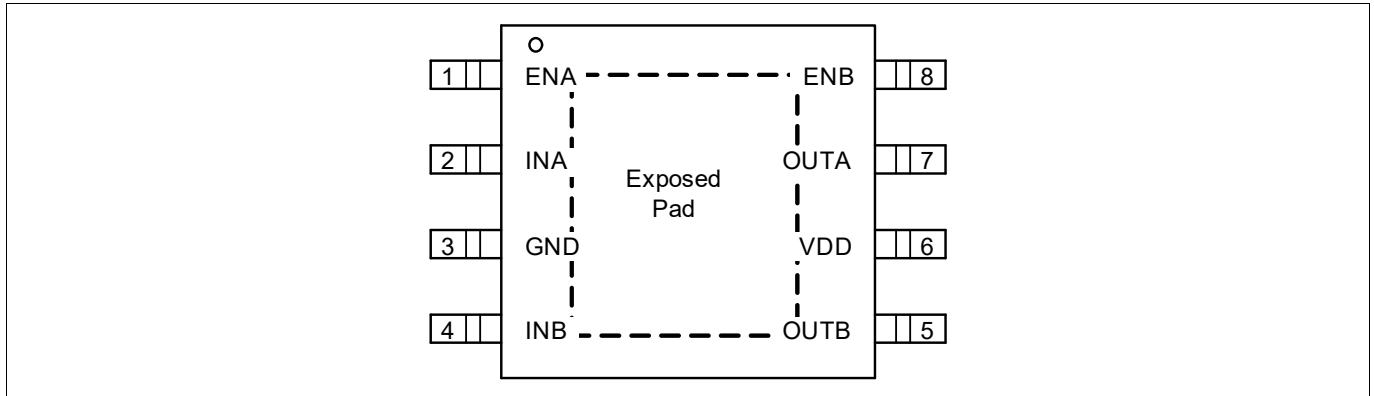
**Table 3 Pin configuration for PG-DSO-8 package**

Pin number	Symbol	Description
1	ENA	<b>Enable input channel A</b> Logic input. If ENA is high or left open, OUTA is controlled by INA. ENA low causes OUTA low
2	INA	<b>Input signal channel A</b> Logic input, controlling OUTA (inverting or non-inverting)
3	GND	<b>Ground</b> Gate driver reference ground
4	INB	<b>Input signal channel B</b> Logic input, controlling OUTB (inverting or non-inverting)
5	OUTB	<b>Driver output channel B</b> Low-impedance output with source and sink capability
6	VDD	<b>Positive supply voltage</b> Operating range 4.5 V/8.6 V to 20 V
7	OUTA	<b>Driver output channel A</b> Low-impedance output with source and sink capability
8	ENB	<b>Enable input channel B</b> Logic Input. If ENB is high or left open, OUTB is controlled by INB. ENB low causes OUTB low

**Pin configuration and description**

**2.2 Input configuration for PG-TSSOP-8 package**

The pin configuration for all input versions of EiceDRIVER™ 2EDN7534R, 2EDN7434R, 2EDN7533R, 2EDN8534R and 2EDN8533R in the PG-TSSOP-8 package is shown in **Figure 2**. Diagrams can be viewed in **Chapter 9.3 (PG-TSSOP-8)**.



**Figure 2 Pin configuration PG-TSSOP-8, top view**

**Table 4 Pin configuration for PG-TSSOP-8 package**

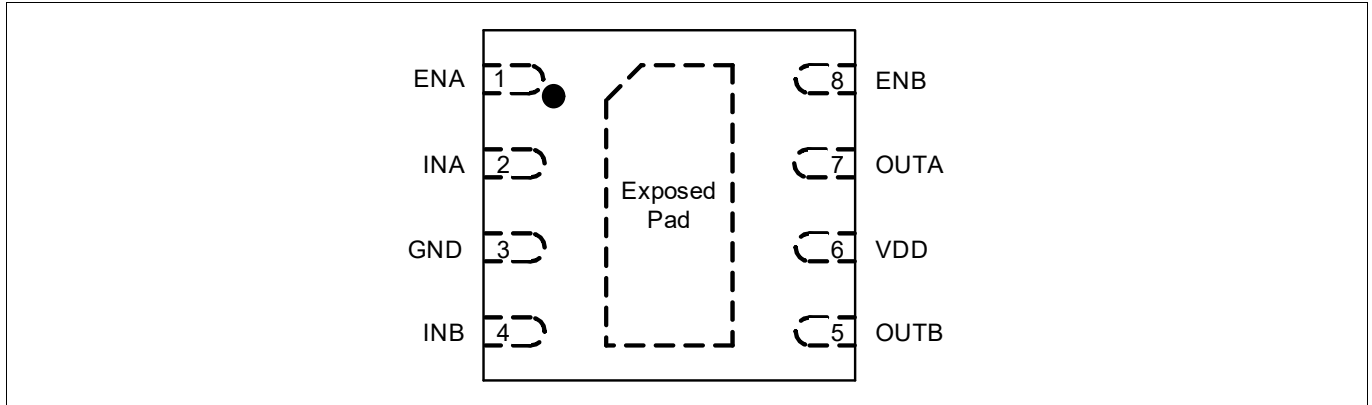
Pin Number	Symbol	Description
1	ENA	<b>Enable input channel A</b> Logic input. If ENA is high or left open, OUTA is controlled by INA. ENA low causes OUTA low
2	INA	<b>Input signal channel A</b> Logic input, controlling OUTA (non-inverting)
3	GND	<b>Ground<sup>1)</sup></b> Gate driver reference ground
4	INB	<b>Input signal channel B</b> Logic input, controlling OUTB (non-inverting)
5	OUTB	<b>Driver output channel B</b> Low-impedance output with source and sink capability
6	VDD	<b>Positive supply voltage</b> Operating range 4.5 V/8.6 V to 20 V
7	OUTA	<b>Driver output channel A</b> Low-impedance output with source and sink capability
8	ENB	<b>Enable input channel B</b> Logic Input. If ENB is high or left open, OUTB is controlled by INB. ENB low causes OUTB low

1) Exposed pad sink of PG-TSSOP-8 packages has to be connected to GND pin

**Pin configuration and description**

**2.3 Input configuration for PG-WSON-8 package**

The pin configuration of EiceDRIVER™ 2EDN7534G in the PG-WSON-8 package is shown in **Figure 3**. Diagrams can be viewed in **Chapter 9.4 (PG-WSON-8)**.



**Figure 3 Pin configuration PG-WSON-8, top view**

**Table 5 Pin configuration for PG-WSON-8 package**

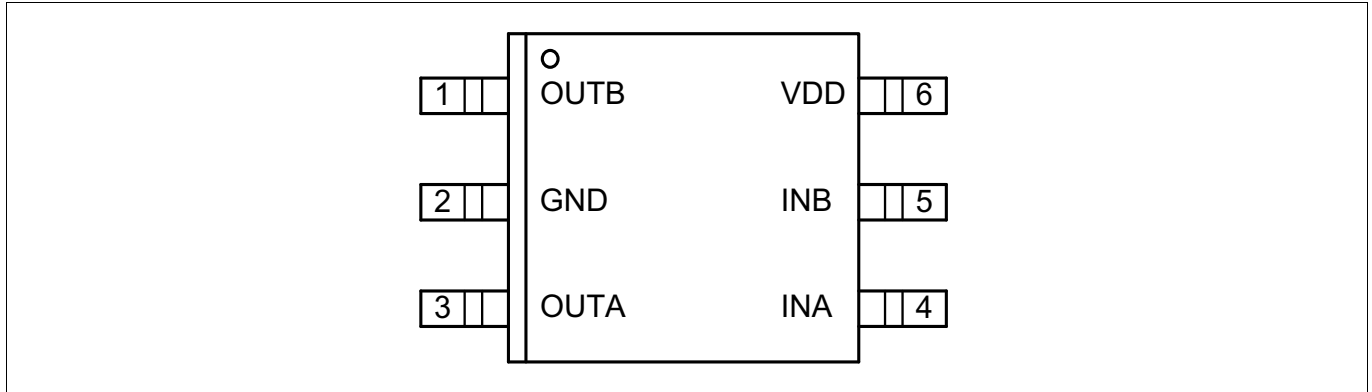
Pin number	Symbol	Description
1	ENA	<b>Enable input channel A</b> Logic input. If ENA is high or left open, OUTA is controlled by INA. ENA low causes OUTA low
2	INA	<b>Input signal channel A</b> Logic input, controlling OUTA (non-inverting)
3	GND	<b>Ground<sup>1)</sup></b> Gate driver reference ground
4	INB	<b>Input signal channel B</b> Logic input, controlling OUTB (non-inverting)
5	OUTB	<b>Driver output channel B</b> Low-impedance output with source and sink capability
6	VDD	<b>Positive supply voltage</b> Operating range 4.5 V to 20 V
7	OUTA	<b>Driver output channel A</b> Low-impedance output with source and sink capability
8	ENB	<b>Enable input channel B</b> Logic Input. If ENB is high or left open, OUTB is controlled by INB. ENB low causes OUTB low

1) Exposed pad of PG-WSON-8 packages has to be connected to GND pin

**Pin configuration and description**

**2.4 Input configuration for PG-SOT23-6 package**

The pin configuration of EiceDRIVER™ 2EDN7534B and 2EDN7533B in the PG-SOT23-6 package is shown in **Figure 4**. Drawings can be viewed in **Chapter 9.5 (PG-SOT23-6)**.



**Figure 4 Pin configuration PG-SOT23-6, top view**

**Table 6 Pin configuration for PG-SOT23-6 package**

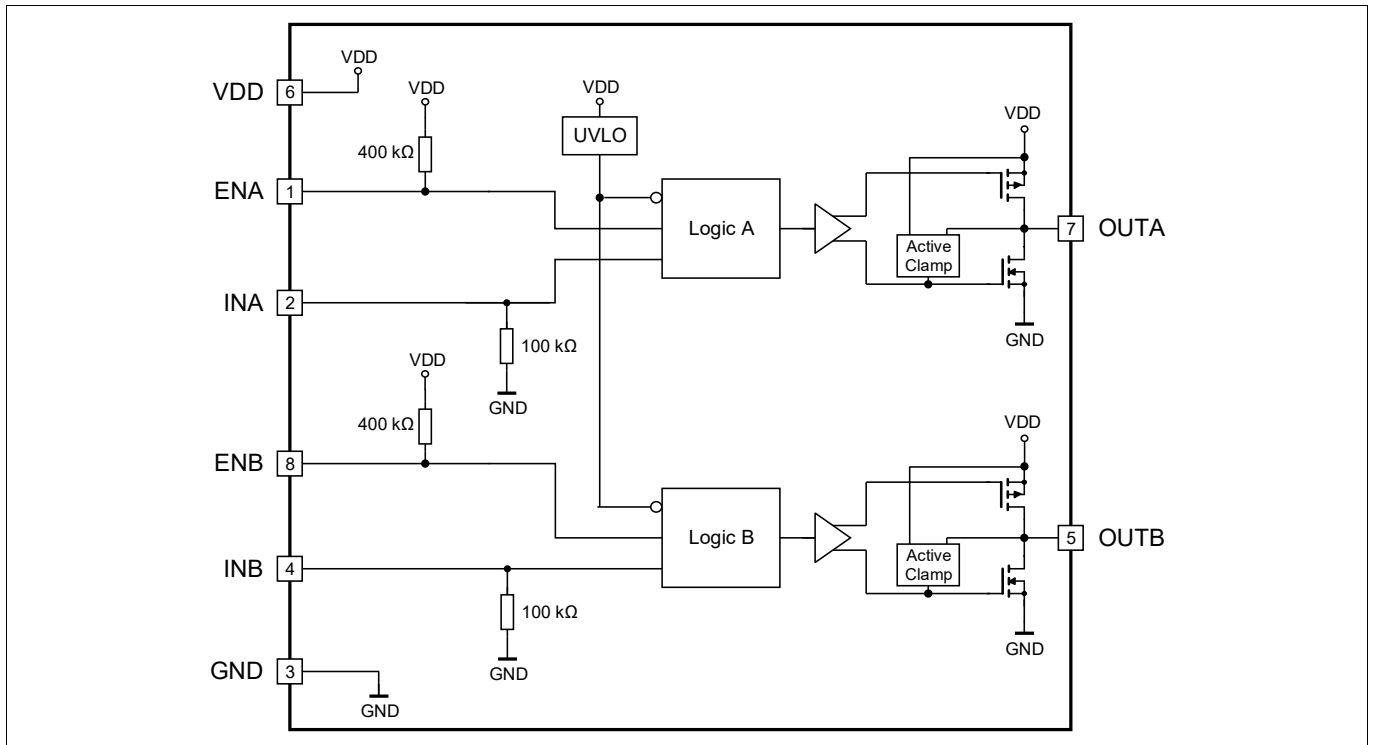
Pin number	Symbol	Description
1	OUTB	<b>Driver output channel B</b> Low-impedance output with source and sink capability
2	GND	<b>Ground</b> Gate driver reference ground
3	OUTA	<b>Driver output channel A</b> Low-impedance output with source and sink capability
4	INA	<b>Input signal channel A</b> Logic input, controlling OUTA (non-inverting)
5	INB	<b>Input signal channel B</b> Logic input, controlling OUTB (non-inverting)
6	VDD	<b>Positive supply voltage</b> Operating range 4.5 V to 20 V



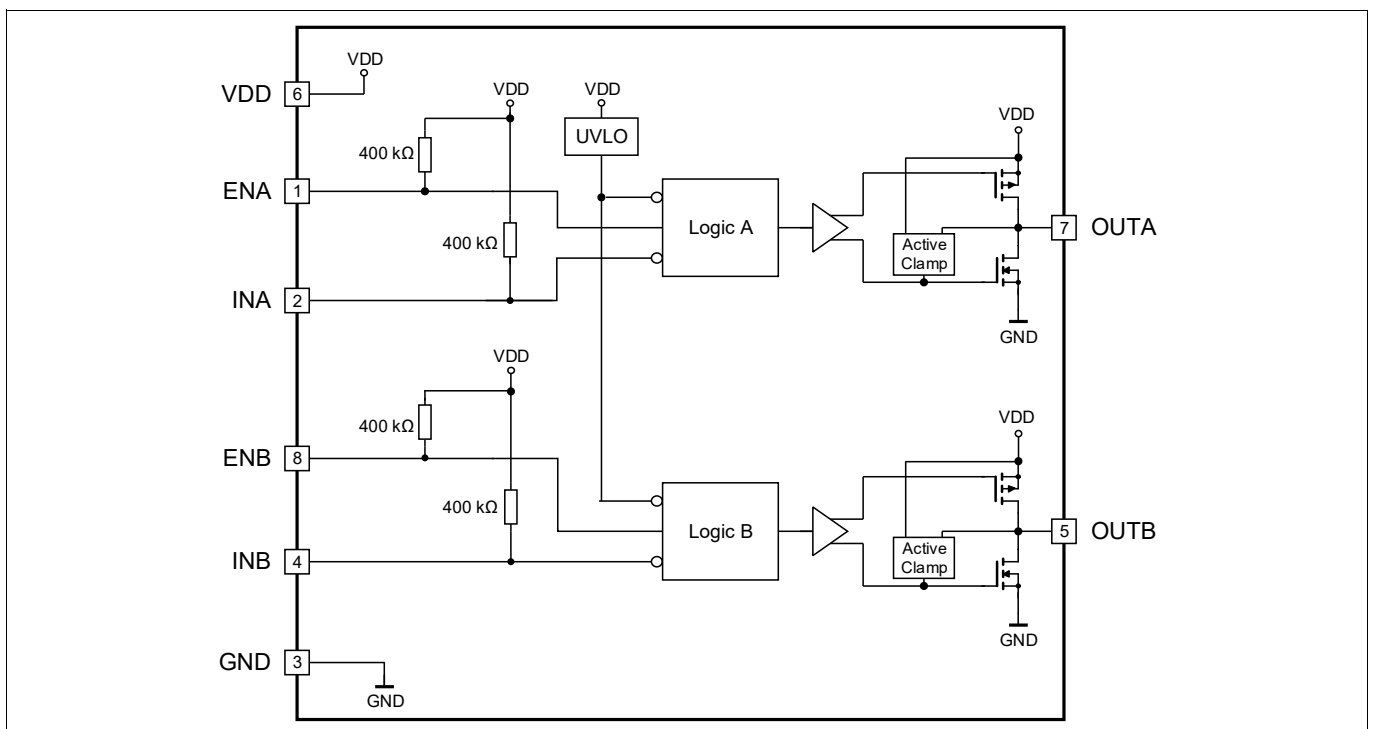
**Block diagram**

**3 Block diagram**

Simplified functional block diagrams for the DSO-8, TSSOP-8, WSON-8 package variants are given in **Figure 5** and **Figure 6**. Block diagrams for the SOT23-6 package variants are shown in **Figure 7** and **Figure 8**. Please refer to functional description in **Chapter 4**.

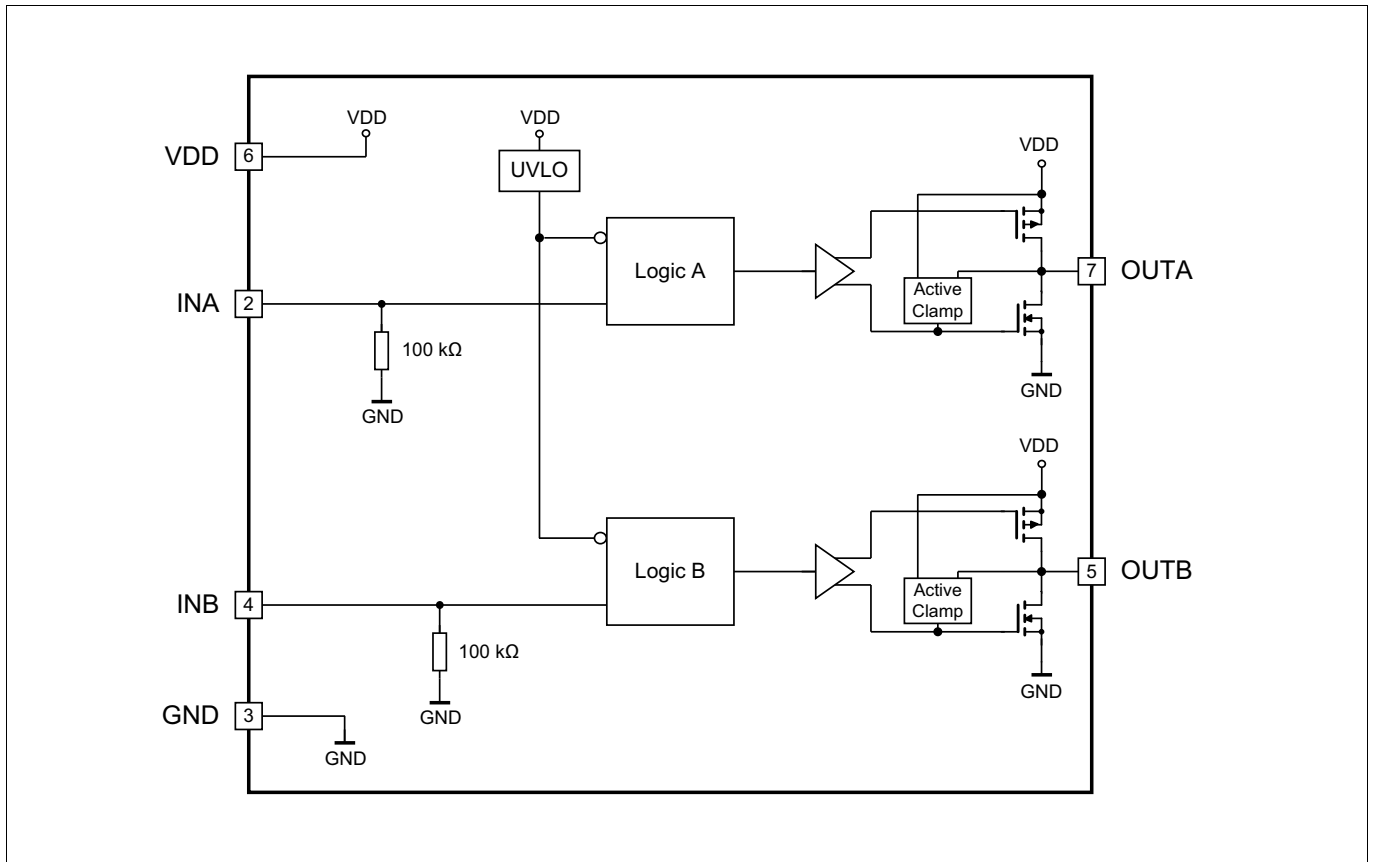


**Figure 5 Simplified block diagram for direct/non-inverting input configuration, 8-pin packages**

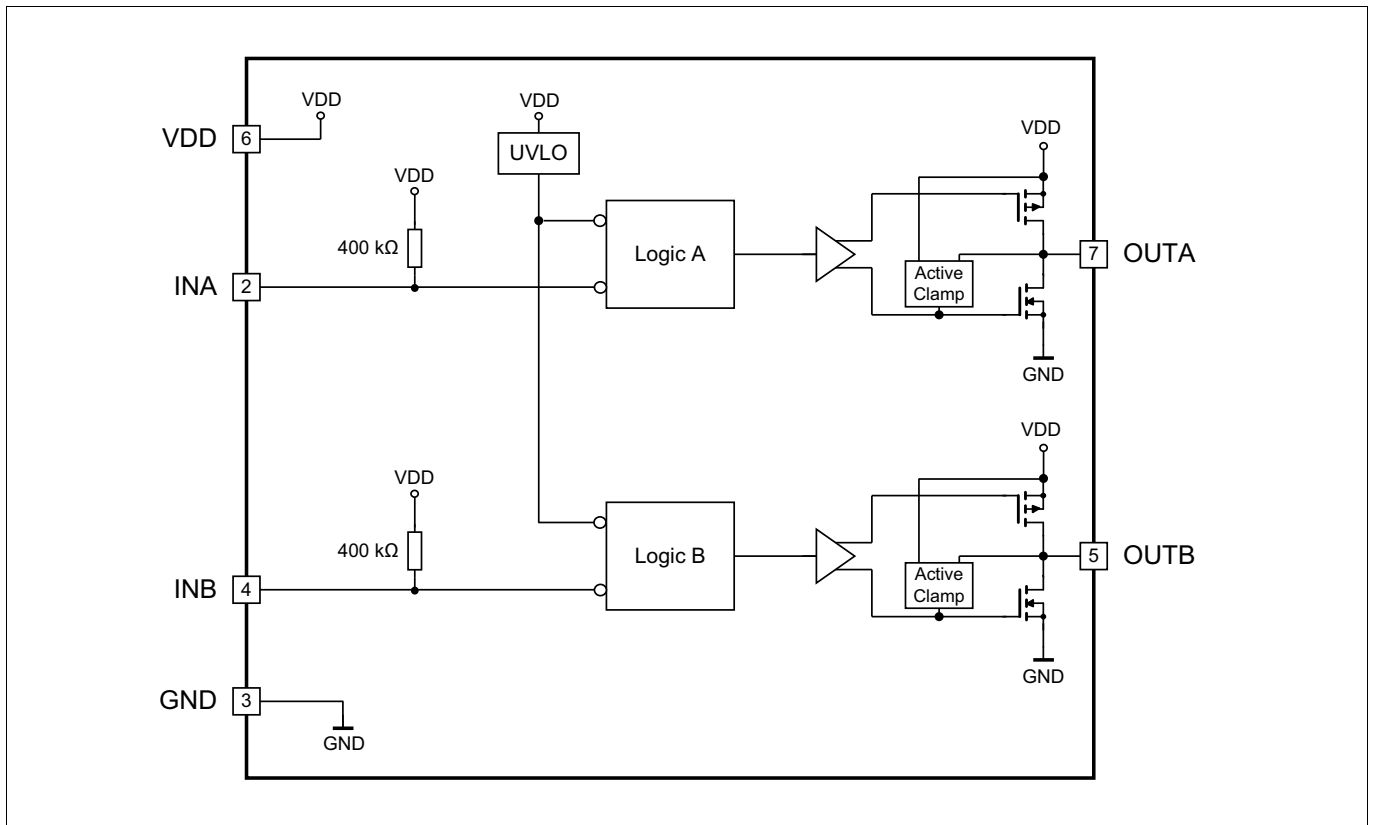


**Figure 6 Simplified block diagram for inverting input configuration, 8-pin packages**

**Block diagram**



**Figure 7** Simplified block diagram for direct/non-inverting input configuration, 6-pin packages



**Figure 8** Simplified block diagram for inverting input configuration, 6-pin packages

**Functional description**

## **4 Functional description**

### **4.1 Introduction**

The EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x is a fast dual-channel driver for low-side switches. Two true rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure high flexibility and cover a high variety of applications.

An extended negative voltage range protects input pins against ground shifts. No current flows over the ESD structure in the IC during a negative input level. All outputs are robust against reverse current. During the interaction with the power MOSFET, reverse reflected power is handled by the internal output stage.

All inputs are compatible with LV-TTL signal levels. The threshold voltages have a typical hysteresis of 0.9 V, that is constant over the supply voltage range.

EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x ensure optimal performance in fast-switching applications because of the low delays and rise/fall times. The maximum skew between Channel A and Channel B is 2 ns.

### **4.2 Supply voltage**

The maximum operating supply voltage is 20 V. This high voltage is valuable in order to exploit the full current capability of EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x when driving low  $R_{\text{DS(on)}}$  MOSFETs. The minimum operating supply voltage is set by the undervoltage lockout function to a typical default values of 4.2 V for the 4 V-UVLO variant and 8 V for the 8 V-UVLO variant.

### **4.3 Undervoltage lockout (UVLO) function**

The undervoltage lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. This protects power MOSFETs from running into linear mode, preventing excessive power dissipation if the voltage is not enough to completely turn on the switches.

The UVLO level is set to a typical value of 4.2 V or 8 V (with hysteresis). UVLO of 4.2 V is normally used for logic level MOSFETs. For standard and high voltage superjunction MOSFETs, a UVLO voltage of typical 8 V is available.

**Table 7 UVLO turn-on and turn-off thresholds**

<b>Nominal UVLO level</b>	<b>UVLO turn-on threshold (typ.)</b>	<b>UVLO turn-off threshold (typ.)</b>
4.2 V	4.2 V	3.9 V
8.0 V	8.0 V	7.0 V

### **4.4 Input configurations**

As described in [Chapter 1](#), EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x are available in two different configurations with respect to the logic of the input pins.

The enable inputs are internally pulled up to a logic high voltage, i.e. the driver is enabled with these pins left open. The direct PWM inputs are internally pulled down to a logic low voltage. This prevents a switch-on event during power up and a not driven input condition. Version with inverted PWM input have an internal pull up resistor to prevent unwanted switch-on.

All inputs are compatible with LV-TTL levels and provide a hysteresis of 0.9 V typ. This hysteresis is independent of the supply voltage.

All input pins have a negative extended voltage range. This prevents cross-current over single wires during GND shifts between signal source (controller) and driver input.

**Functional description**

**4.5 Driver outputs**

The two rail-to-rail output stages realized with complementary MOS transistors are able to provide a maximum sinking/sourcing current of 5 A (4 A output current versions are also available). This driver output stage has a shoot-through protection and current limiting behavior. After a switching event, current limitation is raised up to achieve the typical current peak for an excellent fast reaction time of the following power MOS transistor.

The output impedances for the sourcing p-channel MOS have typical values of 0.8 Ω for 2EDN753x and 2EDN853x and 1.0 Ω for 2EDN743x. The output impedances for the sinking n-channel MOS transistor have typical values of 0.6 Ω for 2EDN753x and 2EDN853x and 0.8 Ω for 2EDN743x. The use of a p-channel sourcing transistor is crucial for achieving true rail-to-rail behavior and avoiding a source follower’s voltage drop.

Gate drive outputs are kept actively low in case of floating ENx or INx inputs, or during startup or power down if the supply voltage is below the UVLO threshold.

**4.6 Active output voltage clamping**

The undervoltage lockout (UVLO) protection ensures no driver operation when the supply voltage is below the UVLO threshold. However, this is not sufficient to keep output low when  $V_{DD}$  is far below the UVLO threshold. As a result, fast dv/dt of the switches could trigger undesired  $V_{gs}$  of the driven device, leading to abnormal turn-ons.

The fast active output voltage clamping of EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x is intended to actively keep the driver output low when the VDD voltage is between 1.2V and  $UVLO_{ON}$  threshold, overcoming the unwanted turn-on issue listed above and ensuring safe off state before device operation.

This structure allows fast reaction and effective clamping of the output pins (OUTx). The exact reaction time depends on the power supply ( $V_{DD}$ ) and on the output voltage levels. Undervoltage Lockout together with the output active clamping ensure that the output is actively held low in case of insufficient supply voltage.

**Table 8 Logic table in case of insufficient supply voltages**

<b>Inputs</b>	<b>Supplies</b>	<b>Output</b>
INx	$V_{DD}$	OUTx
x	$1.2\text{ V} < V_{DD} < UVLO_{VDD,ON}$	L

**Electrical characteristics**

**5 Electrical characteristics**

*Note: The absolute maximum ratings are listed in **Table 9**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**5.1 Absolute maximum ratings**

**Table 9 Absolute maximum ratings**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Positive supply voltage	$V_{DD}$	-0.3	–	22	V	–
Voltage at pins INA, INB, ENA, ENB	$V_{IN}$	-12	–	22	V	–
Voltage at pins OUTA, OUTB	$V_{OUT}$	-0.3	–	$V_{DD} + 0.3$	V	1)
		-2	–	$V_{DD} + 2$	V	Repetitive pulse < 200 ns <sup>2)</sup>
Reverse current peak at pins OUTA, OUTB	$I_{SNKREV}$	-5	–	–	$A_{pk}$	< 500 ns
	$I_{SRCREV}$	–	–	5		
Junction temperature	$T_J$	-40	–	150	°C	–
Storage temperature	$T_S$	-55	–	150	°C	–
ESD capability	$V_{ESD}$	–	–	0.5	kV	Charged Device Model (CDM) <sup>3)</sup>
ESD capability	$V_{ESD}$	–	–	2.0	kV	Human Body Model (HBM) <sup>4)</sup>

- 1) Voltage spikes resulting from reverse current peaks are allowed
- 2) Values are verified by characterization on bench
- 3) According to JESD22-002
- 4) According to JESD22-A114-B (discharging 100 pF capacitor through 1.5 kΩ resistor)

**5.2 Thermal characteristics**

**Table 10 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>PG-DSO-8, <math>T_{amb} = 25^\circ\text{C}</math></b>						
Thermal resistance junction-ambient	$R_{thJA25}$	–	111	–	K/W	1)
Thermal resistance junction-case (top)	$R_{thJC25}$	–	66	–	K/W	2)
Thermal resistance junction-board	$R_{thJB25}$	–	59	–	K/W	3)
Characterization parameter junction-top	$\Psi_{thJC25}$	–	12	–	K/W	4)
Characterization parameter junction-board	$\Psi_{thJB25}$	–	57	–	K/W	5)

**Electrical characteristics**

**Table 10 Thermal characteristics (continued)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>PG-TSSOP-8, <math>T_{amb} = 25^{\circ}\text{C}</math></b>						
Thermal resistance junction-ambient	$R_{thJA25}$	–	48	–	K/W	1)6)
Thermal resistance junction-case (top)	$R_{thJP25}$	–	74	–	K/W	2)
Thermal resistance junction-board	$R_{thJB25}$	–	22.5	–	K/W	3)6)
Characterization parameter junction-top	$\Psi_{thJC25}$	–	3	–	K/W	4)6)
Characterization parameter junction-board	$\Psi_{thJB25}$	–	21	–	K/W	5)6)
<b>PG-WSON-8, <math>T_{amb} = 25^{\circ}\text{C}</math></b>						
Thermal resistance junction-ambient	$R_{thJA25}$	–	46	–	K/W	1)6)
Thermal resistance junction-case (top)	$R_{thJP25}$	–	73	–	K/W	2)
Thermal resistance junction-board	$R_{thJB25}$	–	18	–	K/W	3)6)
Characterization parameter junction-top	$\Psi_{thJC25}$	–	2	–	K/W	4)6)
Characterization parameter junction-board	$\Psi_{thJB25}$	–	17.5	–	K/W	5)6)
<b>PG-SOT23-6, <math>T_{amb} = 25^{\circ}\text{C}</math></b>						
Thermal resistance junction-ambient	$R_{thJA25}$	–	163	–	K/W	1)
Thermal resistance junction-case (top)	$R_{thJC25}$	–	69	–	K/W	2)
Thermal resistance junction-board	$R_{thJB25}$	–	36	–	K/W	3)
Characterization parameter junction-case (top)	$\Psi_{thJC25}$	–	13	–	K/W	4)
Characterization parameter junction-board	$\Psi_{thJB25}$	–	36	–	K/W	5)

- 1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a
- 2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88
- 3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8
- 4) The characterization parameter junction-top, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $R_{th}$ , using a procedure described in JESD51-2a (sections 6 and 7)
- 5) The characterization parameter junction-board, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $R_{th}$ , using a procedure described in JESD51-2a (sections 6 and 7)
- 6) Characterization done on a JEDEC 2s2p PCB with thermal via array connected to the first inner copper layer under the exposed pad

**Electrical characteristics**

**5.3 Operating range**

**Table 11 Operating range**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{DD}$	4.5	–	20	V	Min. defined by UVLO
Logic input voltage	$V_{IN}$	-10	–	20	V	–
Junction temperature	$T_J$	-40	–	150	°C	<sup>1)</sup>

1) Continuous operation above 125°C may reduce life time

**5.4 General electrical characteristics**

Unless otherwise noted, min./max. values of characteristics are the lower and upper limits respectively. They are valid within the full operating range. The supply voltage is  $V_{DD} = 12\text{ V}$ . Typical values are given at  $T_J = 25^\circ\text{C}$ .

**Table 12 Power supply**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VDD quiescent current	$I_{VDDQU1}$	0.5	0.9	1.2	mA	OUT = high, $V_{DD} = 12\text{ V}$
VDD quiescent current	$I_{VDDQU2}$	0.3	0.5	0.7	mA	OUT = low, $V_{DD} = 12\text{ V}$

**Table 13 Undervoltage lockout for logic level MOSFET**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{ON}$	–	4.2	4.5	V	–
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{OFF}$	3.6	3.9	–	V	–
UVLO threshold hysteresis	$UVLO_{HYS}$	0.25	0.3	0.35	V	–

**Table 14 Undervoltage lockout for standard and superjunction MOSFET version**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{ON}$	–	8.0	8.6	V	–
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{OFF}$	6.5	7.0	–	V	–
UVLO threshold hysteresis	$UVLO_{HYS}$	0.8	1.0	1.2	V	–

**Electrical characteristics**

**Table 15 Logic inputs INA, INB, ENA, ENB**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	$V_{INH}$	1.9	2.1	2.3	V	–
Input voltage threshold for transition HL	$V_{INL}$	1.0	1.2	1.4	V	–
Input pull up resistor	$R_{INH}$	–	400	–	k $\Omega$	1)
Input pull down resistor	$R_{INL}$	–	100	–	k $\Omega$	2)

1) Inputs with initial high logic level

2) Inputs with initial low logic level

**Table 16 Static output characteristics for 2EDN753x, 2EDN853x**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level (sourcing) output resistance	$R_{ONSRC}$	0.4	0.8	1.4	$\Omega$	$I_{SRC} = 50 \text{ mA}$
High level (sourcing) output current <sup>1)</sup>	$I_{SRCPEAK}$	–	5.0	–	A	–
Low level (sinking) output resistance	$R_{ONSNK}$	0.35	0.6	1.2	$\Omega$	$I_{SNK} = 50 \text{ mA}$
Low level (sinking) output current <sup>1)</sup>	$I_{SNKPEAK}$	–	-5.0	–	A	–

1) Parameter is not subject to production test - verified by design/characterization

**Table 17 Static output characteristics for 2EDN743x**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level (sourcing) output resistance	$R_{ONSRC}$	0.5	1.0	1.7	$\Omega$	$I_{SRC} = 50 \text{ mA}$
High level (sourcing) output current <sup>1)</sup>	$I_{SRCPEAK}$	–	4.0	–	A	–
Low level (sinking) output resistance	$R_{ONSNK}$	0.4	0.8	1.45	$\Omega$	$I_{SNK} = 50 \text{ mA}$
Low level (sinking) output current <sup>1)</sup>	$I_{SNKPEAK}$	–	-4.0	–	A	–

1) Parameter is not subject to production test - verified by design/characterization



**Electrical characteristics**

**Table 18 Dynamic Characteristics (see Figure 9, Figure 10, Figure 11 and Figure 12)**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input/Enable to output propagation delay	$t_{PDHh}$	15	19	25	ns	$C_{LOAD} = 1.8 \text{ nF}$ , $V_{DD} = 12 \text{ V}$ ; low to high transition at Input/Enable
Input/Enable to output propagation delay	$t_{PDHl}$	15	19	25	ns	$C_{LOAD} = 1.8 \text{ nF}$ , $V_{DD} = 12 \text{ V}$ high to low transition at Input/Enable
Input/Enable to output propagation delay mismatch between the two channels on the same IC	$\Delta t_{PD}$	–	–	2	ns	–
Rise time <sup>1)</sup>	$t_{RISE}$	–	8.6	15	ns	$C_{LOAD} = 1.8 \text{ nF}$ , $V_{DD} = 12 \text{ V}$
Fall time <sup>1)</sup>	$t_{FAIL}$	–	6	13	ns	$C_{LOAD} = 1.8 \text{ nF}$ , $V_{DD} = 12 \text{ V}$
Minimum input pulse width that changes output state <sup>1)</sup>	$t_{PW}$	–	6	10	ns	$C_{LOAD} = 1.8 \text{ nF}$ , $V_{DD} = 12 \text{ V}$
$V_{DD}$ start-up time <sup>1)</sup> from $UVLO_{ON}$ to $OUT_x$	$t_{START}$	–	1.8	–	$\mu\text{s}$	$V_{DD}$ rising to 12 V; see <a href="#">Figure 11</a>
$V_{DD}$ deactivation time <sup>1)</sup> from $UVLO_{OFF}$ to $OUT_x$	$t_{STOP}$	–	500	–	ns	$V_{DD}$ falling from 12 V; see <a href="#">Figure 11</a>
Activation time of output clamping in UVLO condition <sup>1)</sup>	$t_{CLAMP,OUT}$	–	20	–	ns	see <a href="#">Figure 13</a>

1) Parameter is not subject to production test - verified by component verification

Timing diagrams

## 6 Timing diagrams

Figure 9 shows the definition of rise, fall and delay times for the inputs of the non-inverting/direct version (with enable pin high or open).

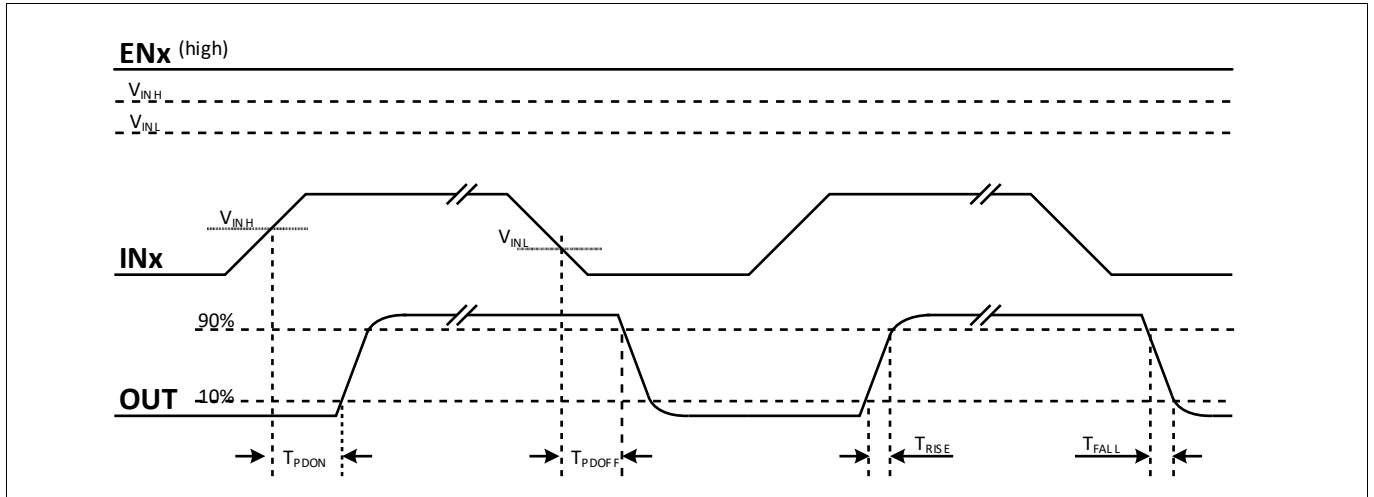


Figure 9 Propagation delay, rise and fall time definition for the direct/non-inverting configuration

Figure 10 shows the definition of rise, fall and delay times for the inputs of the inverting version (with enable pins high or open).

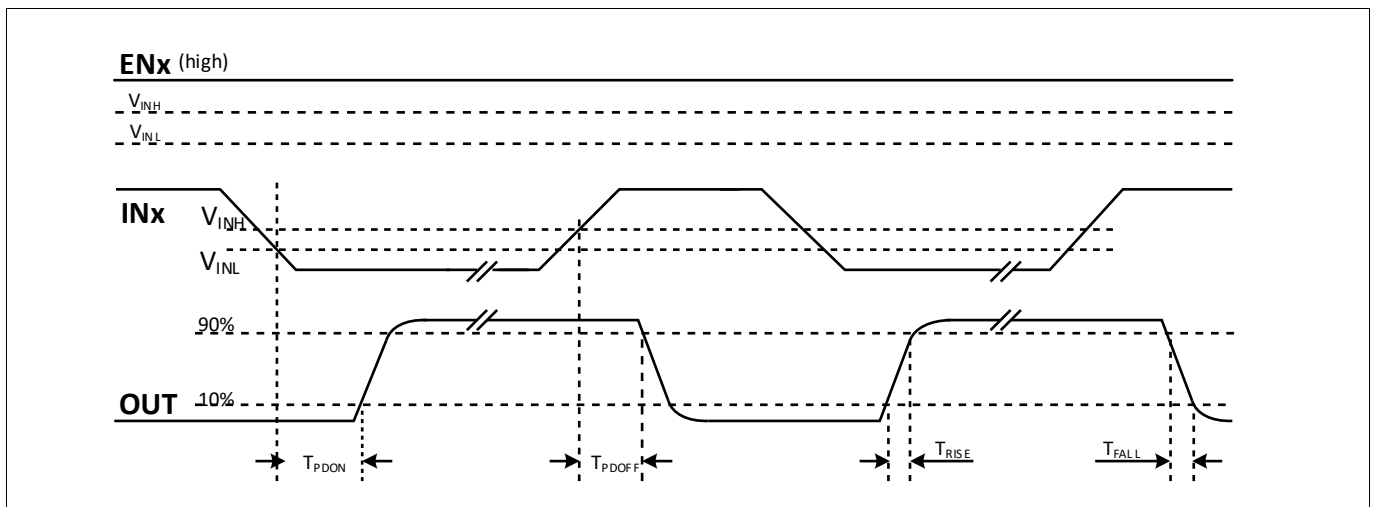
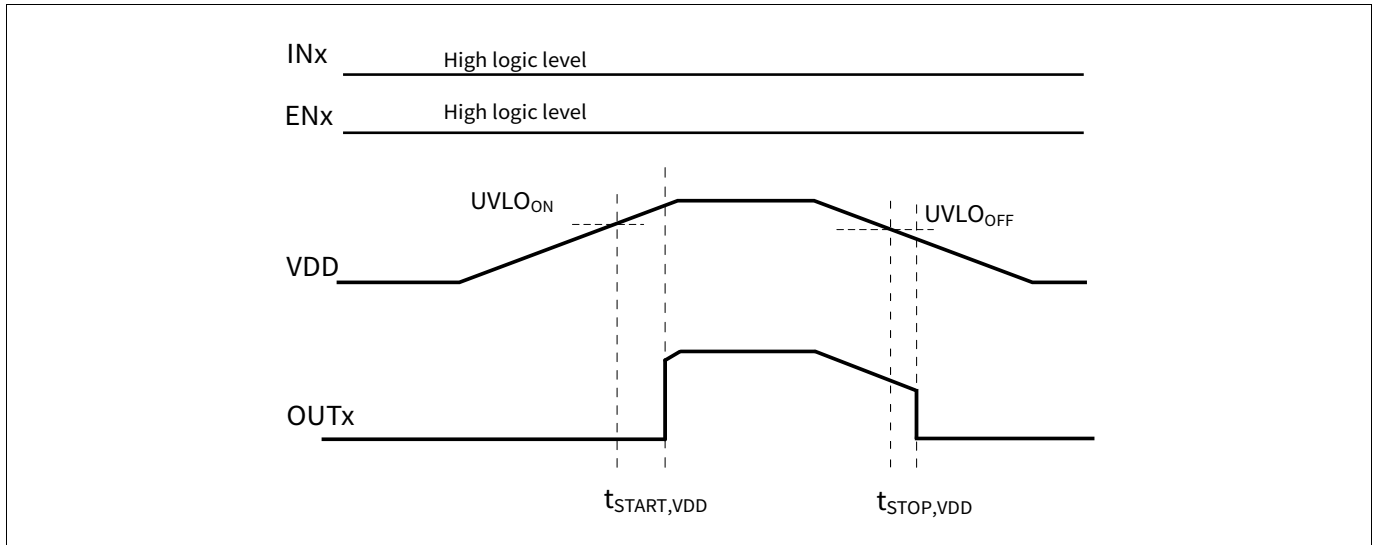


Figure 10 Propagation delay, rise and fall time definition for the inverting configuration

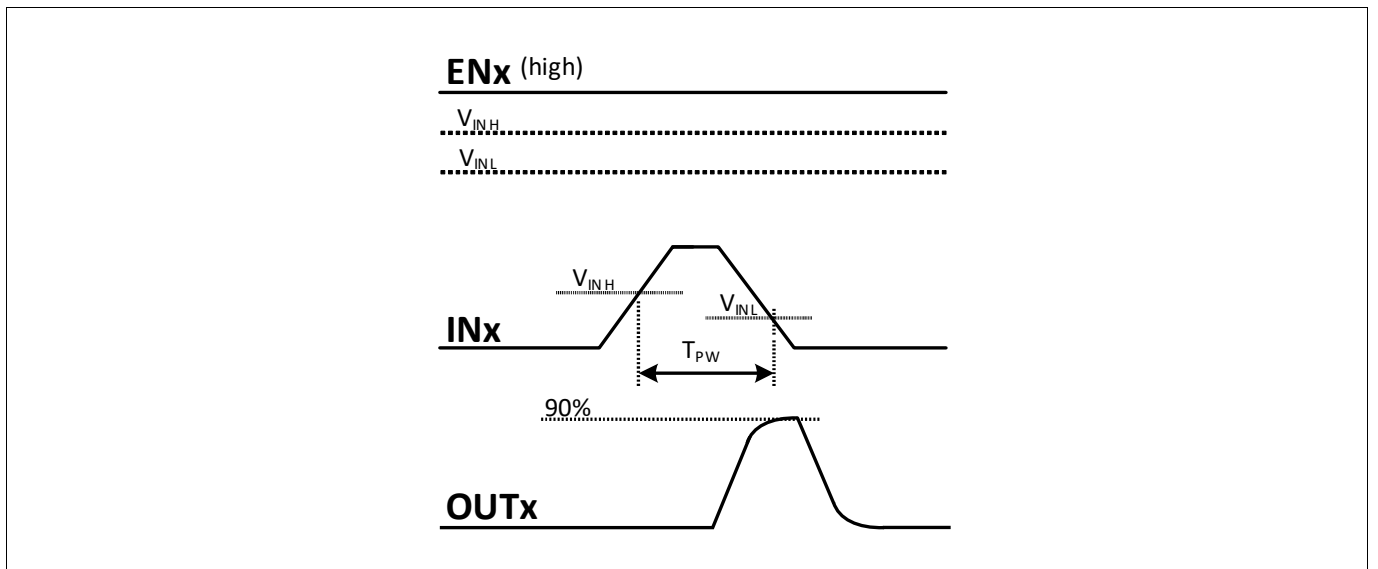
**Timing diagrams**

**Figure 11** illustrates the undervoltage lockout function.



**Figure 11 UVLO behaviour, input ENx and INx drives OUTx normally high**

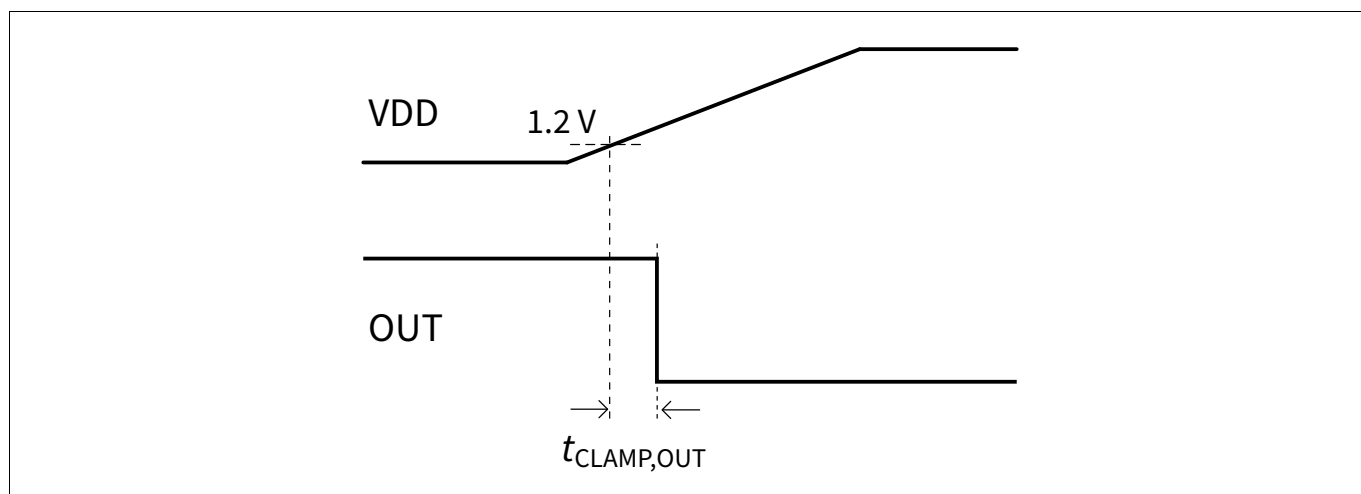
**Figure 12** illustrates the minimum input pulse width that changes output state.



**Figure 12 Minimum input pulse width definition**

**Timing diagrams**

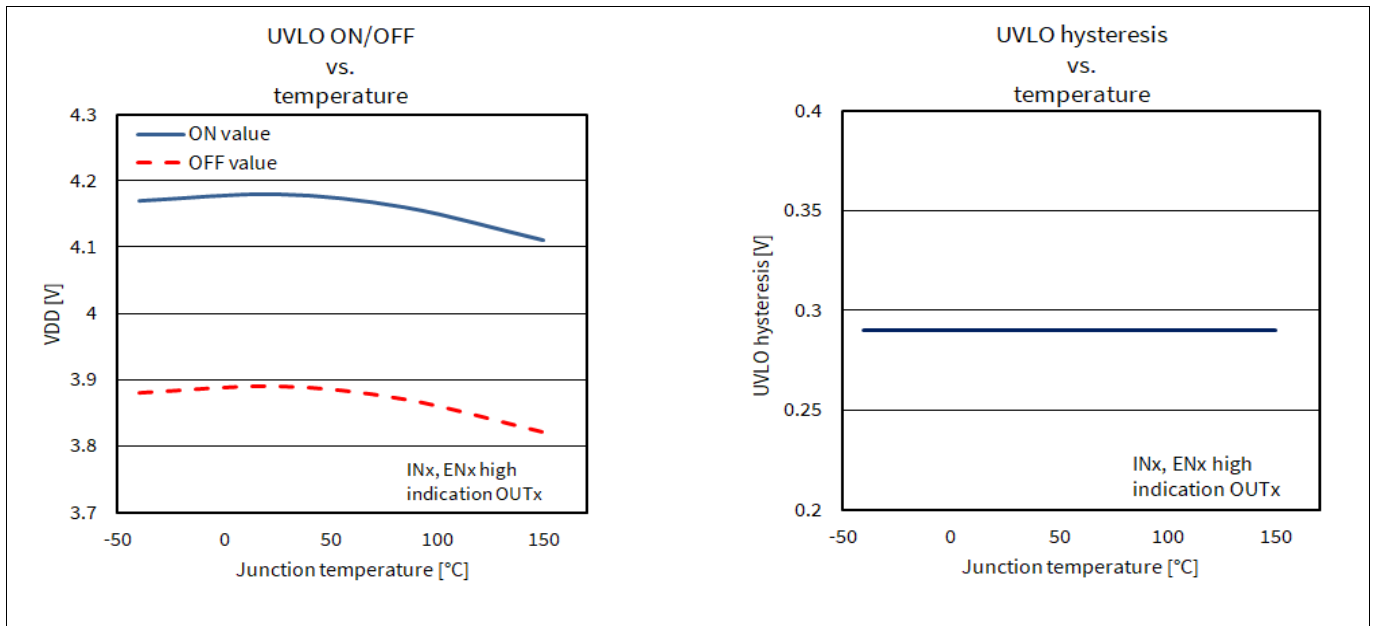
**Figure 13** illustrates  $t_{\text{CLAMP,OUT}}$ , the time required to clamp potential output induced overshoots in UVLO condition ( $V_{\text{DD}} < UVLO_{\text{ON}}$ )



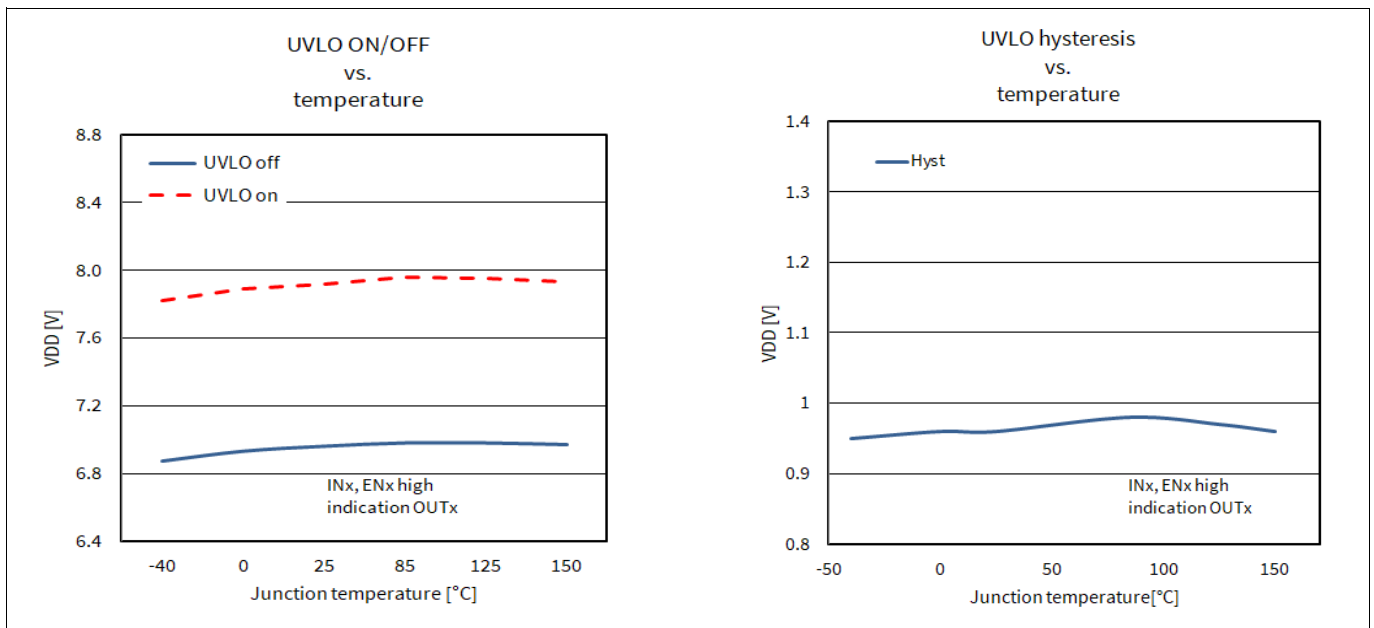
**Figure 13** Activation time of output clamping in UVLO conditions (unloaded output)

Typical characteristics

**7 Typical characteristics**

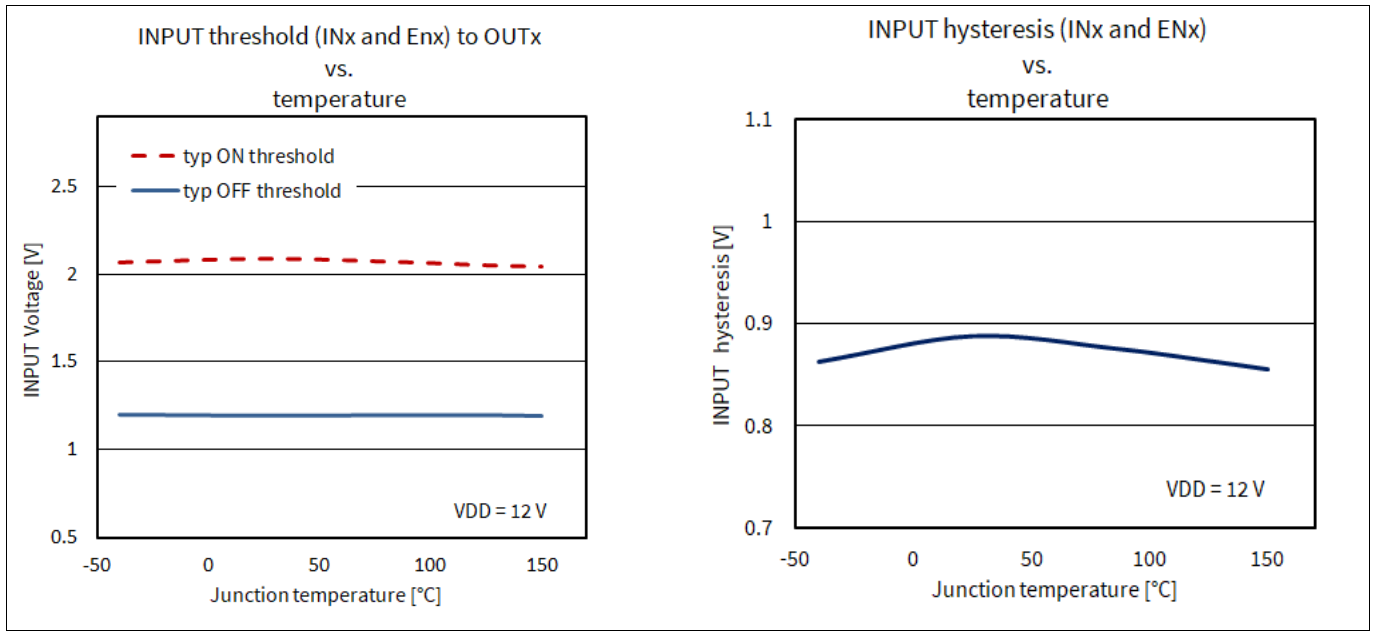


**Figure 14 Typical undervoltage lockout behavior vs. temperature for 2EDN7x (4 V)**

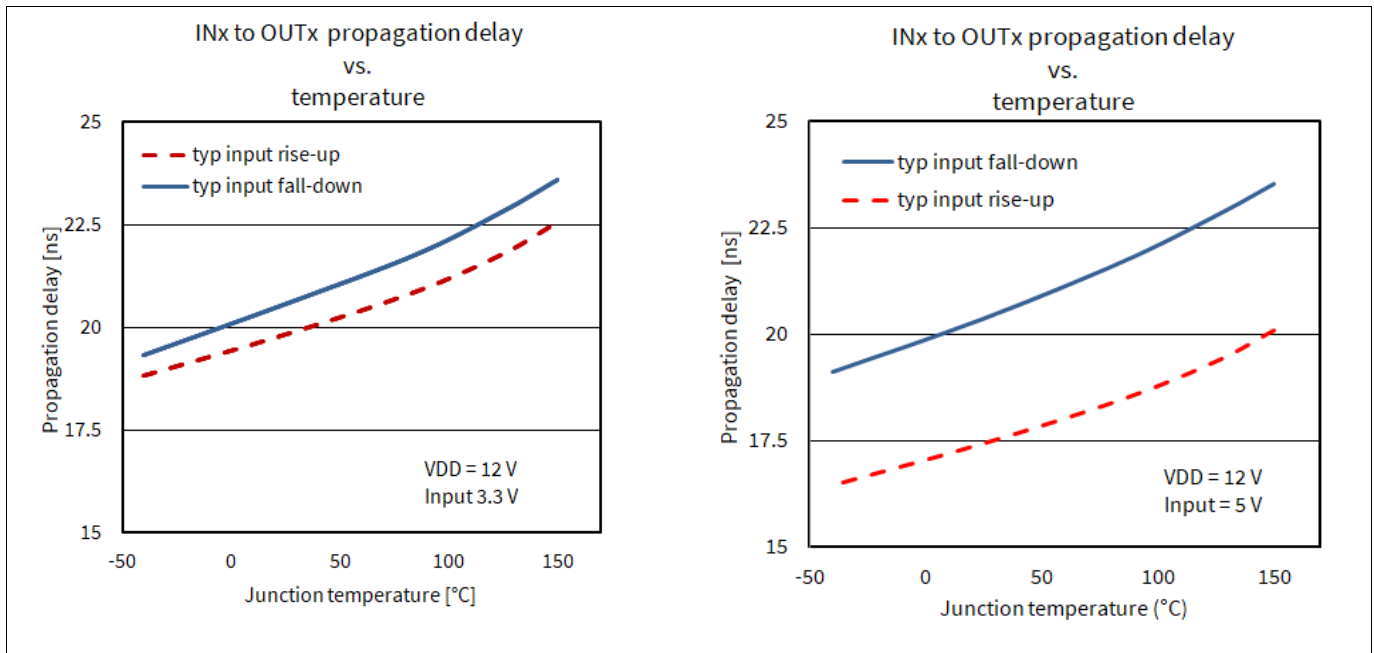


**Figure 15 Typical undervoltage lockout behavior vs. temperature for 2EDN8x (8 V)**

**Typical characteristics**

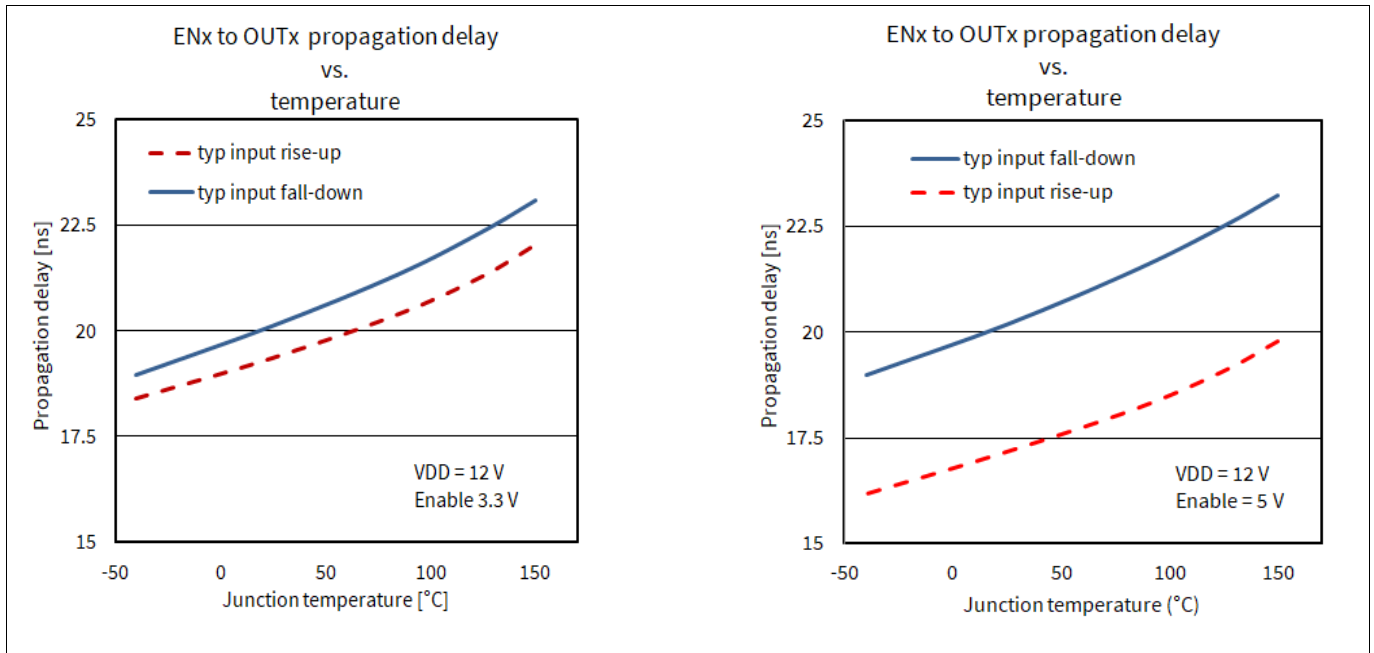


**Figure 16 Input characteristics (INx and ENx)**

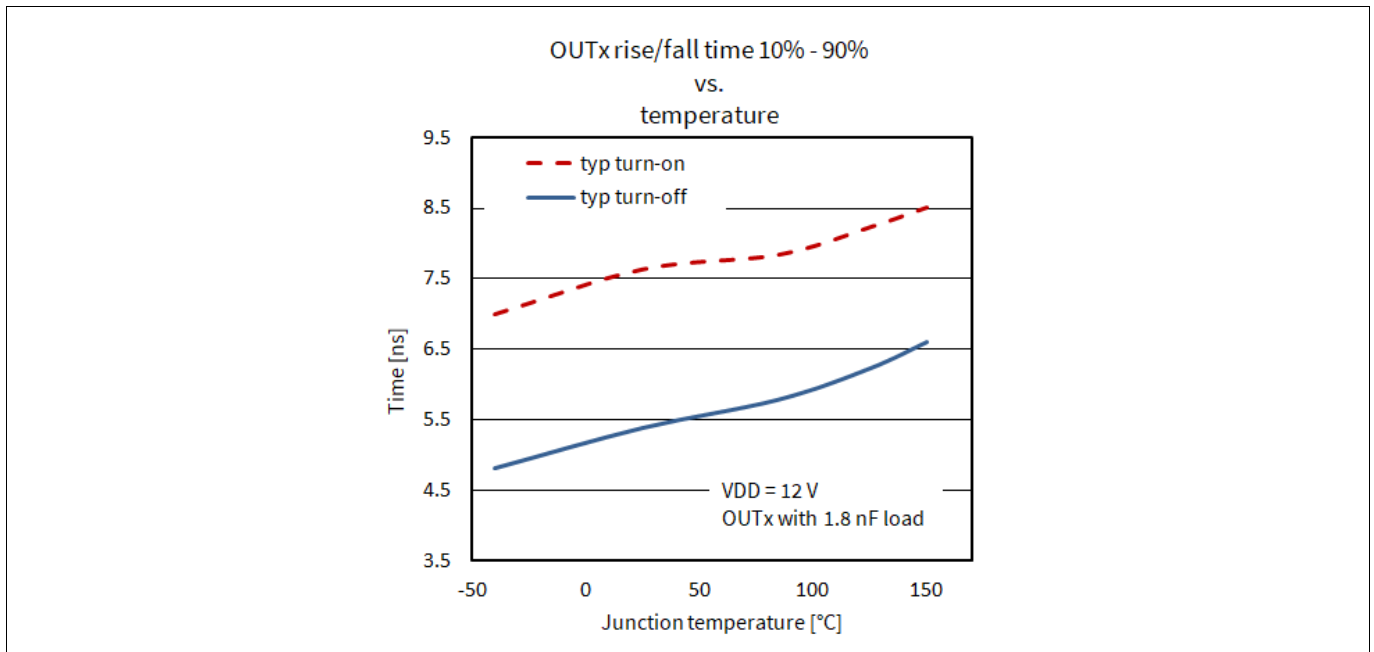


**Figure 17 Propagation delay (INx) on different input logic levels (see Figure 9)**

**Typical characteristics**

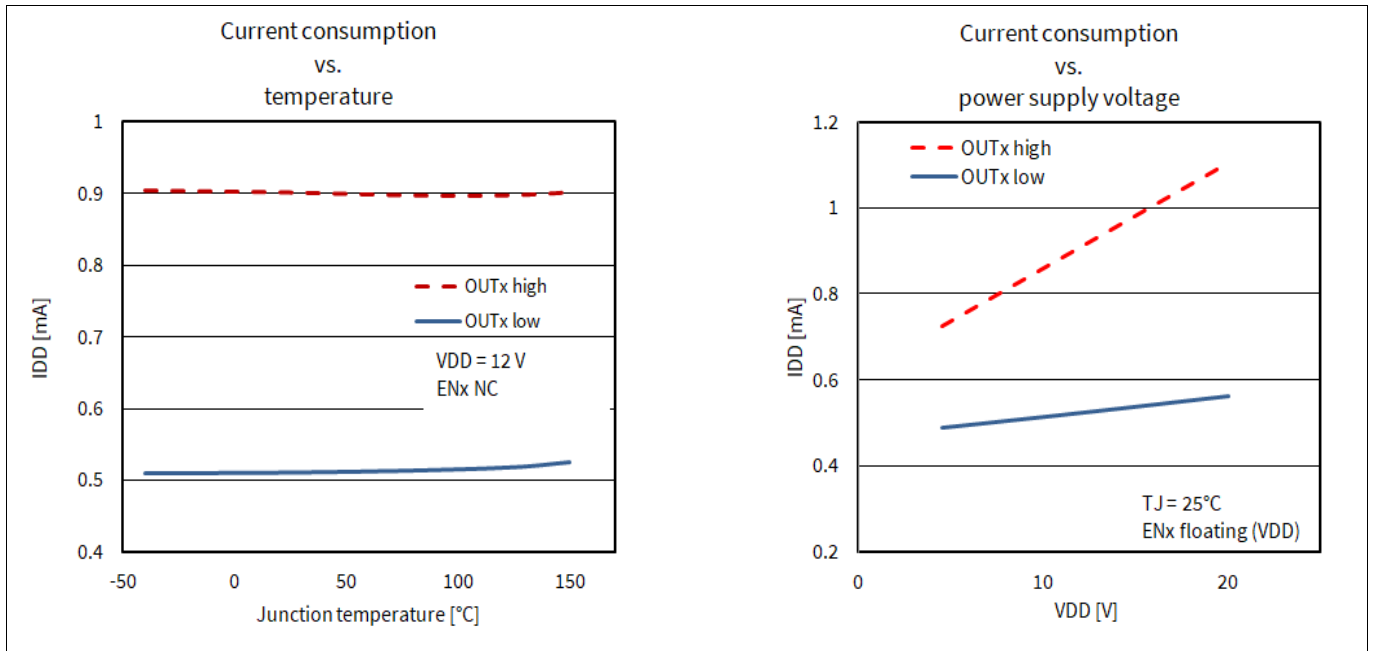


**Figure 18 Propagation delay (ENx) on different input logic levels (see Figure 10)**

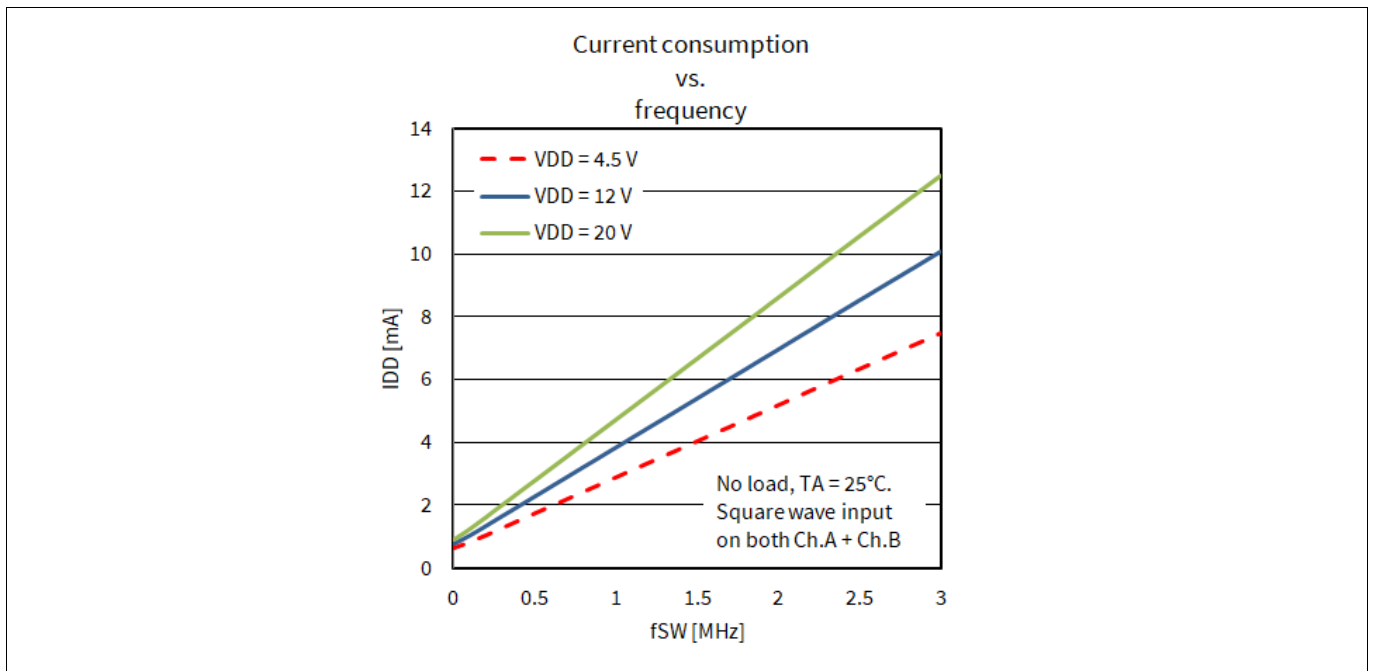


**Figure 19 Rise/fall times with load on output (see Figure 9)**

**Typical characteristics**



**Figure 20 Power consumption related to temperature and power supply**



**Figure 21 Current consumption versus frequency**

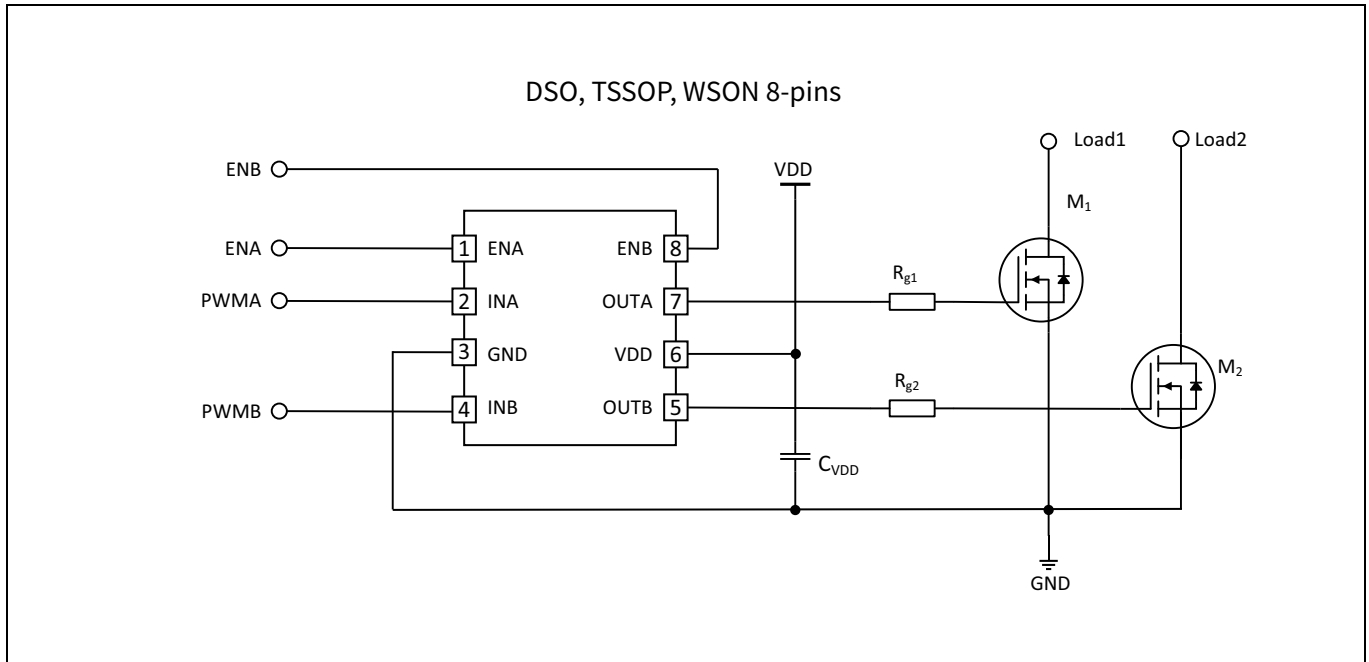


**Application and implementation**

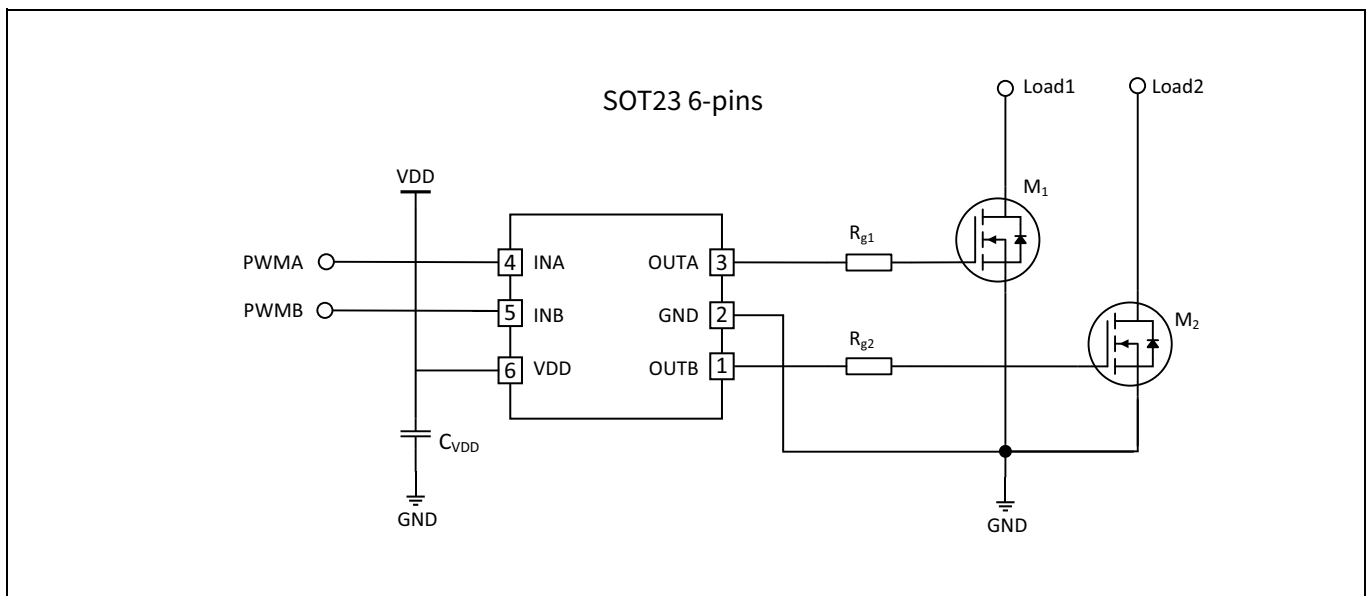
**8 Application and implementation**

*Note: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device*

**Figure 22** and **Figure 23** show typical applications for the 8-pin and 6-pin package versions respectively.



**Figure 22 Typical application for 8-pin packages**



**Figure 23 Typical application for 6-pin packages**

Package outlines

## 9 Package outlines

Note: For further information on package types, recommendation for board assembly, please go to: [Infineon packages](#).

### 9.1 Device numbers and markings

**Table 19 Product versions**

Part number	Orderable part number (OPN)	Device marking
2EDN7534F	2EDN7534FXTMA1	2N7534AF EiceDRIV XXHYWW
2EDN7434F	2EDN7434FXTMA1	2N7434AF EiceDRIV XXHYWW
2EDN7533F	2EDN7533FXTMA1	2N7533AF EiceDRIV XXHYWW
2EDN8534F	2EDN8534FXTMA1	2N8534AF EiceDRIV XXHYWW
2EDN8533F	2EDN8533FXTMA1	2N8533AF EiceDRIV XXHYWW
2EDN7534R	2EDN7534RXTMA1	2N7534 AR HYYWW
2EDN7434R	2EDN7434RXTMA1	2N7434 AR HYYWW
2EDN7533R	2EDN7533RXTMA1	2N7533 AR HYYWW
2EDN8534R	2EDN8534RXTMA1	2N8534 AR HYYWW
2EDN8533R	2EDN8533RXTMA1	2N8533 AR HYYWW
2EDN7534G	2EDN7534GXTMA1	2N7534 AG HYYWW
2EDN7534B	2EDN7534BXTSA1	YW <sup>1</sup> 754
2EDN7533B	2EDN7533BXTSA1	YW <sup>1</sup> 753

1) The date code digits "Y" and "W" in device marking for the SOT23-6 package are explained in [Table 20](#) and [Table 21](#)

**Package outlines**

**Table 20 Year date code marking - digit “Y”**

Year	Y	Year	Y	Year	Y
2000	0	2010	0	2020	0
2001	1	2011	1	2021	1
2002	2	2012	2	2022	2
2003	3	2013	3	2023	3
2004	4	2014	4	2024	4
2005	5	2015	5	2025	5
2006	6	2016	6	2026	6
2007	7	2017	7	2027	7
2008	8	2018	8	2028	8
2009	9	2019	9	2029	9

**Table 21 Week date code marking - digit “W”**

Week	W	Week	W	Week	W	Week	W	Week	W
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	-	-
10	K	21	Y	32	f	43	t	-	-
11	L	22	Z	33	g	44	u	-	-

Package outlines

9.2 PG-DSO-8

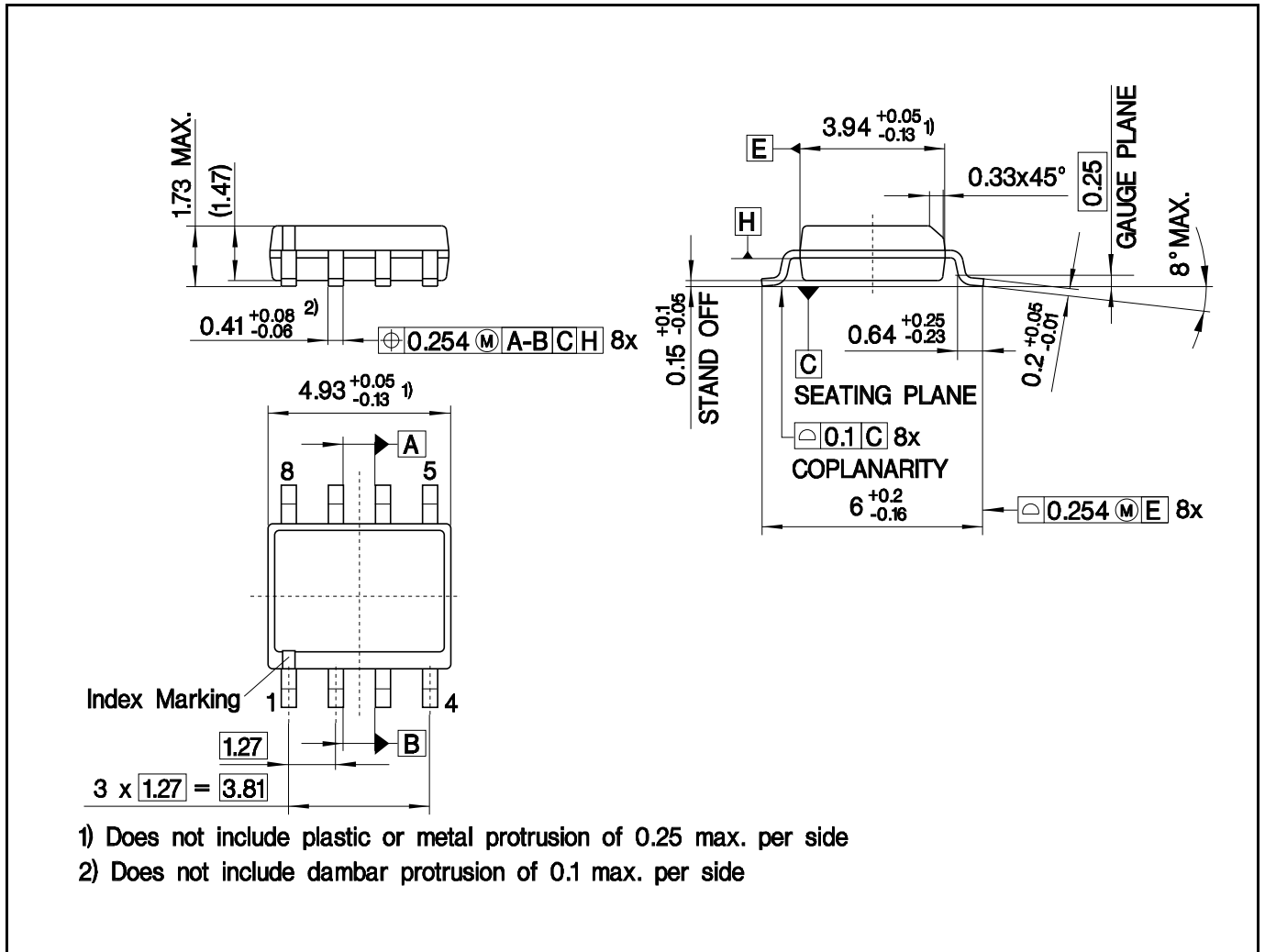


Figure 24 PG-DSO-8 outline

Package outlines

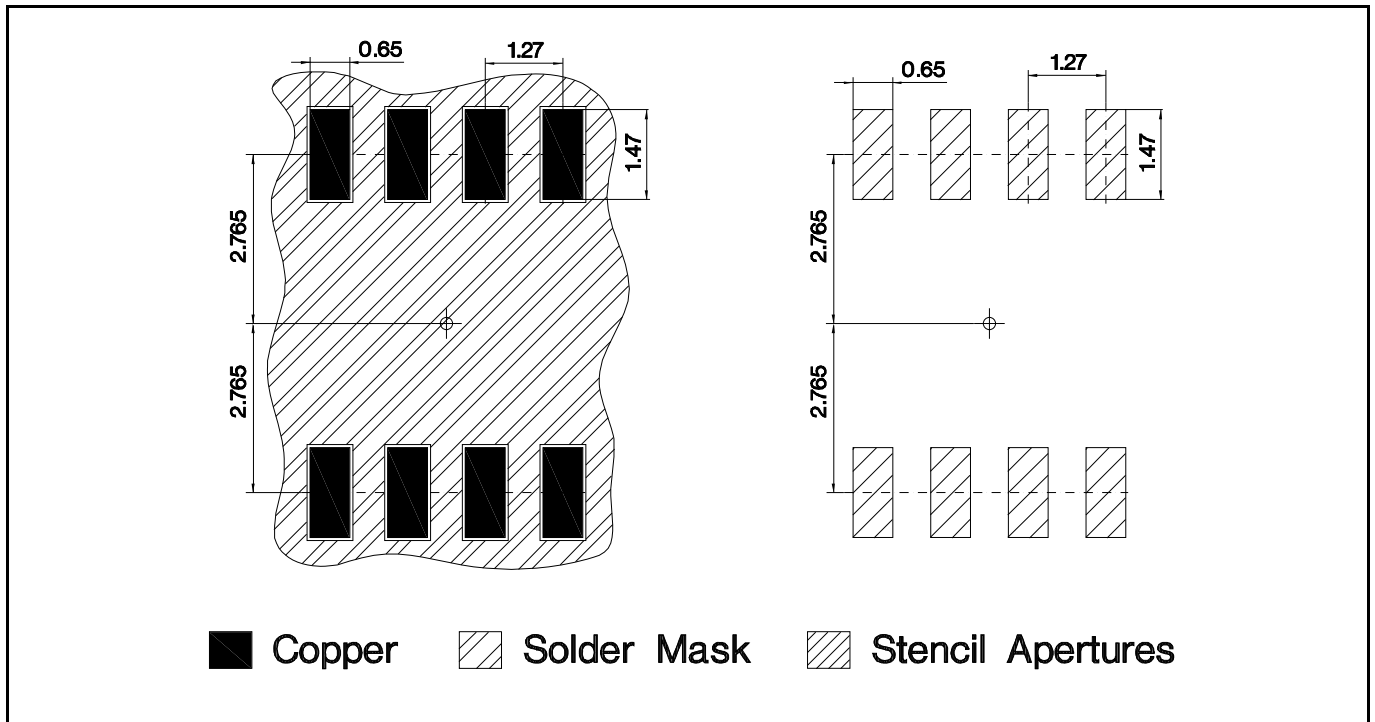


Figure 25 PG-DSO-8 footprint

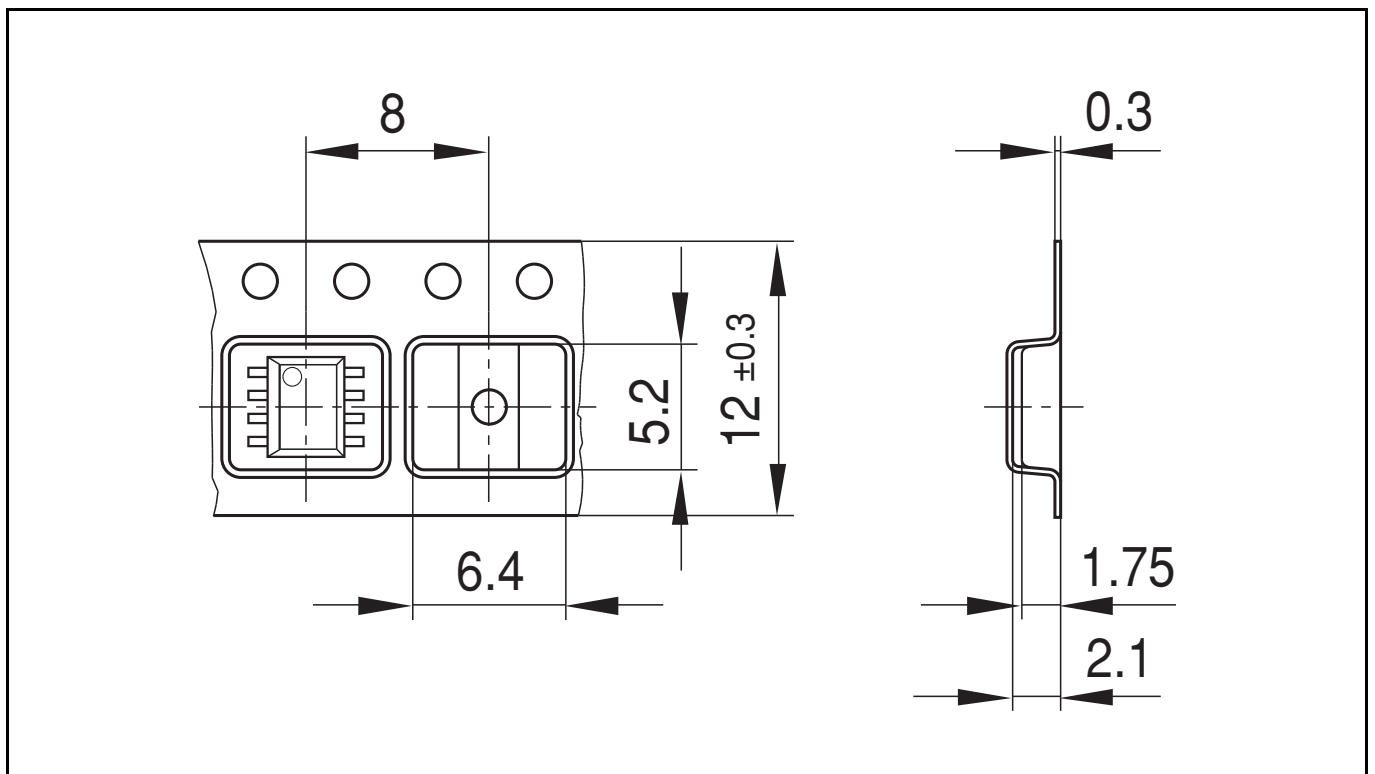


Figure 26 PG-DSO-8 packaging

Package outlines

9.3 PG-TSSOP-8

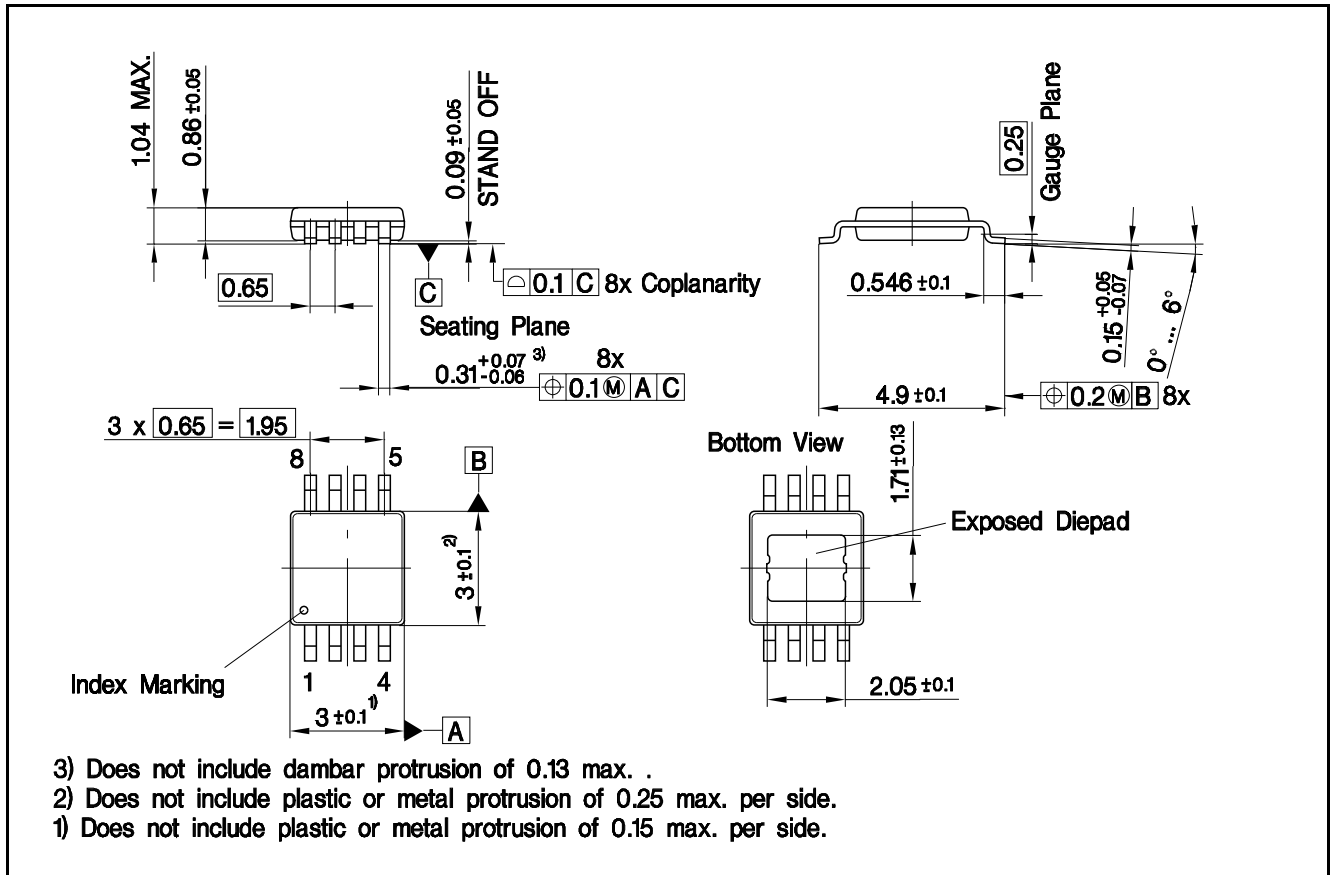


Figure 27 PG-TSSOP-8 outline

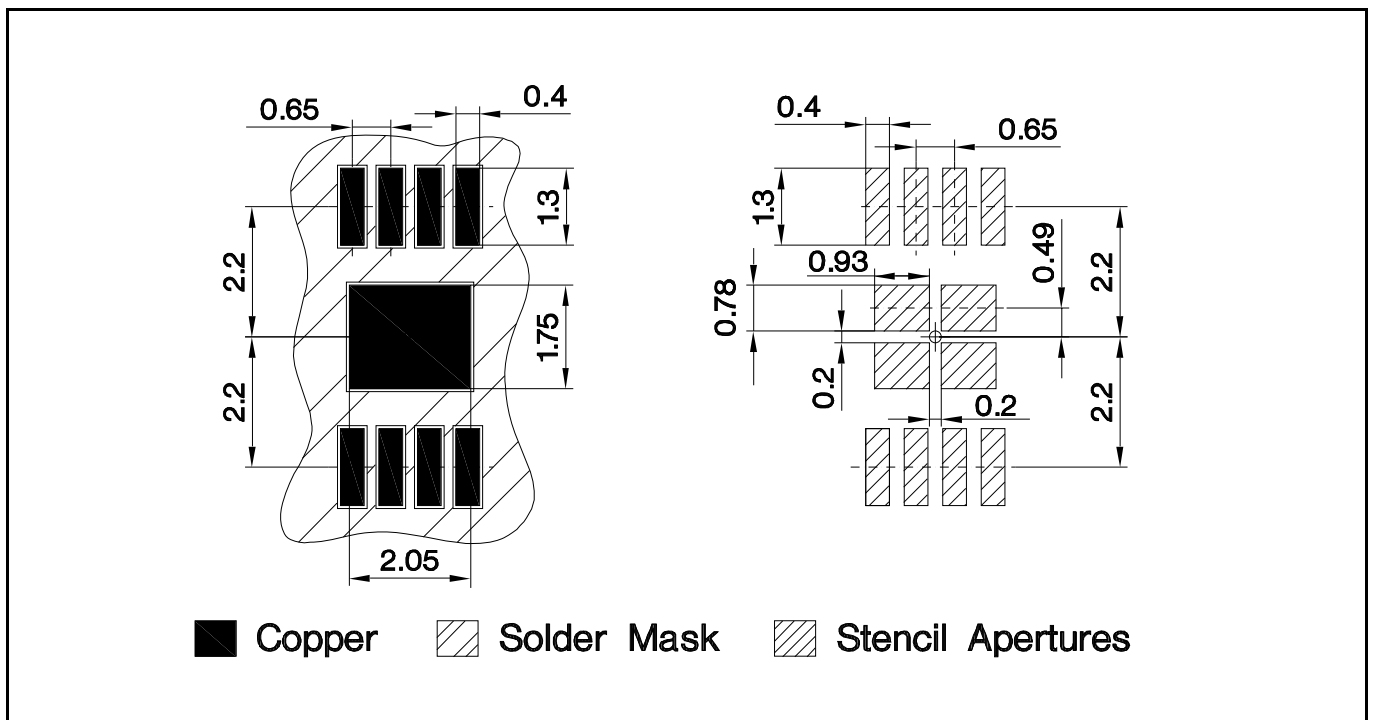


Figure 28 PG-TSSOP-8 footprint

Package outlines

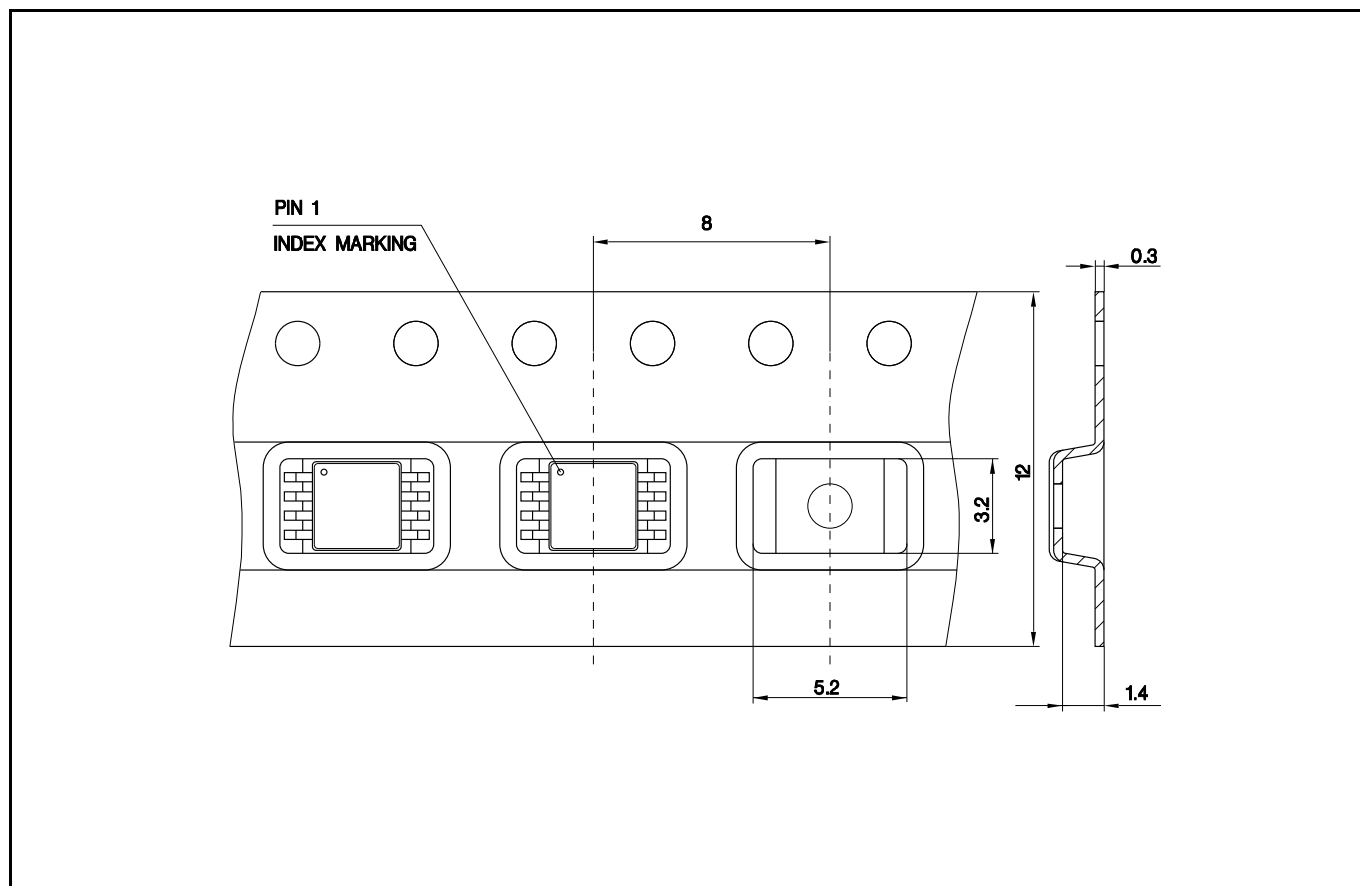
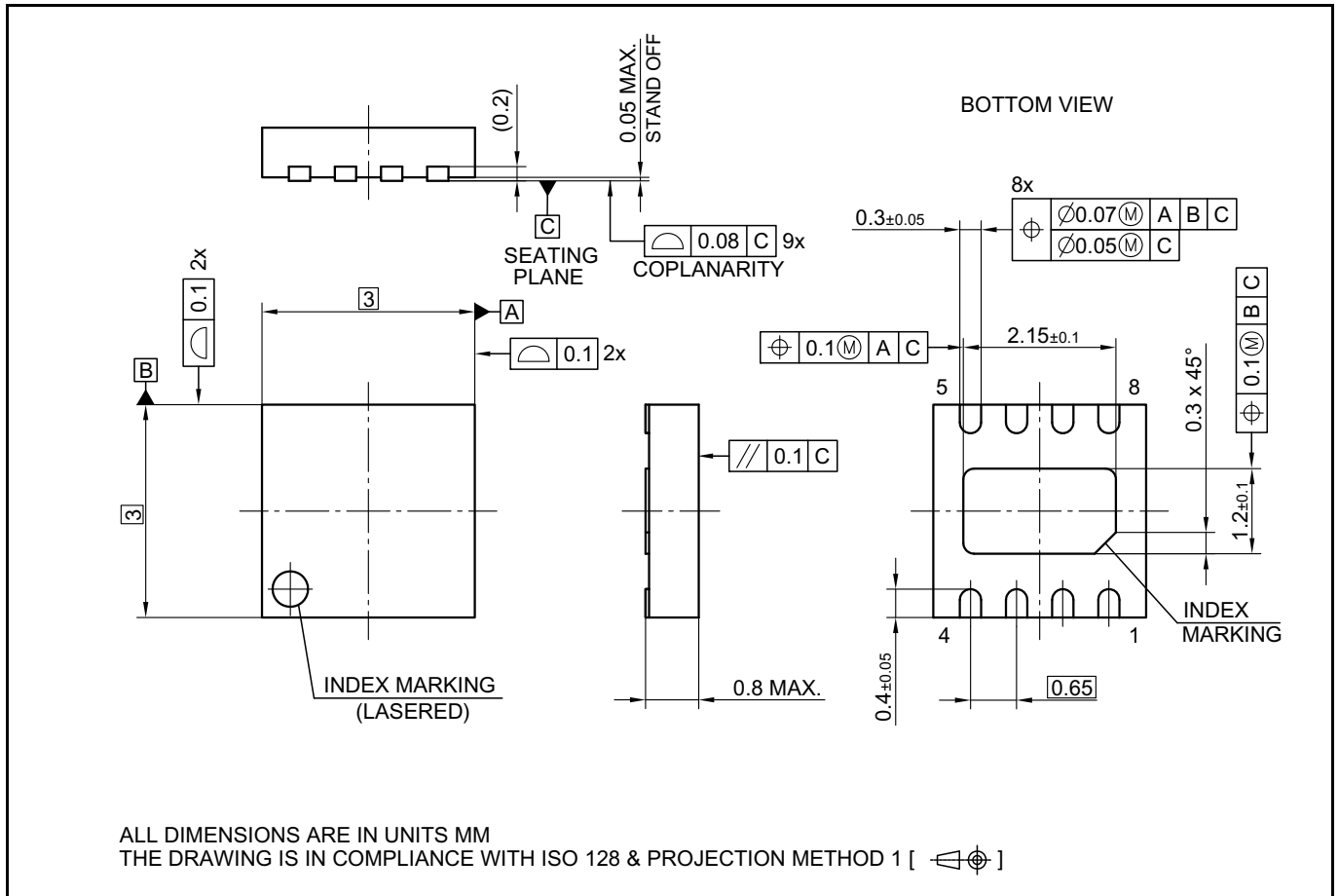


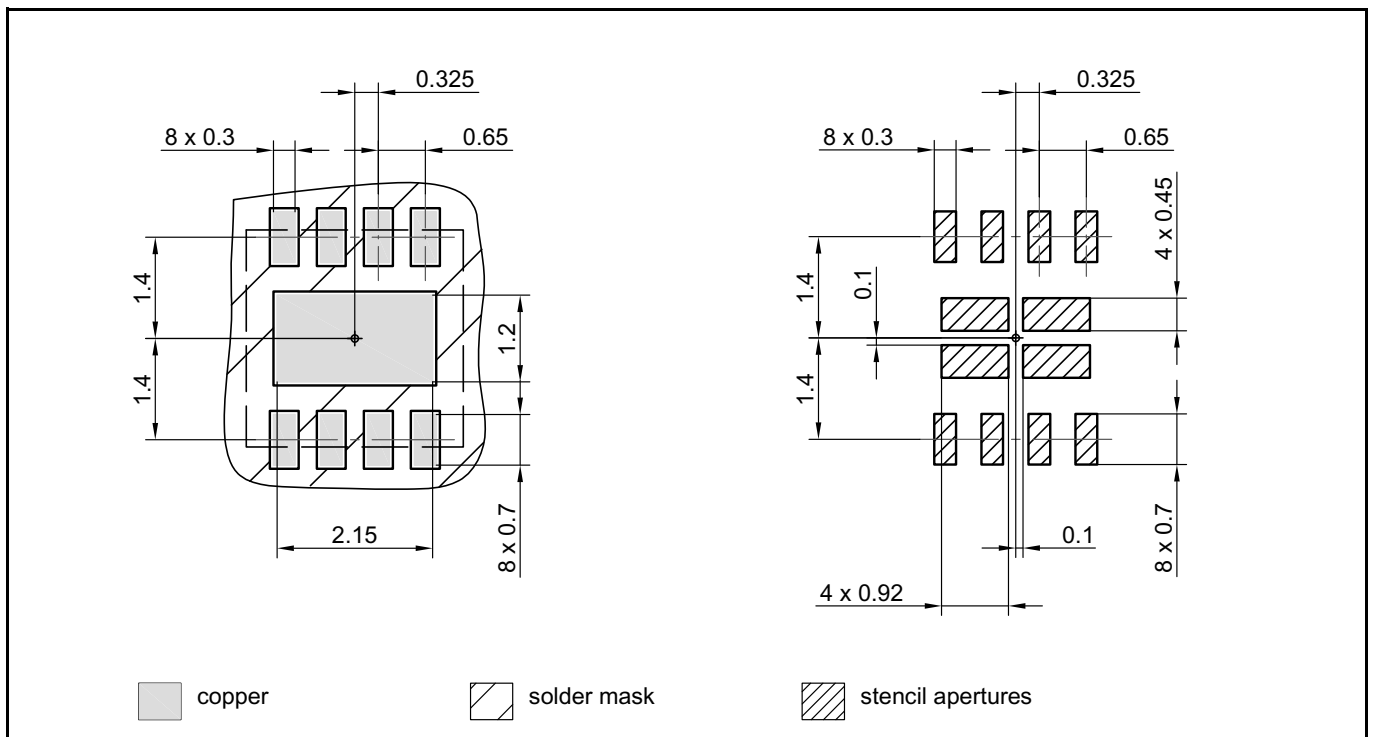
Figure 29 PG-TSSOP-8 packaging

**Package outlines**

**9.4 PG-WSO8-8**



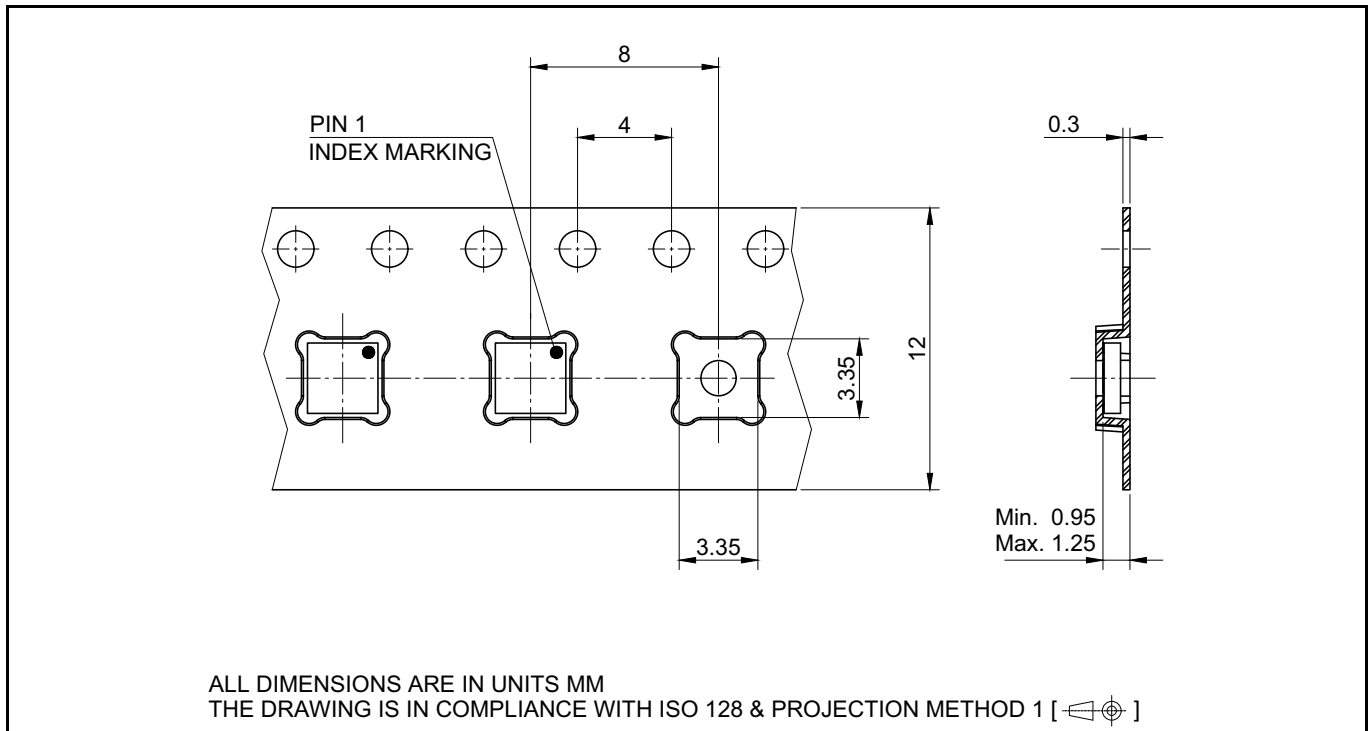
**Figure 30 PG-WSO8-8 outline**



**Figure 31 PG-WSO8-8 footprint**

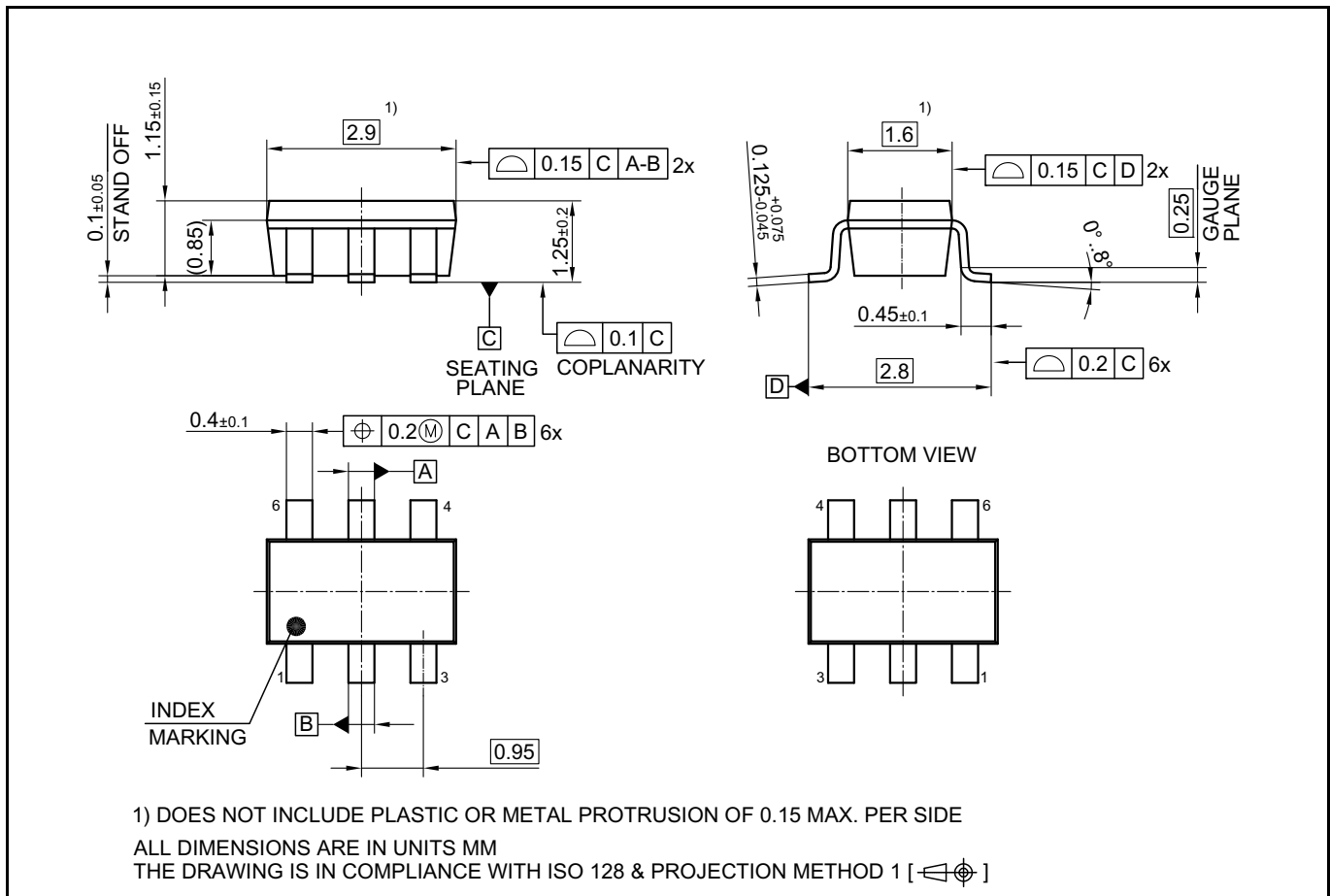


**Package outlines**



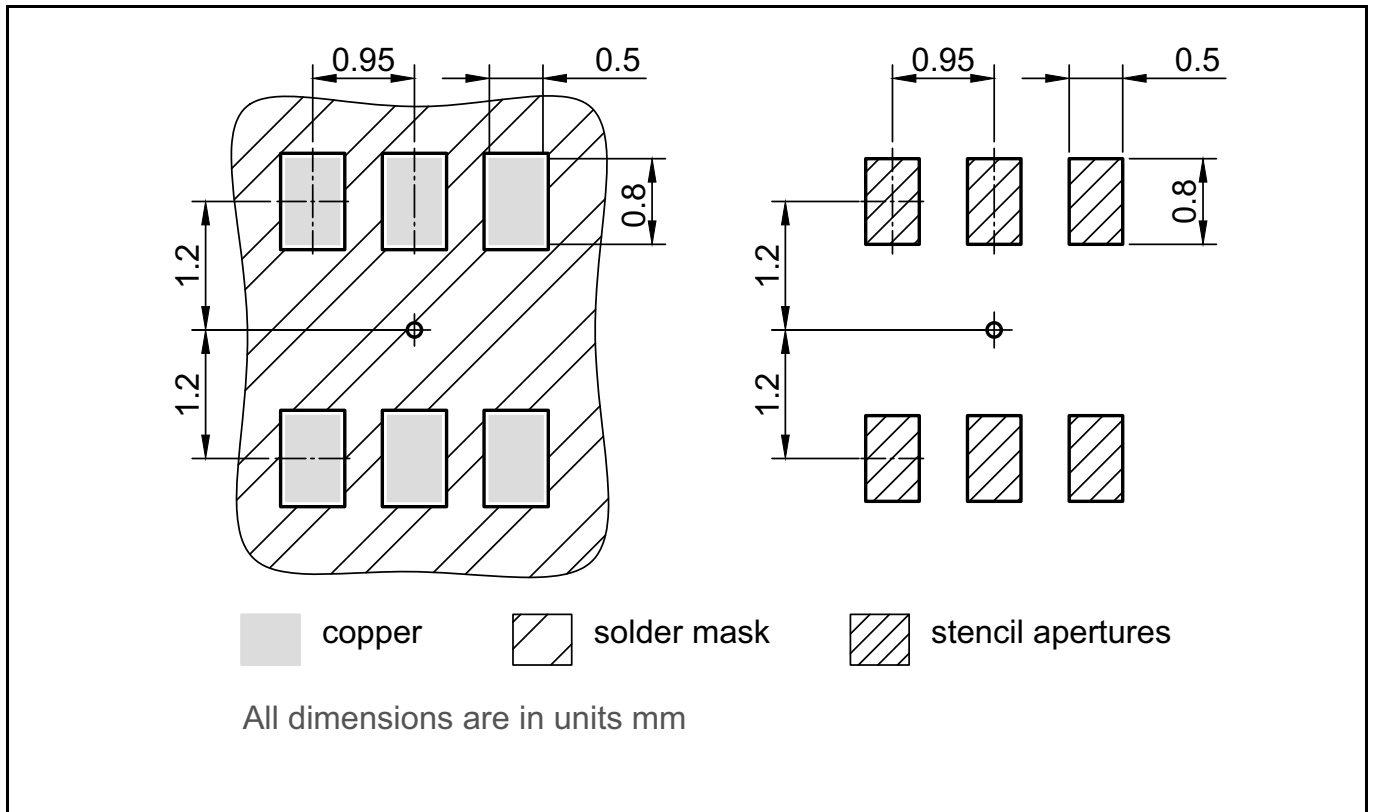
**Figure 32 PG-WSO8-8 packaging**

**9.5 PG-SOT23-6**

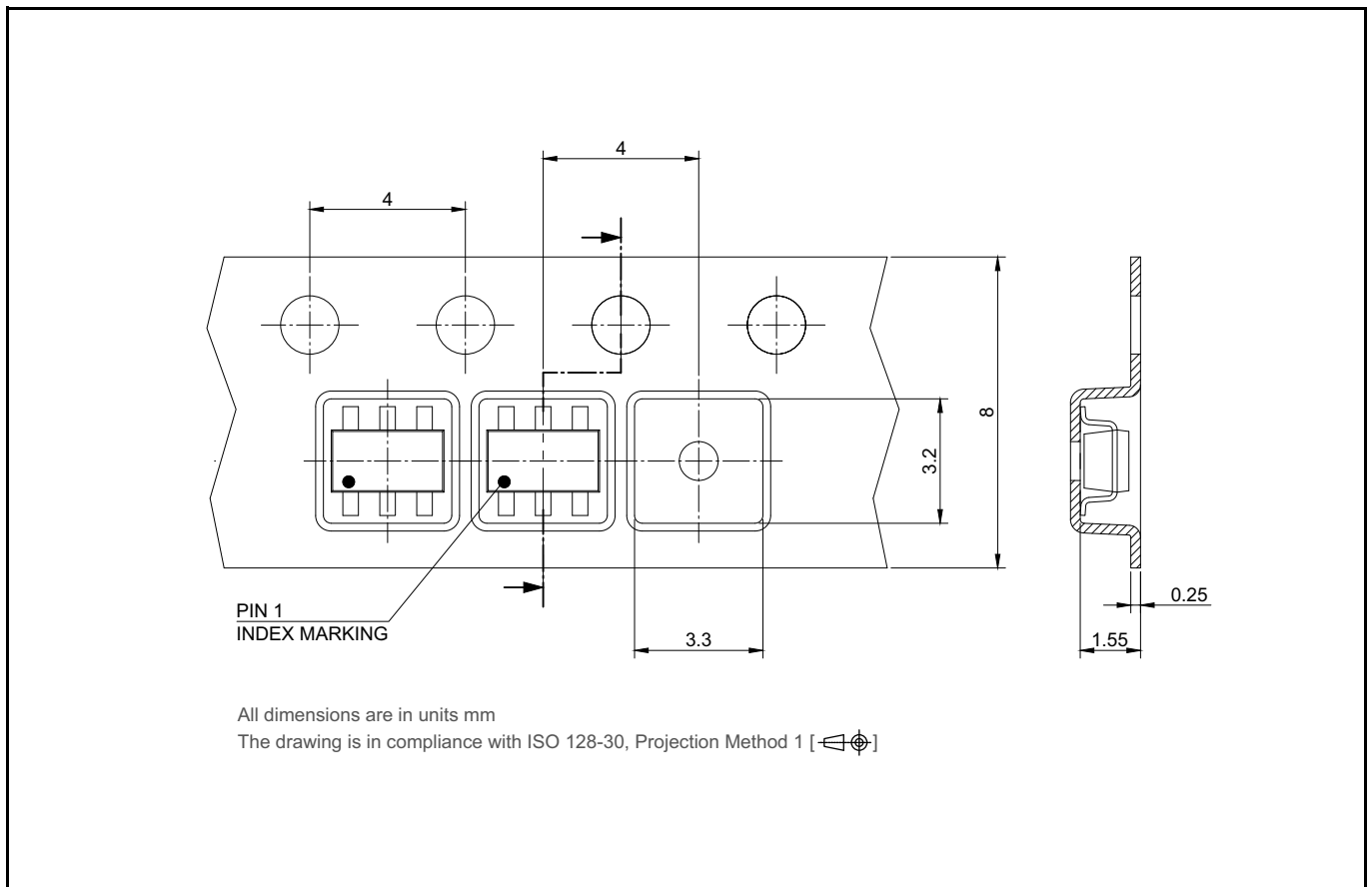


**Figure 33 PG-SOT23-6 outline**

**Package outlines**



**Figure 34 PG-SOT23-6 footprint**



**Figure 35 PG-SOT23-6 packaging**

**Revision history**

## **10 Revision history**

<b>Version</b>	<b>Date</b>	<b>Changes</b>
Rev.1.0	2021-10-29	Datasheet release

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**Document reference**

**EiceDRIVER™**

**2EDN753x/2EDN853x/2EDN743x**

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