CIP Hybrid Power Starter Kit

CIP Hybrid Power Starter Kit User's Guide

Preface

The Core Independent Peripheral (CIP) Hybrid Power Starter Kit is a hardware platform designed to demonstrate the flexibility of Microchip's CIP hybrid power microcontroller as used in a Switched Mode Power Supply (SMPS) application. The board incorporates the PIC16F1779 as the freely programmable Power Management IC (PMIC) device of a synchronous buck converter.

The synchronous buck converter on the board accepts input voltages ranging from 6V to 16V and delivers an output voltage of 3.3V with a maximum load current of 8A. The output of the power supply is rated for maximum 25W.

The CIP Hybrid Power Starter Kit supports three different control modes:

- Voltage Mode Control (VMC)
- Peak Current Mode Control (PCMC)
- Average Current Mode Control (ACMC) - the components are not populated by default

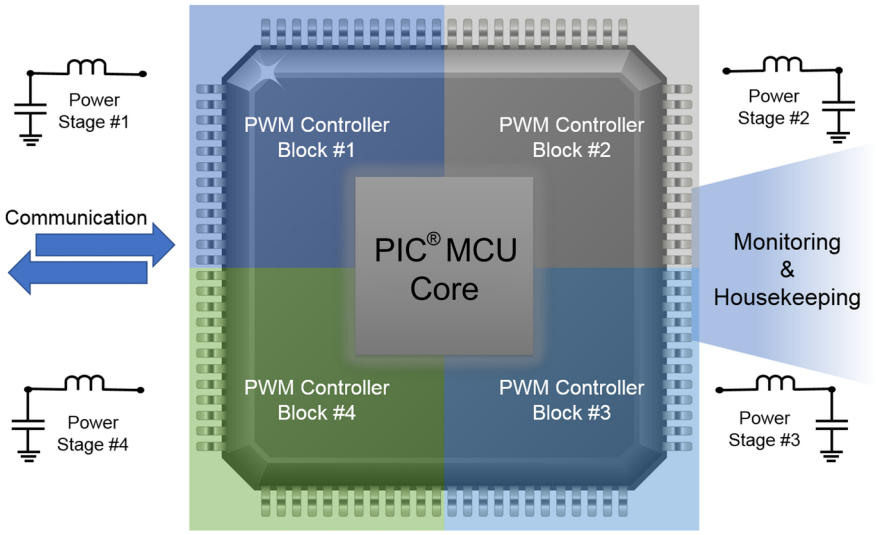
In addition, the synchronous buck converter plant has been equipped with three different current sensing options to allow users to experiment with different Pulse-Width Modulator (PWM) controller feedback configurations:

- Current Sense Transformer
- DC Resistance Sensing
- High-Side Shunt Amplifier - the component is not populated by default

The CIP Hybrid Power Starter Kit introduces the PIC16F1779 CIP hybrid power microcontroller. This device incorporates four digitally enhanced analog PWM controller function blocks into a low-power, 8-bit microcontroller architecture allowing users to tailor features and functions to application specific requirements. The PWM controller functional blocks are built in as CIPs, making MCU core activity independent from the PWM controller functional block operation.

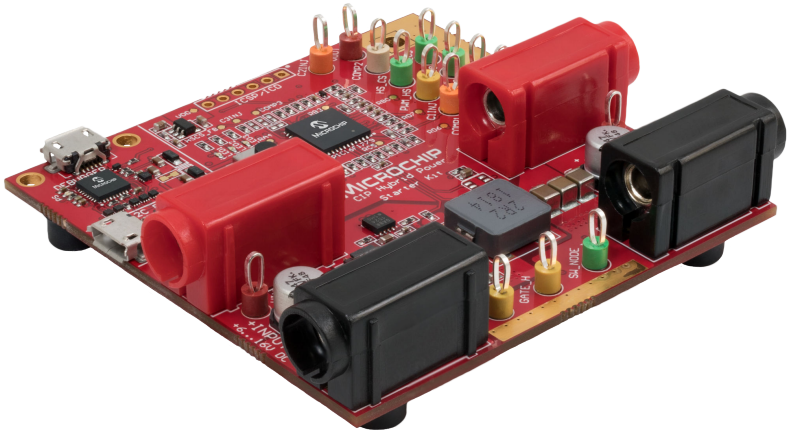
The PWM controller blocks can be configured at design time or during run time. This is useful for creating nonlinear operating profiles for applications such as programmable power supplies like USB Power delivery DC/DC converters, multi-loop control systems in battery chargers and LED drivers as well as intelligent PMIC devices for embedded systems supporting proprietary or standardized communication like PMBus™ protocols.

PIC16F1779 CIP Hybrid Power Microcontroller



The CIP Hybrid Power Starter Kit features an on-board debugger that provides access to a serial port interface (serial to USB bridge), which is a mass storage interface for easy 'drag and drop' programming. It allows configuration and full access to the PIC® microcontroller In-circuit Serial Programming (ICSP) for programming and debugging using the MPLAB® X Integrated Development Environment (IDE) without the need for further hardware development tools to start an evaluation and development process.

The CIP Hybrid Power Starter Kit comes preprogrammed and configured in PCMC utilizing the current sense transformer feedback option for demonstrating the functional operation of the synchronous buck converter. Further code examples and configurations are available for download from the CIP Hybrid Power Starter Kit product webpage.



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1.1 Features

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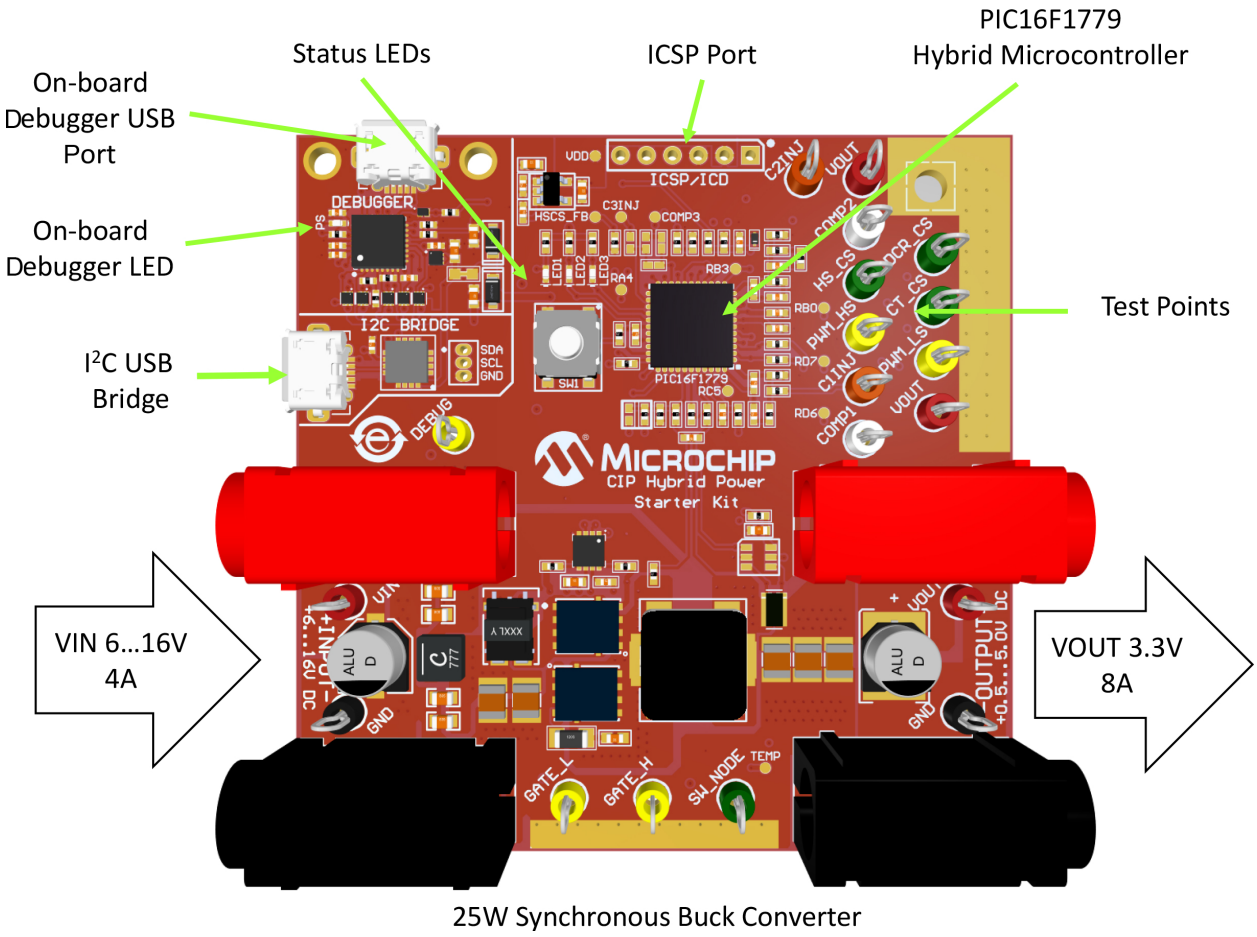
- One Power on LED and Two Status LEDs
- One Mechanical User Switch
- On-Board Debugger:
  - Board identification in MPLAB X IDE
  - One green power and status LED
  - Programming and debugging
  - Virtual COM port (CDC)
  - One logic analyzer channel (DGI GPIO)
- I^2C Bridge Support
- Nominal Operating Conditions:
  - Input voltage: +9V DC
  - Output voltage: +3.3V
  - Max. output current: 8A
  - Max. output power: 25W
- Absolute Maximum Ratings:
  - Input voltage: +6 to +16V DC
  - Output voltage: +0.5 to +5V
  - Output current: 8A
  - Output power: 30W
- Efficiency: 94.4% at 65% Load

1.2 Kit Overview

The CIP Hybrid Power Starter Kit is a hardware platform designed to demonstrate the flexibility of the PIC16F1779 hybrid microcontroller as a freely programmable power management device used on a synchronous buck converter.

Figure 1-1. CIP Hybrid Power Starter Kit Overview



1.2.1 Test Points

Measurements can be done through the available test points listed below.

Table 1-1. Test Points Labels

Test Point	Description
VIN	Input Voltage
VOUT	Output Voltage
GND	Ground
GATE_L	MOSFET Driver Low-side gate drive
GATE_H	MOSFET Driver High-side gate drive
SW_NODE	Switch node signal
COMP1	Type II compensator output for Current mode control
COMP2	Type III compensator output for Voltage mode control(1)
PWM_LS	PIC16F1779 Low-side PWM signal
PWM_HS	PIC16F1779 High-side PWM signal

.....continued	
Test Point	**Description**
C1INJ	BODE injection for Current mode control
C2INJ	BODE injection for Voltage mode control
CT_CS	Current transformer current sensing
DCR_CS	Inductor DC resistance current sensing(2)
HS_CS	High-side shunt current sensing
DEBUG	Microcontroller debug pin with 5 kHz frequency (100 us on/100 us off)(3)

Note:

1. Active only when used.
2. Active only when configured and enabled by software.
3. Active only when driven by software.

1.2.2 LED Indicators

The CIP Hybrid Power Starter Kit features four LEDs with the following functions. The green LED1 indicates that the board has enough power to provide proper 5V bias to the microcontroller. The red LED2 and blue LED3 are test LEDs that indicate the board is operating properly. The function of the LEDs can be modified and programmed by the user to give other status signals that are relevant to the board. By default, when the CIP Hybrid Power Starter Kit is functional, the blue LED3 flashes with 600 ms period (300 ms on, 300 ms off). The red LED2 is controlled by the pushbutton switch. LED2 lights up when the switch is pressed. The green PD LED shows the status of the board during programming.

Table 1-2. LED Indicators

LED Color	Label	System Element Monitored
Green	LED1	Board Power On Indicator
Red	LED2	Test Status(1)
Blue	LED3	Test Status(1)
Green	PS	On-board debugger Power/ Status

Note:

1. Must be enabled by software.

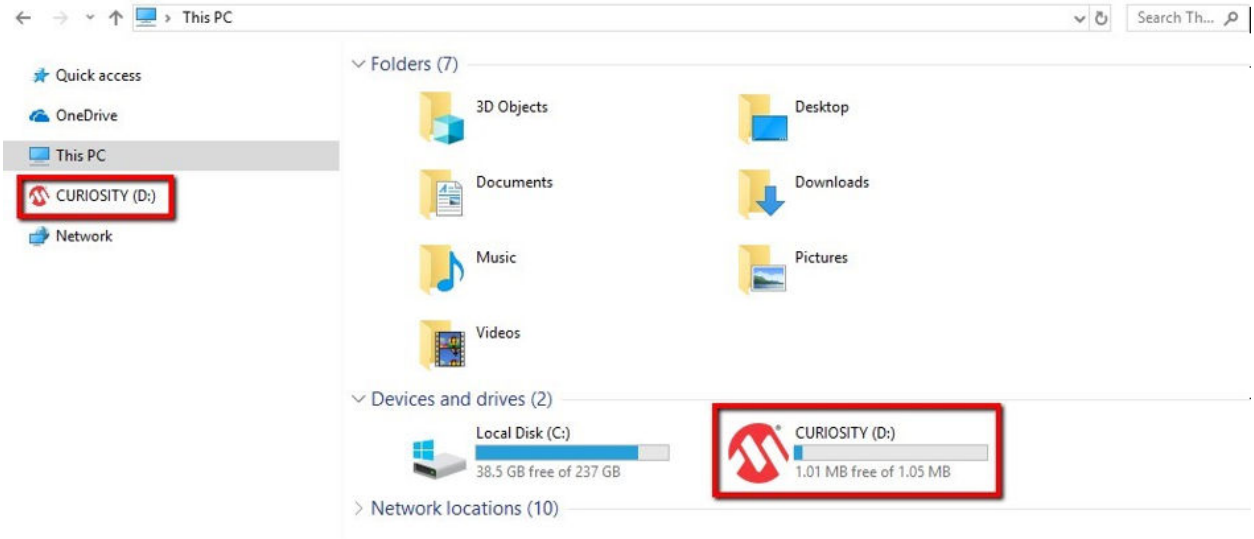
2. Getting Started

2.1 Connecting the Board to the PC

Connect the CIP Hybrid Power Starter Kit to the computer using a standard micro-USB cable. Once plugged in, the LED1 is ON, the LED3 is toggling and the PS is lit up, indicating that the board is receiving power from the USB. The board appears as a removable storage device on the host PC, as shown in the figure below. Double click the CURIOSITY drive to open it and get started.

Note: All procedures are the same for Windows®, Mac OS® and Linux® environments.

Figure 2-1. CIP Hybrid Power Starter Kit Board as Removable Storage



The CURIOSITY drive contains the following files:

- `AUTORUN.ICO` - icon file for the Microchip logo.
- `AUTORUN.INF` - system file required for Windows Explorer to show the icon file.
- `KIT-INFO.HTM` - redirects the user to a site containing information about the board.
- `KIT-INFO.TXT` - a text file with details about the board like the serial number.
- `STATUS.TXT` - a text file containing the status condition of the board.

Double click on the `KIT-INFO.HTM` file to access the CIP Hybrid Power Starter Kit webpage. On this page, the user can quickly see additional example codes to operate the board in other test modes: open loop and closed loop configurations.

2.2 The USB Programming Interface

While the CIP Hybrid Power Starter Kit comes out of the box fully programmed and provisioned, the user can still access the firmware through the USB interface. There are two methods to do it: through drag and drop, or through the on-board programmer/debugger using the MPLAB X IDE starting with version 5.10.

2.2.1 USB Mass Storage (Drag and Drop)

One way to program the device is to drag and drop a `.hex` file into the CURIOSITY drive. The XC8 compiler tool chain generates a `.hex` file for each project it builds. This `.hex` file contains the code of the

project. The USB debugger facilitates putting code into the board by having this drag and drop feature. This feature does not require any USB driver to be installed and works in all major operating system environments. Alternative application example `.hex` files for the board firmware will be available for download from the Downloads section at the bottom of the CIP Hybrid Power Starter Kit webpage.

2.2.2 USB Programmer/Debugger Interface

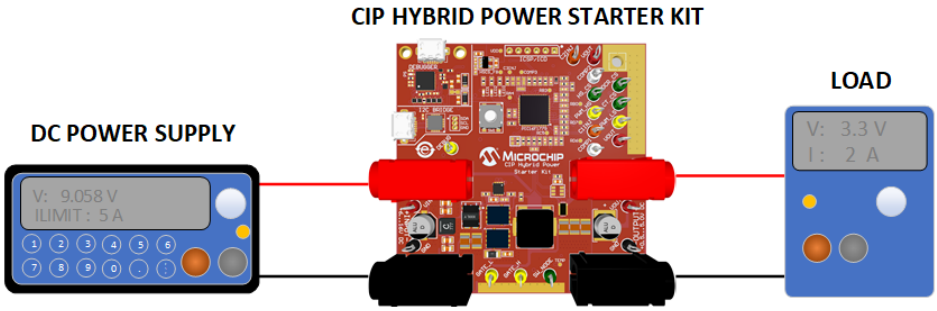
The PIC16F1779 microcontroller can also be programmed and debugged directly via the MPLAB X starting with version 5.10. The CIP Hybrid Power Starter Kit is automatically detected by the MPLAB X IDE, enabling full programming and debugging through the on-board debugger interface. The Xplained Window appears and provides relevant information about the CIP Hybrid Power Starter Kit.

2.3 Connecting the Board to the DC Power Supply and Load

The CIP Hybrid Power Starter Kit comes preprogrammed in the PCMC configuration. The kit can be quickly tested for output voltage regulation. The steps are as follows:

1. Connect a DC power supply to the input connector J1 and J2 (observe the polarity). Set the DC supply to 9V and current limit of 5A.
2. Attach an electronic load to the output connector J3 and J4 (observe the polarity). Set the electronic load to constant current of 2A.
3. Turn on the DC supply; the blue LED is flashing with an interval of 600 ms (300 ms on/300 ms off).
4. When the switch is pressed, the red LED turns on; when the switch is released, it turns off.
5. Measure voltage at output. A regulated VOUT of 3.3V is present.

Figure 2-2. Connecting Board to DC Power Supply and Load



2.4 Test Modes

The CIP Hybrid Power Starter Kit has four different test modes. These modes can be programmed to the microcontroller either through drag and drop programming or using the MPLAB X IDE.

Test Mode	Description
Open Loop	Runs the board in open loop using only PWM and COG peripherals
Open Loop with Current Limit	Runs the board in open loop using PWM, COG, CMP, PRG and FVR peripherals
Peak Current Mode Control (PCMC)	Runs the synchronous buck converter in PCMC closed loop
Voltage Mode Control (VMC)	Runs the synchronous buck converter in VMC closed loop

2.5 Design Documentation and Relevant Links

The following list contains links to the most relevant documents and software for the CIP Hybrid Power Starter Kit board. For users accessing the electronic version of this document, the underlined labels are clickable and will redirect to the appropriate website.

- MPLAB X IDE - a free IDE to develop applications for Microchip microcontrollers and digital signal controllers.
- MPLAB Code Configurator (MCC) - a free, graphical programming environment that generates seamless, easy-to-understand C code to be inserted into the project. Using an intuitive interface, it enables and configures a rich set of peripherals and functions specific to the application.
- MCC SMPS Library - an MCC plug-in that allows quick and easy configuration, and code generation for 8-bit PIC SMPS applications. This library contains a set of modules for generic fundamental SMPS building blocks and topologies. These support PIC device families designed for CIP Hybrid Power Controllers.
- MPLAB MINDI™ Analog Simulator - a comprehensive tool for circuit analysis consisting of the SIMPLIS/Simetrix environment and built-in Microchip component libraries for simulation.
- Microchip Sample Store - a Microchip sample store where samples of devices can be ordered.
- AN1978 SEPIC LED Driver Demo Board for Automotive Applications - a LED Driver design using PIC16F1769.
- AN2122 Flyback SMPS Using a Microcontroller as Control Unit - a Flyback Converter design using PIC16F1769.
- AN2455 Operational Amplifier PSpice® Model of 8-Bit PIC Microcontrollers - a comparative study of the actual PIC16F1769 internal operational amplifier with the PSpice model for simulation.
- AN2456 Configurability in a Switched Mode Power Supply Controller - describes the advantages and flexibility of a configurable SMPS microcontroller.
- AN1471 Efficiency Analysis of a Synchronous Buck Converter using Microsoft® Office® Excel®-Based Loss Calculator - provides designers of synchronous buck converters with a fast and accurate way to calculate system power losses, as well as overall system efficiency.
- TB3103 Buck Converter Using the PIC16F753 Analog Features - describes a synchronous buck power supply based on the PIC16F753 using 100% analog control for output regulation.
- TB3104 Boost Converter Using the PIC16F753 Analog Features - describes a boost power supply based on the PIC16F753 using 100% analog control for output regulation.
- TB3155 Multiphase Interleaved PWM Controller with Diode Emulation Using 8-Bit PIC Microcontrollers - outlines a method of realizing a multiphase PWM controller by configuring Microchip's 8-bit PIC microcontrollers.

3. On-Board Debugger

The CIP Hybrid Power Starter Kit contains an on-board debugger for programming and debugging. The on-board debugger is a composite USB device of several interfaces: a debugger, a mass storage device, a data gateway, and a Virtual COM port (CDC).

Together with Microchip MPLAB X, the on-board debugger interface can program and debug the PIC16F1779.

A Data Gateway Interface (DGI) is available for use with the logic analyzer channels for code instrumentation, to visualize the program flow. DGI GPIOs can be graphed using the Data Visualizer.

The Virtual COM port is connected to a UART on the PIC16F1779 and provides an easy way to communicate with the target application through terminal software.

The on-board debugger controls one Power and Status LED (marked PS) on the CIP Hybrid Power Starter Kit board. The table below shows how the LED is controlled in different operation modes.

Table 3-1. On-board Debugger LED Control

Operation Mode	Status LED
Boot Loader mode	LED blink at 1 Hz during power-up.
Power-up	LED is lit - constant.
Normal operation	LED is lit - constant.
Programming	Activity indicator; the LED flashes slowly during programming/debugging.
Fault	The LED flashes fast if a power fault is detected.
Sleep/Off	LED is off. The on-board debugger is either in Sleep mode or powered down. This can occur if the kit is externally powered.

3.1 Virtual COM Port

A general purpose bridge between a host PC and a target device.

3.1.1 Overview

The debugger implements a composite USB device that includes a standard Communications Device Class (CDC) interface, which appears on the host as a Virtual COM Port. The CDC can be used to stream arbitrary data in both directions between the host and the target: the characters sent from the host will appear in the UART form on the CDC TX pin, and the UART characters sent into the CDC RX pin will be sent back to the host.

On Windows machines, the CDC will enumerate as Curiosity Virtual COM Port and appear in the Ports section of the device manager. The COM port number is usually shown here.

Info: On older Windows systems, a USB driver is required for CDC. This driver is included in Atmel® Studio and MPLAB X installations.

On Linux machines, the CDC will enumerate and appear as `/dev/ttyACM#`.

On MAC machines, the CDC will enumerate and appear as `/dev/tty.usbmodem#`. Depending on which terminal program is used, it will appear in the available list of modems as `usbmodem#`.

3.1.2 Limitations

Not all UART features are implemented in the debugger CDC. The constraints are outlined here:

- **Baud rate** must be in the range 1200 bps to 500 kbps. Values outside this range will be capped to these values, without warning. Baud rate can be changed on-the-fly.
- **Character format**: only 8-bit characters are supported.
- **Parity**: can be odd, even, or none.
- **Hardware flow control**: not supported.
- **Stop bits**: one or two bits are supported.

3.1.3 Signaling

During the USB enumeration, the host OS will start both communication and data pipes of the CDC interface. At this point, it is possible to set and read back the baud rate and other UART parameters of the CDC, but data sending and receiving will not be enabled.

When a terminal connects on the host, it must assert the DTR signal. This is a virtual control signal that is implemented on the USB interface, but not in hardware on the debugger. Asserting DTR from the host will indicate to the debugger that a CDC session is active, will enable its level shifters (if available), and will start the CDC data send and receive mechanisms.

Deasserting the DTR signal will not disable the level shifters, but it will disable the receiver, so no further data will be streamed to the host. Data packets that are already queued up for sending to the target will continue to be sent out, but no further data will be accepted.

3.1.4 Advanced Use

CDC Override Mode

In normal operation, the on-board debugger is a true UART bridge between the host and the device. However, under certain use cases, the debugger can override the Basic Operating mode and use the CDC pins for other purposes.

Dropping a text file (with extension `.txt`) into the debugger's mass storage drive can be used to send characters out of the CDC TX pin. The text file must start with the characters:

```
CMD:SEND_UART=
```

The maximum message length is 50 characters - all remaining data in the frame are ignored.

The default baud rate used in this mode is 9600 bps, but if the CDC is already active or has been configured, the baud rate last used still applies.

USB-Level Framing Considerations

Sending data from the host to the CDC can be done byte-wise or in blocks, which will be chunked into 64-byte USB frames. Each such frame will be queued up for sending to the CDC TX pin. Sending a small amount of data per frame can be inefficient, particularly at low baud rates, since the debugger buffers frames, not bytes. A maximum of 4 x 64-byte frames can be active at any time, the debugger will throttle the incoming frames accordingly. Sending full 64-byte frames containing data is the most efficient.

When **receiving data** from the target, the debugger will queue up the incoming bytes into 64-byte frames, which are sent to the USB queue for transmission to the host when they are full. Incomplete frames are also pushed to the USB queue at approximately 100 ms intervals, triggered by USB start-of-frame tokens. Up to 8 x 64-byte frames can be active at any time.

If the host, or the software running on it, fails to receive data fast enough, an overrun will occur. When this happens, the last-filled buffer frame will be recycled instead of being sent to the USB queue, and a full frame of data will be lost. To prevent this occurrence, the user must ensure that the CDC data pipe is being read continuously, or the incoming data rate must be reduced.

3.2 Mass Storage Disk

A simple way to program the target device is through drag and drop with `.hex` files.

3.2.1 Mass Storage Device

The debugger implements a highly optimized variant of the FAT12 file system that has a number of limitations, partly due to the nature of FAT12 itself, and partly due to optimizations made to fulfill its purpose in this development kit.

The CURIOSITY drive is USB Chapter 9 compliant as a mass storage device, but does not in any way fulfill the expectations of a general purpose mass storage device. This behavior is intentional.

The debugger enumerates as a Curiosity Nano USB device that can be found in the disk drives section of the Windows device manager. The CURIOSITY drive appears in the file manager and claims the next available drive letter in the system.

The CURIOSITY drive contains approximately one MB of free space. This does not reflect the size of the target device's Flash in any way. When programming a `.hex` file, the binary data are encoded in ASCII with metadata providing a large overhead, so one MB is a trivially chosen value for disk size.

It is not possible to format the CURIOSITY drive. When programming a file to the target, the filename may appear in the disk directory listing - this is merely the operating system's view of the directory, which, in reality, has not been updated. It is not possible to read out the file contents. Removing and replugging the kit will return the file system to its original state, but the target will still contain the application that has been previously programmed.

To erase the target device, simply copy a text file starting with "CMD:ERASE" onto the disk.

By default, the CURIOSITY drive contains several read-only files for generating icons as well as reporting status and linking to further information:

- `AUTORUN.ICO` - icon file for the Microchip logo.
- `AUTORUN.INF` - system file required for Windows Explorer to show the icon file.
- `KIT-INFO.HTM` - redirect to the development board website.
- `KIT-INFO.TXT` - a text file containing details about the kit firmware, name, serial number and device.
- `STATUS.TXT` - a text file containing the programming status of the board.

Info: When `STATUS.TXT` is updated by the debugger dynamically, the contents may be cached by the OS and not reflect the correct status.

3.2.2 Configuration Words/Fuse Bytes

Configuration Words (PIC® MCU Targets)
Configuration Word settings included in the project being programmed after program Flash is programmed. The debugger will *not* mask out any bits in the Configuration Words when writing them, but since it uses Low-Voltage Programming mode, it is unable to clear the LVP Configuration bit. If the incorrect clock source is selected, for example, and the board does not boot, it is always possible to perform a bulk erase (always done before programming) and restore the device to its default settings.

3.3 On-Board Debugger Implementation

The CIP Hybrid Power Starter Kit implementation of the on-board debugger and the connections to the PIC16F1779 device are shown in the table below.

Table 3-2. Debugger Connections

Debugger Pin	PIC16F1779 Pin	Function	Shared Functionality
DBG0	RB7	ICSP Data	-
DBG1	RB6	ICSP Clock	-
DBG2	RA6	DGI GPIO0	Debug test point(1)
DBG3	RE3	MCLR	-
CDC TX	RB4	UART RX	-
CDC RX	RB5	UART TX	-

Note:

1. Driven by user firmware.

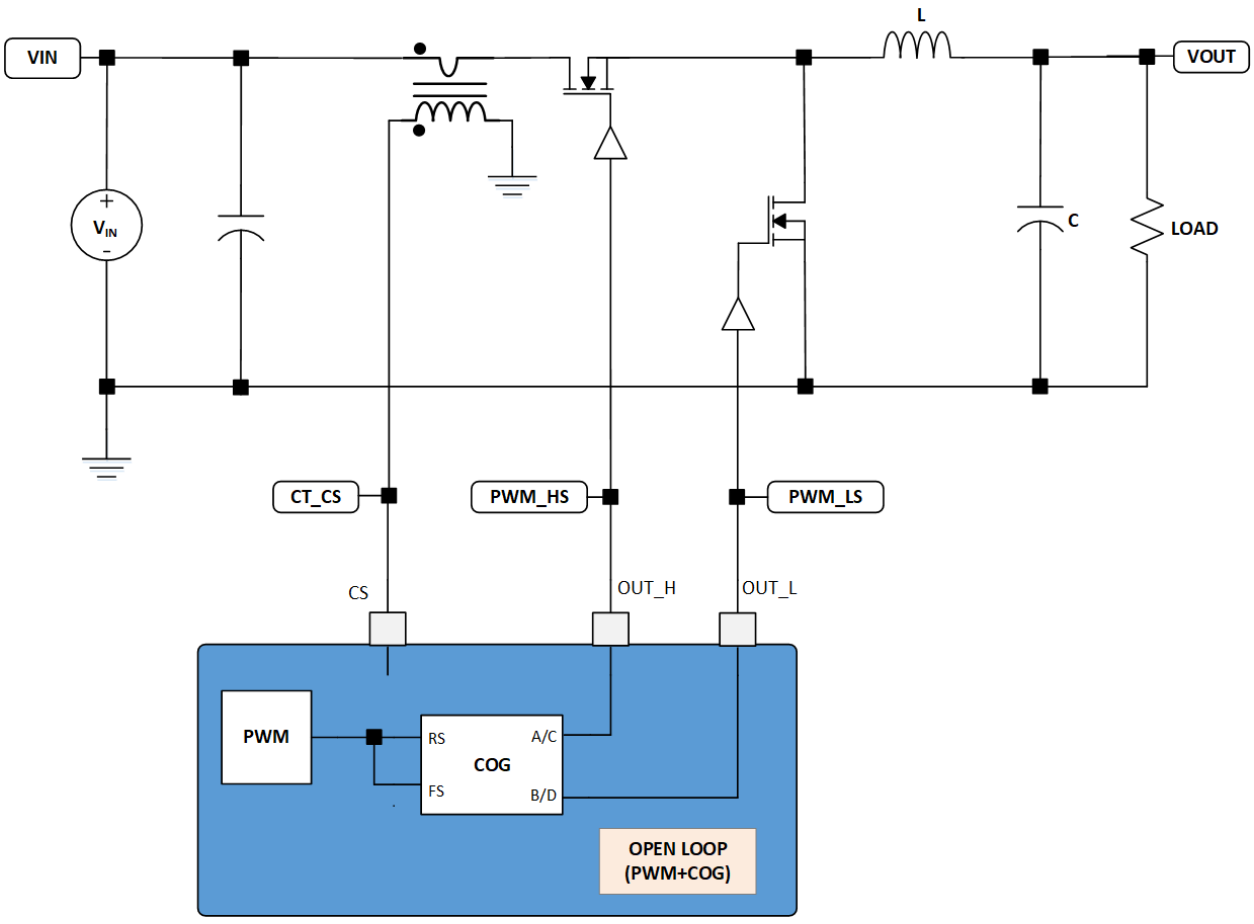
4. Test Modes Operation

The CIP Hybrid Power microcontroller is highly configurable and programmable to allow four different modes on the synchronous buck power train. The project files and codes for the different test modes can be found on the CIP Hybrid Power Starter kit landing page. The desired mode of operation can be downloaded to the board directly through drag and drop programming of the `.hex` file found in the project folder location. Alternatively, MPLAB X IDE and MCC SMPS Library can be used to program and configure the CIP Hybrid Power microcontroller to the desired test mode. Install the latest stable release of the MCC SMPS Library on MCC prior to performing these configurations. The MCC SMPS Library User's Guide explains in detail on how to configure the peripherals.

4.1 Open Loop (PWM+COG) Mode

This configuration enables the digital PWM module and complementary output control with dead times. The PWM outputs of PIC16F1779 produce a fixed switching frequency of 500 kHz with a fixed duty ratio of ~20%. The signal is fed to the rising and falling source of the Complementary Output Generator (COG) which produces the complementary PWM signals for driving the high-side and low-side switches. The Open Loop mode is very useful during the hardware validation of the power converters to analyze operation and signal integrity under stable conditions. The figure below shows the block diagram of the open loop configuration.

Figure 4-1. Open Loop Configuration

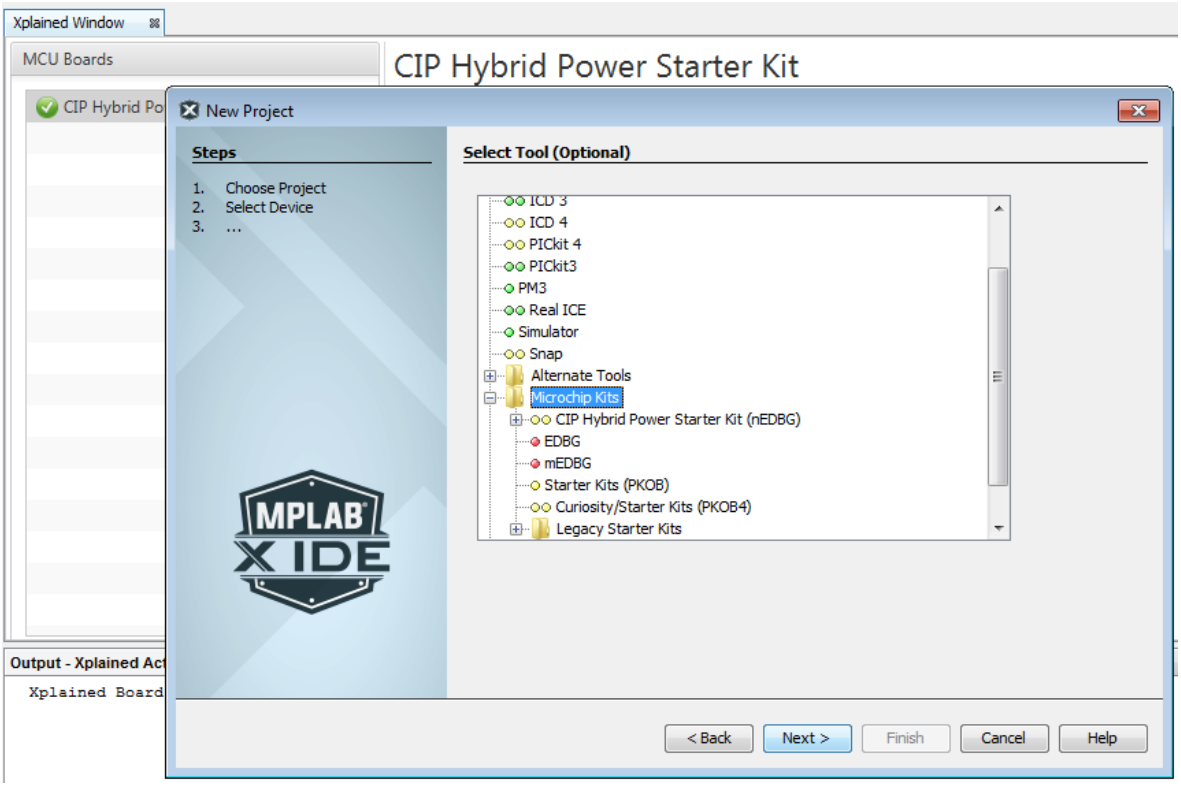


4.1.1 MCC SMPS Library Configuration for Open Loop

The following instructions show how to setup the peripherals of the CIP Hybrid Power Starter Kit to be able to operate in Open Loop test mode.

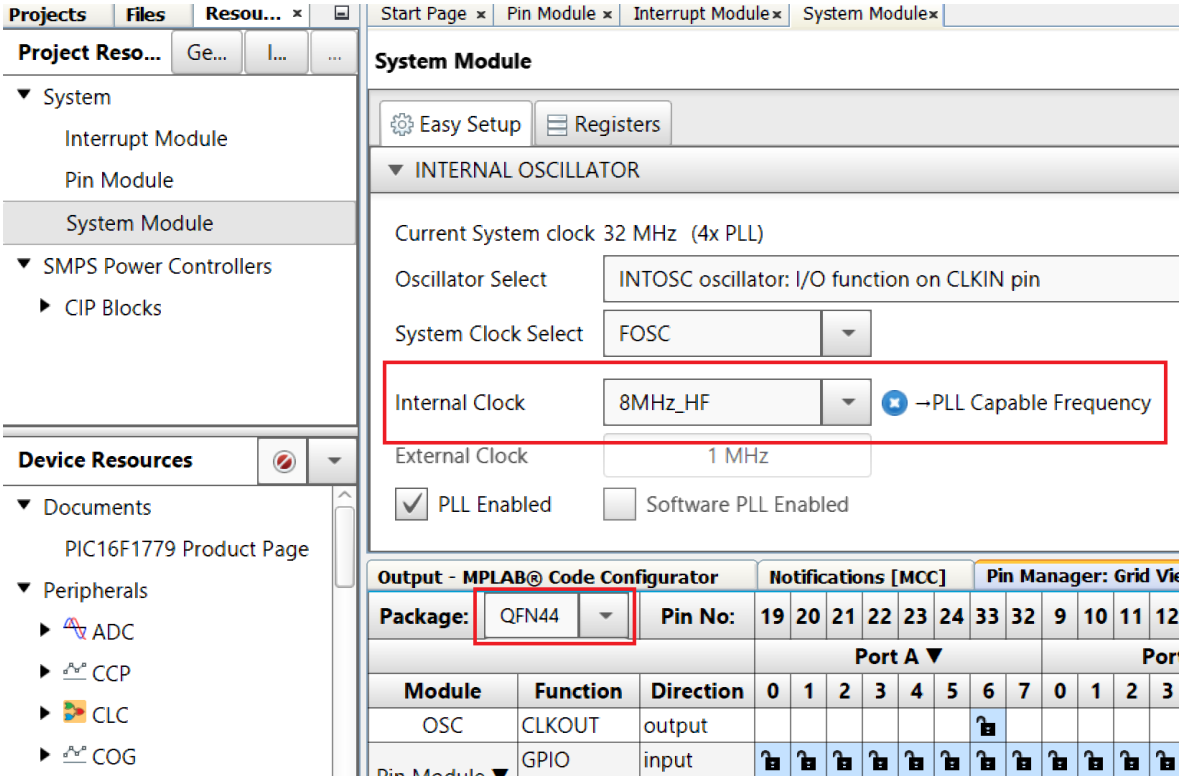
1. Open MPLAB X. Connect the CIP Hybrid Power Starter Kit to the computer through an on-board debugger USB port using a conventional micro-USB cable. MPLAB X will detect the CIP Hybrid Power Starter Kit and an Xplained Window appears that provides relevant information about the board.
2. Create new Standalone Project in MPLAB X. Select the PIC16F1779 device. Select the CIP Hybrid Starter Kit as programming tool. Name this project “OpenLoop”.

Figure 4-2. Creating New MPLAB X Standalone Embedded Project



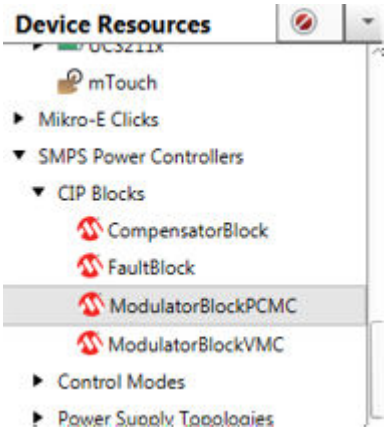
3. Open MCC. Save the MCC configuration as `OpenLoop.mc3`.
4. Change the internal oscillator clock to 8 MHz from the System Module in the Project Resources area. On the Pin Manager, change the package to QFN44.

Figure 4-3. System Module Settings



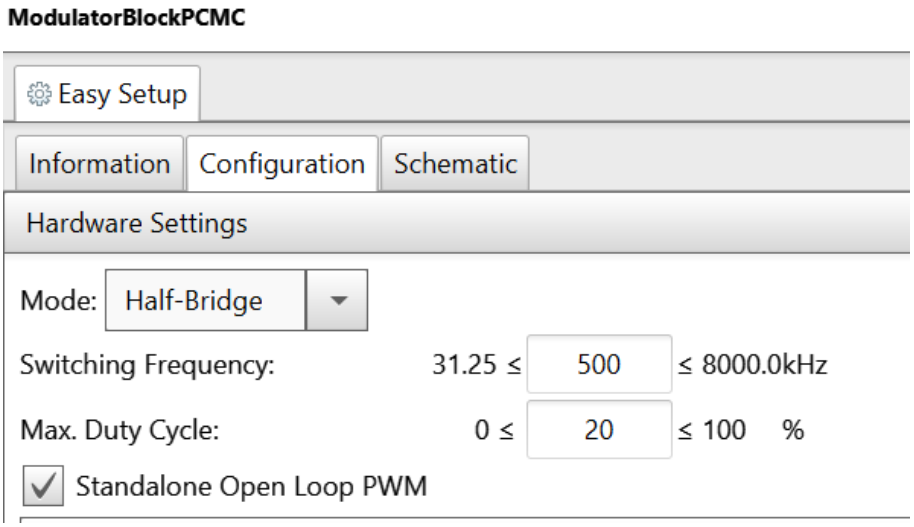
5. Go to the Device Resources area, click **SMPS Power Controllers** and expand **CIP Blocks**, double click on **ModulatorBlockPCMC**. This action will move the selected module to the Project Resources area.

Figure 4-4. ModulatorBlockPCMC



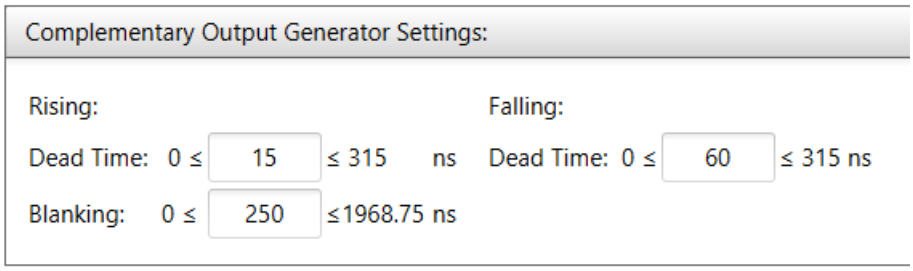
6. In the Project Resources area, click the **ModulatorBlockPCMC**. On the **Configuration** tab, under Hardware Settings, select Half-Bridge mode. Change the switching frequency to 500 kHz, and the duty cycle to 20%. Check **Standalone Open Loop PWM**.

Figure 4-5. Hardware Settings for Open Loop



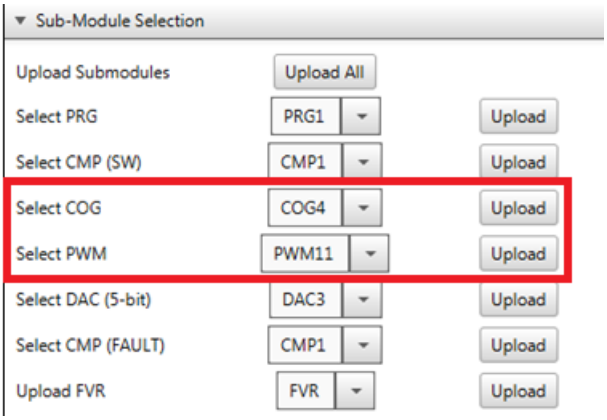
7. Under the Complementary Output Generator Settings, change rising dead time to 15 ns, falling dead time to 60 ns, and blanking time to 250 ns.

Figure 4-6. Complementary Output Generator Settings for Open Loop



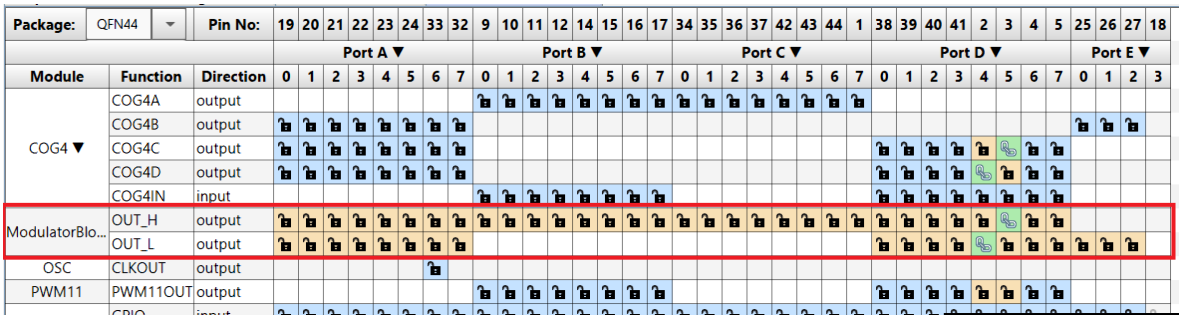
8. Select COG4 and PWM11 in the Sub-Module Selection and click the **Upload** button. Check if COG4 and PWM11 have been correctly added to the Project Resources area.

Figure 4-7. Sub-Module Selection for Open Loop



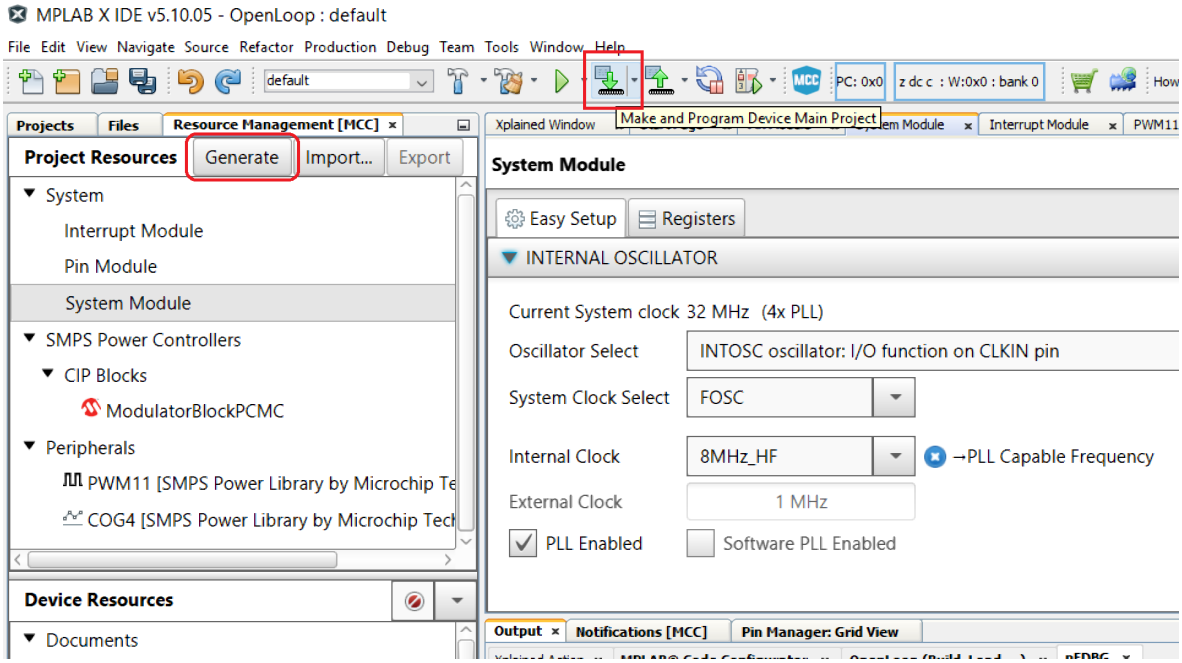
9. Go to the Pin Manager: Grid View. Search for the Modulator section. Select RD5 as the output pin for signal OUT_H and RD4 as the output pin for signal OUT_L.

Figure 4-8. Pin Manager Selection for Open Loop



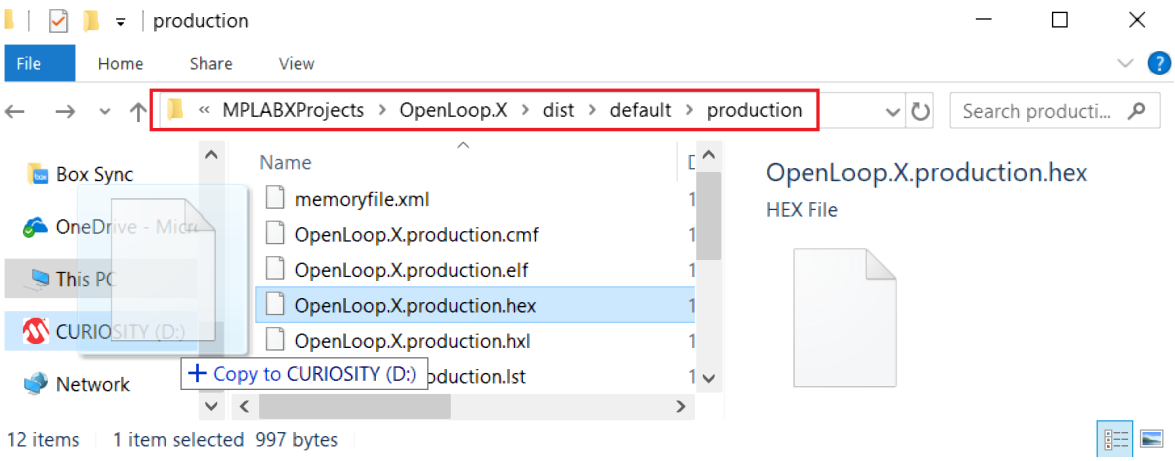
10. Click the **Generate** button from Project Resources area to generate the code.
11. Program the PIC16F1779 device on the CIP Hybrid Power Starter Kit by clicking the “Make and Program Device Main Project” icon.

Figure 4-9. Generating Code Button and Programming



12. Alternatively, the user can also download the Open Loop firmware to the CIP Hybrid Power Starter Kit by dragging the generated `.hex` file of the project to the CURIOSITY drive. The `.hex` file is located on the --dist\default\production folder.

Figure 4-10. Drag and Drop Method for Programming the Device



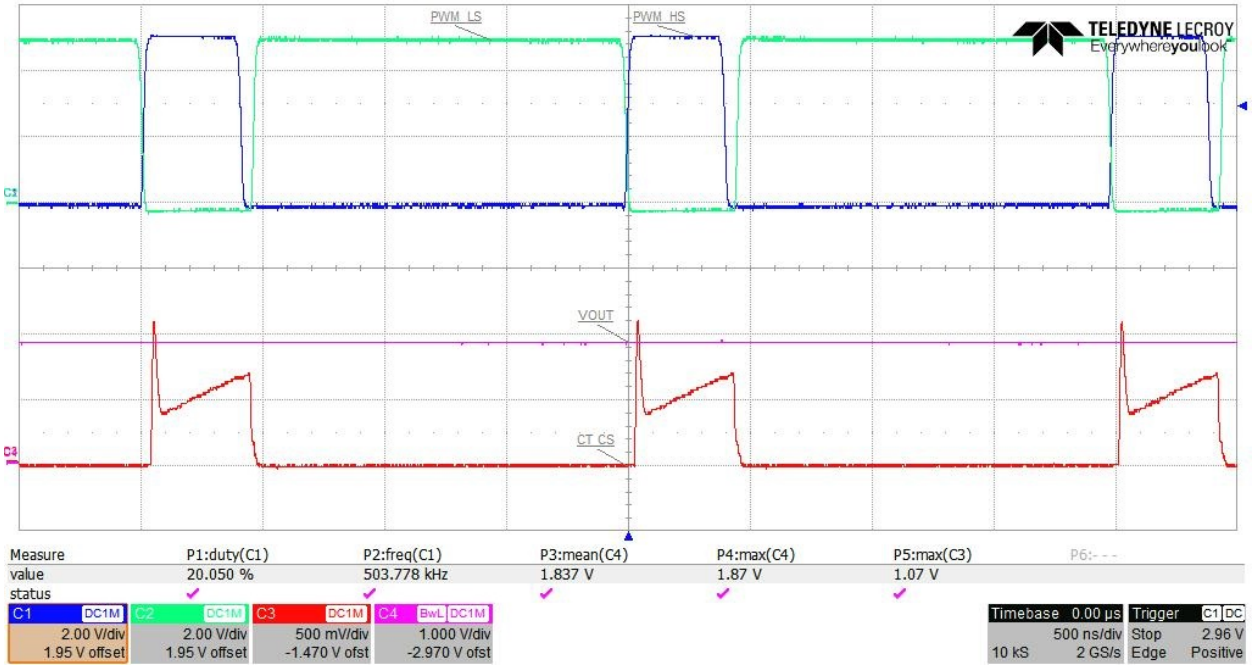
13. The CIP Hybrid Power Starter Kit can now be tested for Open Loop operation and will immediately start to generate the PWM output signals driving the synchronous buck converter.

4.1.2 Open Loop Test

Below are the steps for testing the Open Loop operation of the CIP Hybrid Power Starter Kit.

1. Remove programming interface. Place CH1 oscilloscope probe to PWM_HS test point, CH2 oscilloscope probe to PWM_LS test point, CH3 oscilloscope probe to CT_CS test point, and CH4 oscilloscope probe to VOUT test point.
2. Connect DC supply (set to 9V) and LOAD (set to 2A). Power-up the board. PWM_HS, PWM_LS and CT_CS signals and VOUT can be monitored.
3. Increasing VIN will increase VOUT following the equation VOUT = [duty ratio] * VIN.

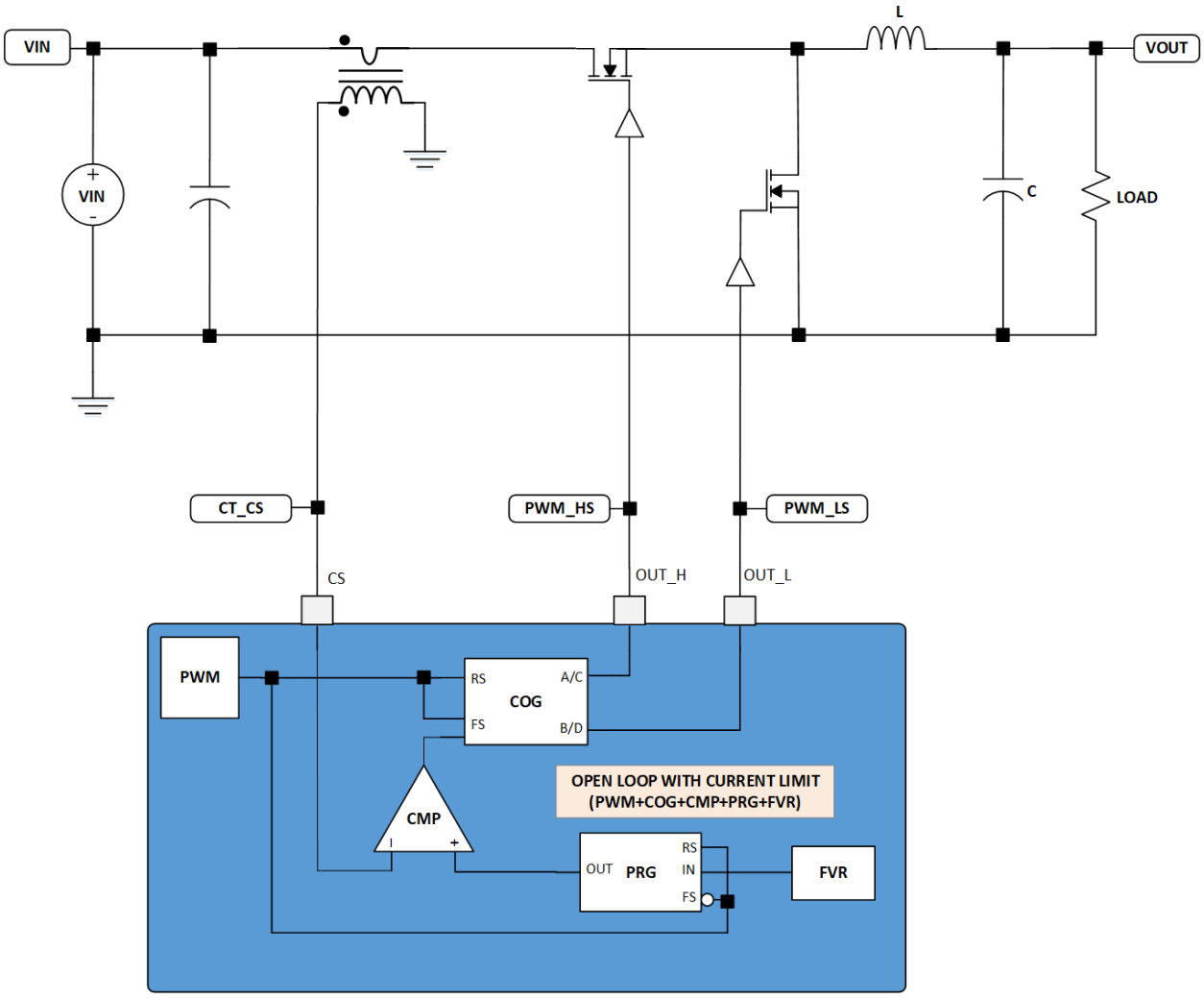
Figure 4-11. PWM_HS, PWM_LS and CT_CS Signals and VOUT Measurement



4.2 Open Loop with Current Limit (PWM+COG+CMP+PRG+FVR) Mode

The current limit is simulated by adding another falling source to the COG module. This falling source is derived from the comparator CMP output. The CMP controls the duty cycle by comparing the input current sense signal from the current transformer to a reference level set by the fixed voltage reference (FVR). The reference signal is slope-compensated before being fed to the comparator by adding a negative ramp to the FVR using the Programmable Ramp Generator (PRG). The figure below shows the block diagram of the open loop configuration.

Figure 4-12. Open Loop with Current Limit Configuration



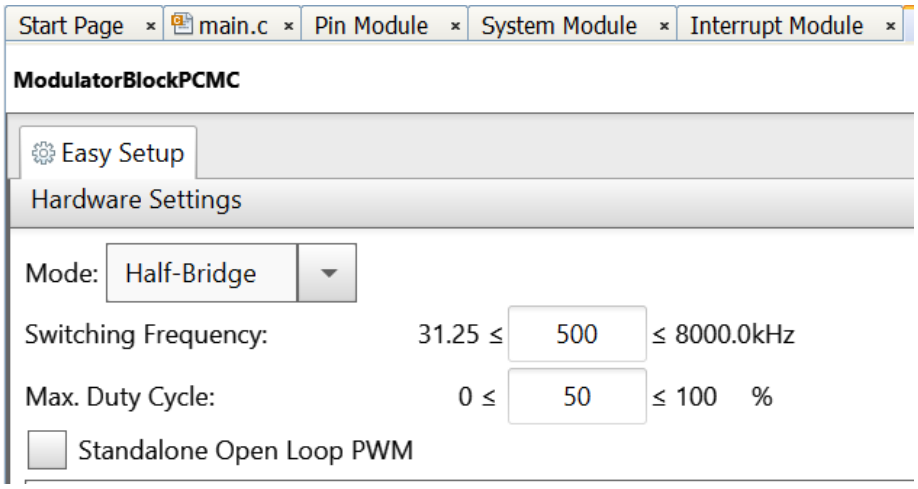
4.2.1 MCC SMPS Library Configuration for Open Loop with Current Limit

The following instructions show how to setup the peripherals of the CIP Hybrid Power Starter Kit to be able to operate in Open Loop with Current Limit test mode.

1. Open MPLAB X. Connect the CIP Hybrid Power Starter Kit to the computer through an on-board debugger USB port using a conventional micro-USB cable. MPLAB X will detect the CIP Hybrid Power Starter Kit and an Xplained Window appears that provides relevant information about the board.

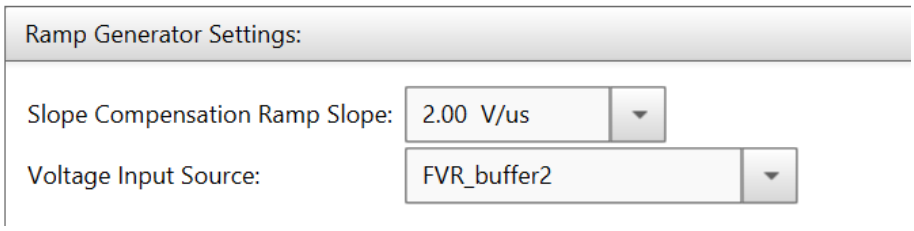
2. Create new Standalone Project in MPLAB X. Select the PIC16F1779 device. Select the CIP Hybrid Starter Kit as programming tool. Name this project “OpenLoopCurrentLimit”.
3. Open MCC. Save the MCC configuration as `OpenLoopCurrentLimit.mc3`.
4. In the Project Resources area, change the internal oscillator clock to 8 MHz from the System Module. On the Pin Manager, change the package to QFN44.
5. Go to the Device Resources area, click **SMPS Power Controllers** and expand **CIP Blocks**, double click on **ModulatorBlockPCMC**. This action will move the selected module to the Project Resources area.
6. In the Project Resources area, click the **ModulatorBlockPCMC**. Go to the **Configuration** tab, under Hardware Settings, change the switching frequency to 500 kHz, and the duty cycle to 50%. Uncheck **Standalone Open Loop PWM**.

Figure 4-13. Hardware Settings for Open Loop with Current Limit



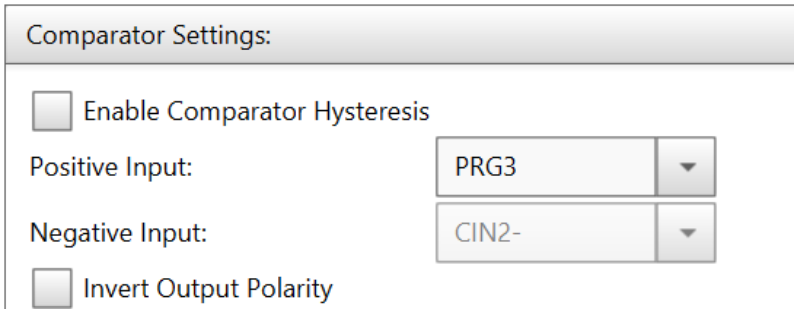
7. Under the Ramp Generator Settings, add slope compensation ramp of 2 V/us and use FVR_buffer2 as the DC offset.

Figure 4-14. Ramp Generator Settings for Open Loop with Current Limit



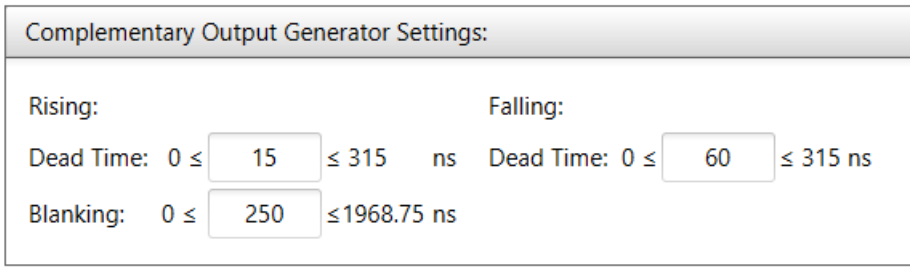
8. Under the Comparator Settings, select PRG3 as the positive input of the comparator.

Figure 4-15. Comparator Settings for Open Loop with Current Limit



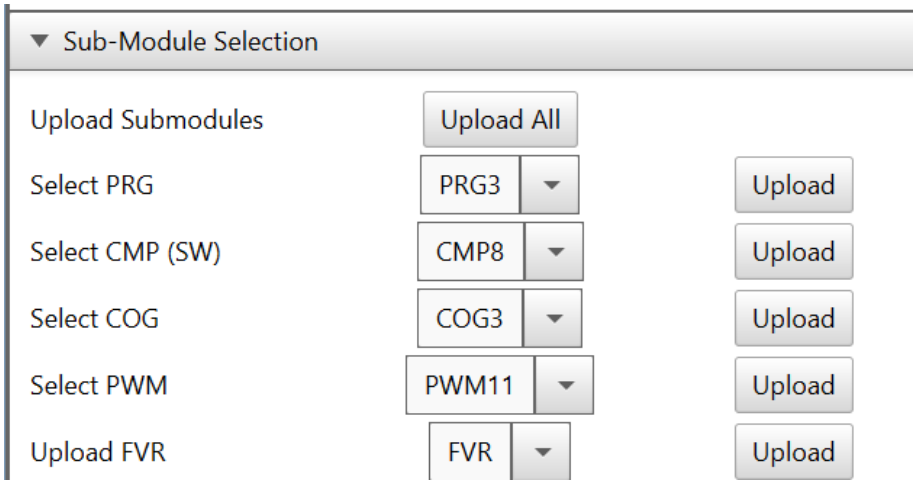
9. Under the Complementary Output Generator Settings, change rising dead time to 15 ns, falling dead time to 60 ns, and blanking time to 250 ns.

Figure 4-16. Complementary Output Generator Settings for Open Loop with Current Limit



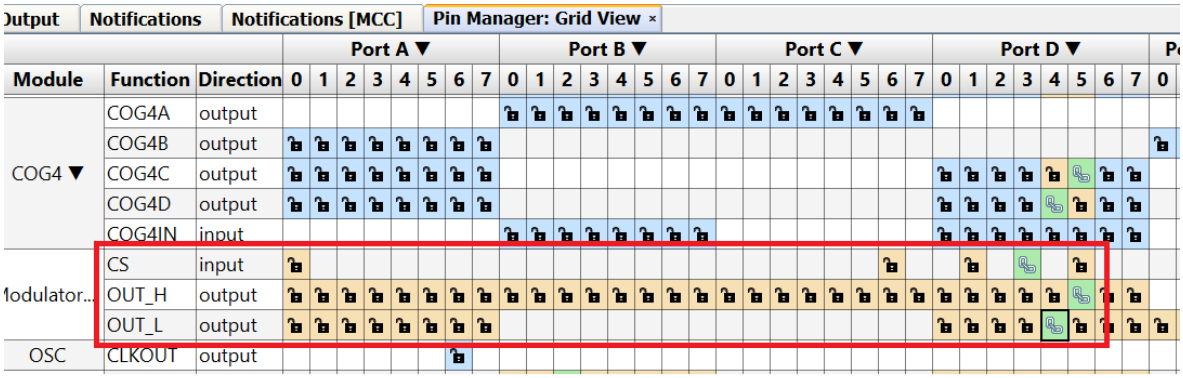
10. Select PRG3, CMP8, COG4, PWM11 and FVR on the Sub-Module Selection and **Upload All** button. Check if all the peripherals have been correctly added to the Project Resources area.

Figure 4-17. Sub-Module Selection for Open Loop with Current Limit



11. Go to Pin Manager: Grid View. Select RD5 as output pin for signal OUT_H, RD4 as output pin for signal OUT_L and RD3 as input pin for feedback signal CS.

Figure 4-18. Pin Manager Selection for Open Loop with Current Limit



12. Click **Generate** button to generate the code. Program the PIC16F1779 device on the CIP Hybrid Power Starter Kit by clicking the “Make and Program Device Main Project” icon.
13. Alternatively, the user can also download the Open Loop firmware to the CIP Hybrid Power Starter Kit by dragging the generated `.hex` file of the project to the CURIOSITY drive. The `.hex` file is located on the --dist\default\production folder.

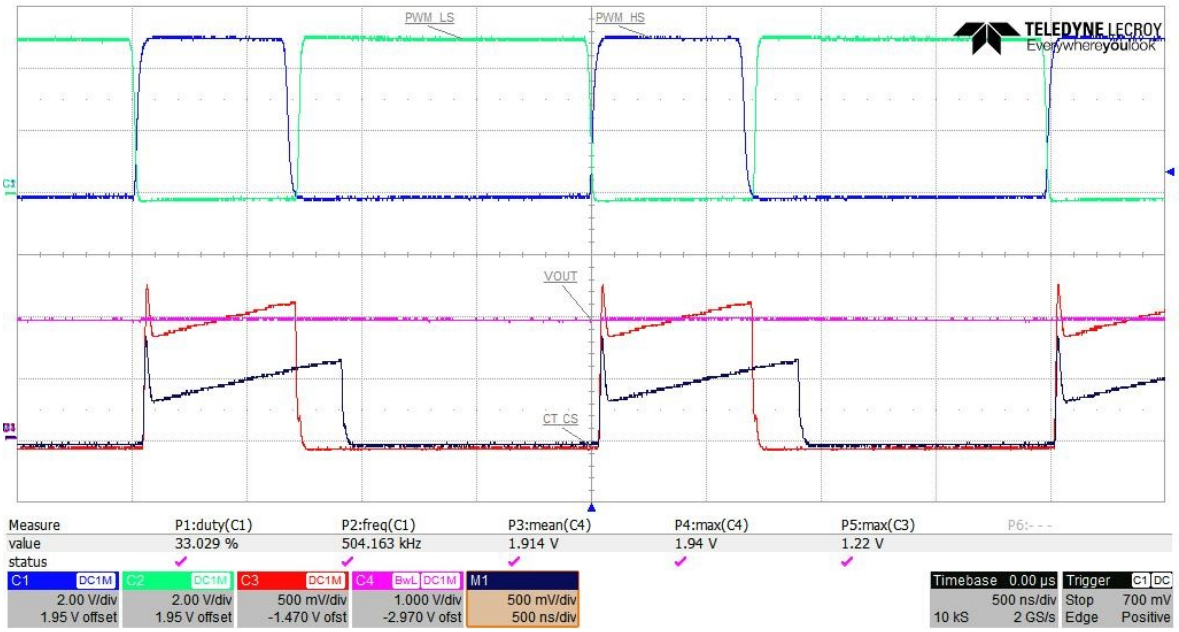
14. The CIP Hybrid Power Starter Kit can now be tested for Open Loop with Current Limit operation and will immediately start to generate the PWM output signals driving the synchronous buck converter.

4.2.2 Open Loop with Current Limit Test

Below are the steps for testing the Open Loop with Current Limit operation of the CIP Hybrid Power Starter Kit.

1. Remove programming interface. Place CH1 oscilloscope probe to PWM_HS test point, CH2 oscilloscope probe to PWM_LS test point, CH3 oscilloscope probe to CT_CS test point, and CH4 oscilloscope probe to VOUT test point.
2. Connect DC supply (set to 6V) and LOAD (set to 2A). Power-up the board. PWM_HS, PWM_LS and CT_CS signals and VOUT can be monitored.
3. Increasing VIN increases VOUT, but duty cycle is decreases because the CT_CS signal is touching the PRG signal at the defined slope.

Figure 4-19. PRG Effect on CT_CS Signal and PWM Duty Cycle



4. Increasing the load will decrease VOUT, since the duty cycle is being limited by the CT_CS signal touching the PRG signal.

4.3 PCMC Closed Loop Mode

Peak Current Mode Control is a dual loop control mode consisting of an outer voltage feedback loop and an inner inductor current feedback loop.

The outer voltage loop uses an on-chip Operational Amplifier (OPA) as differential error amplifier, comparing the output voltage feedback signal against an internal reference voltage. This reference voltage is applied by a Digital-to-Analog Converter (DAC), which is configured and set by firmware. The inverting input and output of the error amplifier are routed to device pins to insert an external RC compensation filter into the amplifier feedback loop.

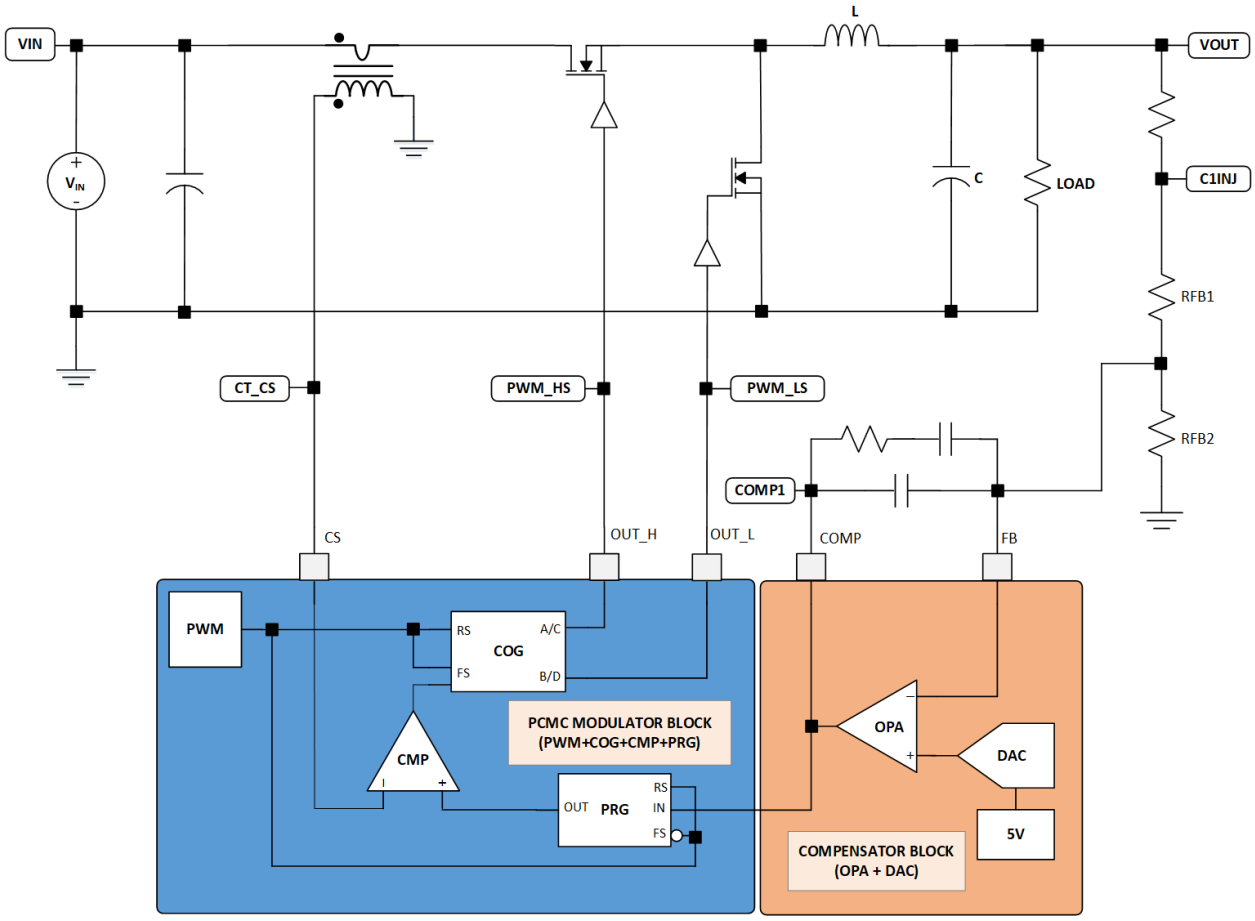
The inner inductor current feedback loop is closed by routing the inductor current feedback signal on to an analog comparator CMP, which compares the current feedback signal against the output of the error

amplifier. The comparator output is further routed into the PWM output generator logic COG, truncating the active on-time when the inductor current exceeds the reference signal level.

In this setup, the digital PWM module is determining the switching period and maximum duty ratio at which the active on-time will be terminated in case the COG has not been tripped by the current loop comparator CMP.

To prevent sub-harmonic oscillations in this fixed frequency, continuous conduction mode PCMC system, the PRG is put between the error amplifier OPA output and the inductor current comparator CMP reference input. This module is modulating a negative ramp onto output signal of the error amplifier OPA. The PRG modulation ramp is synchronized with the PWM to reset the negative sawtooth waveform at the end of the period. The figure below shows the peripheral configuration of the microcontroller for PCMC Closed Loop operation.

Figure 4-20. PCMC Closed Loop Configuration



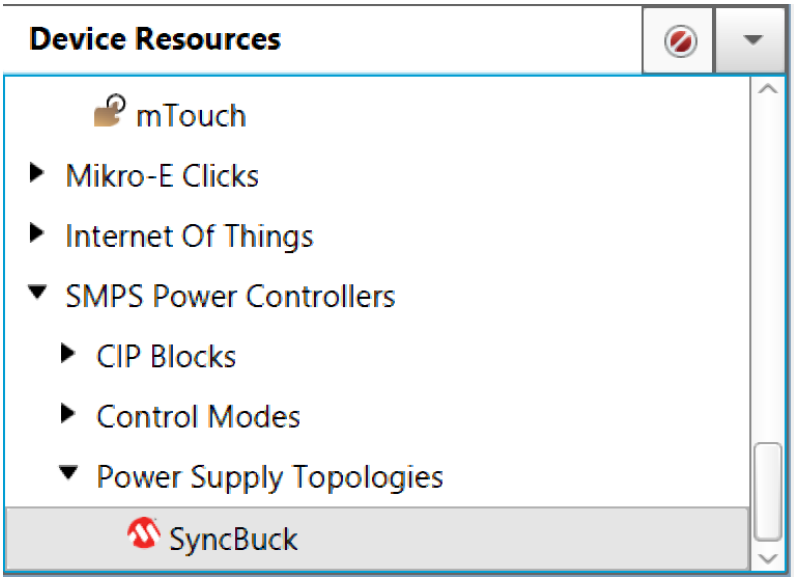
4.3.1 MCC SMPS Library Configuration for PCMC Closed Loop

The following instructions show how to setup the peripherals of the CIP Hybrid Power Starter Kit to be able to operate in PCMC test mode.

1. Open MPLAB X. Connect the CIP Hybrid Power Starter Kit to the computer through an on-board debugger USB port using a conventional micro-USB cable. MPLAB X will detect the CIP Hybrid Power Starter Kit and an Xplained Window appears that provides relevant information about the board.

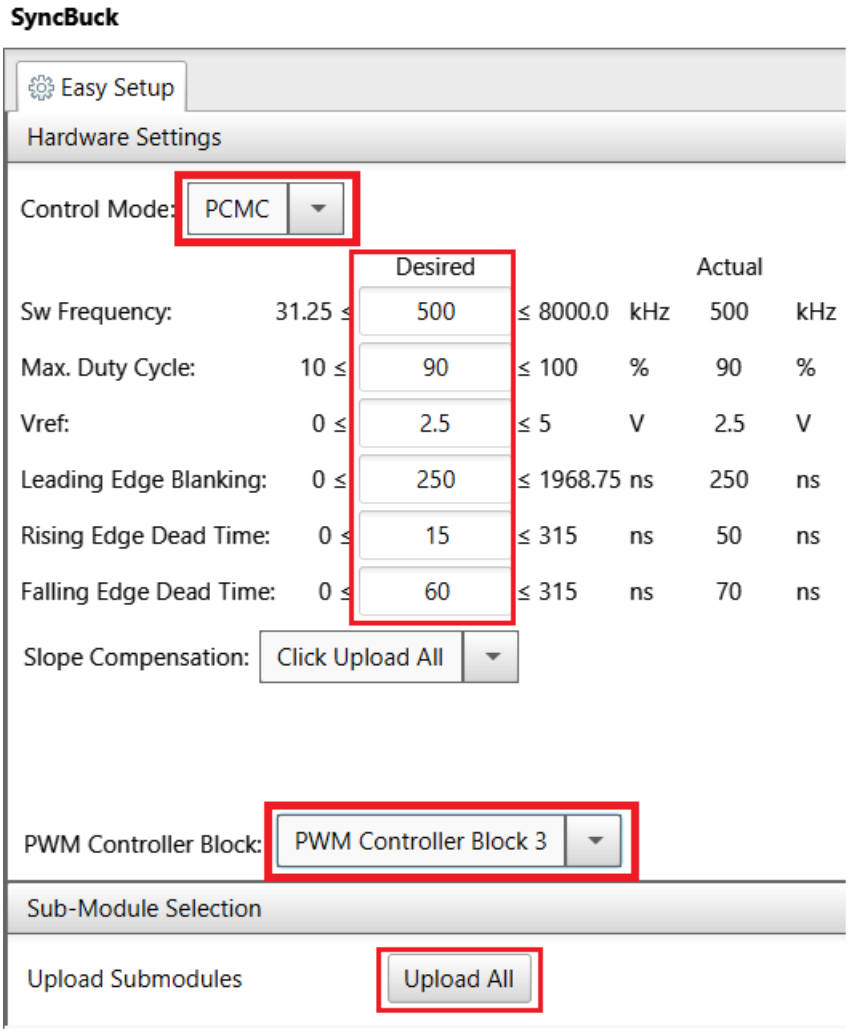
2. Create new Standalone Project in MPLAB X. Select the PIC16F1779 device. Select the CIP Hybrid Starter Kit as programming tool. Name this project “PCMC”.
3. Open MCC. Save the MCC configuration as `PCMC.mc3`.
4. In the Project Resources area, change the internal oscillator clock to 8 MHz from the System Module. On the Pin Manager, change the package to QFN44.
5. Go to the Device Resources area, click **SMPS Power Controllers** and expand **Power Supply Topologies**, double click on **SyncBuck**. This action will move the SyncBuck to the Project Resources area.

Figure 4-21. Selecting SyncBuck from Device Resources



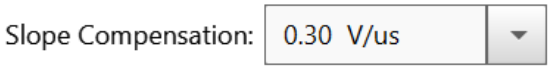
6. In the Project Resources area, click on **SyncBuck**. On the **Configuration** tab, under Hardware Settings, select PCMC as the control mode. Change the switching frequency to 500 kHz, the duty cycle to 90%, reference voltage to 2.5V, leading edge blanking to 250 ns, rising edge dead time to 15 ns, and falling edge dead time to 60 ns. Choose PWM Controller Block 3.
7. Click the **Upload All** button. This action will load all the peripherals of the PWM Controller Block 3 on the Project Resources area.

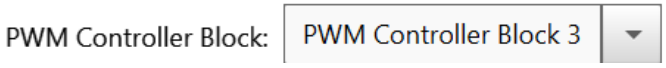
Figure 4-22. Hardware Settings for PCMC Synchronous Buck Converter



8. Add slope compensation of 0.3 V/us.

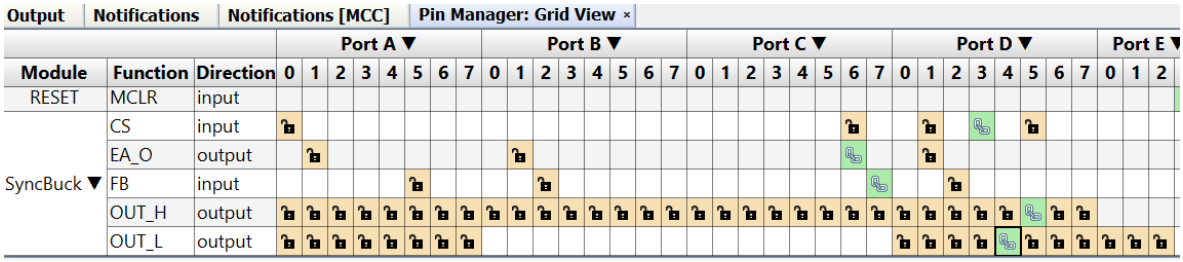
Figure 4-23. Slope Compensation for PCMC Synchronous Buck Converter





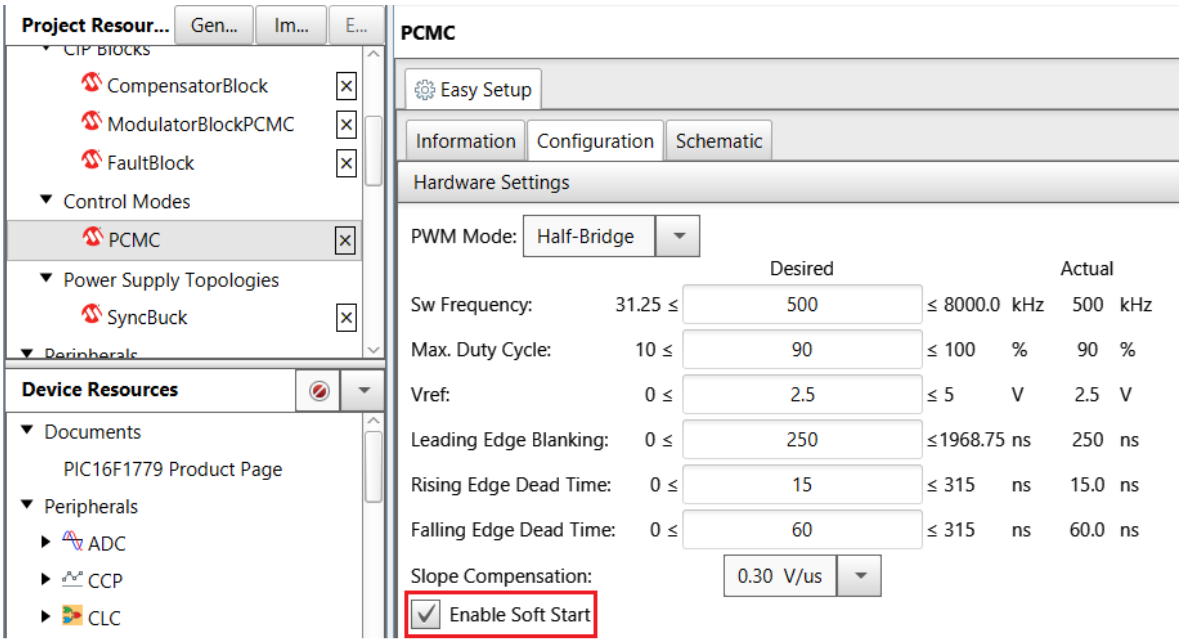
9. Go to the Pin Manager: Grid View. Assign RD3 as input pin for CS, RC6 as output pin for signal EA_OUT, RC7 as input pin for signal FB, RD5 as output pin for signal OUT_H, and RD4 as output pin for signal OUT_L.

Figure 4-24. Pin Assignments for PCMC Synchronous Buck Converter



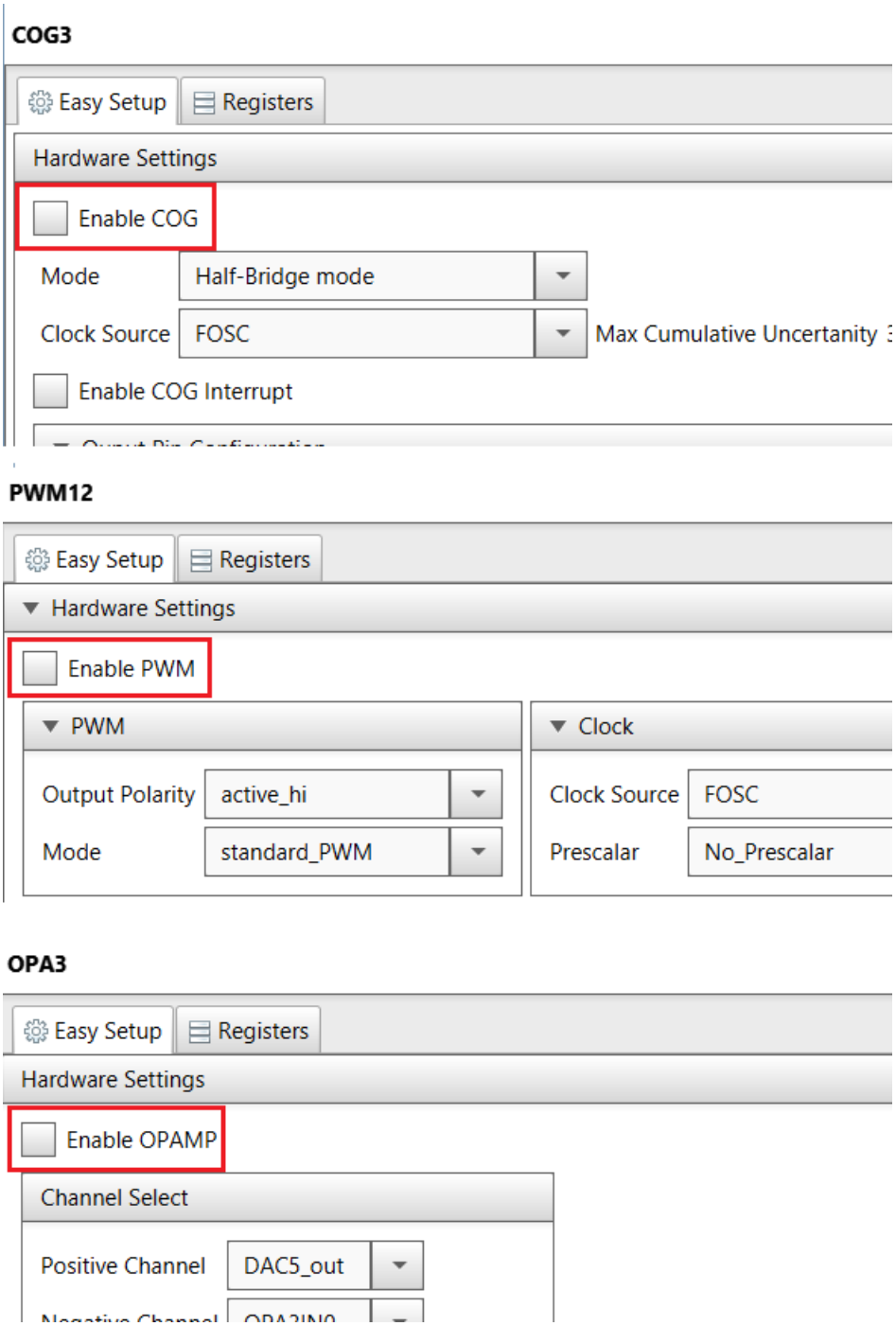
10. Soft start is enabled by default on the PCMC Control Mode section.

Figure 4-25. Enabling Soft Start in PCMC Synchronous Buck Converter



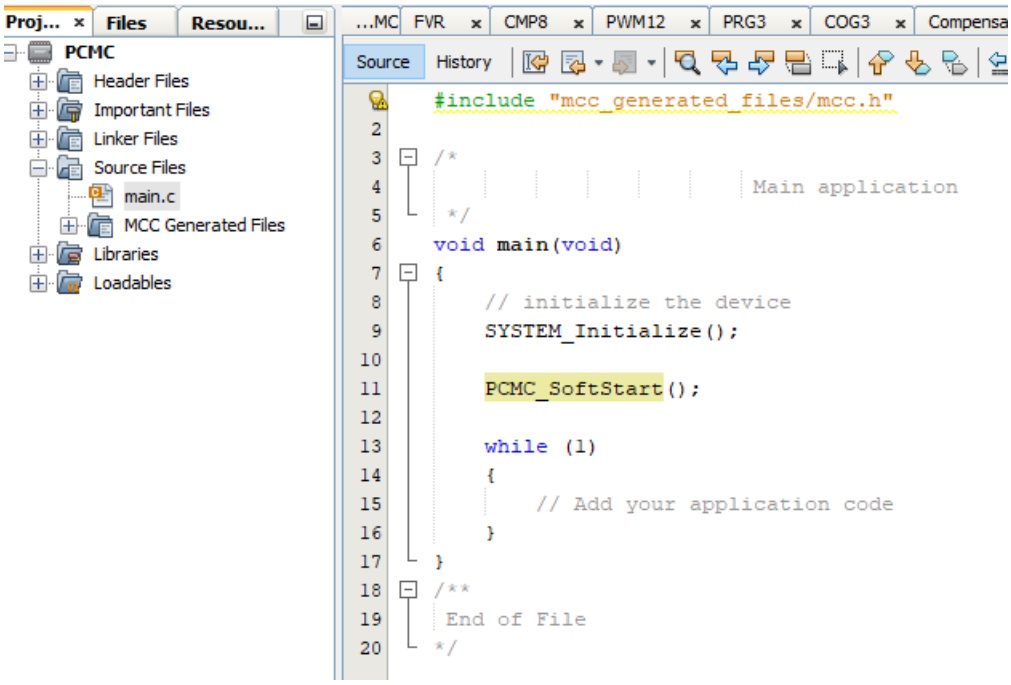
11. Enabling soft start disables the COG, PWM and OPA peripherals at power on.

Figure 4-26. COG, PWM and OPA Disabled Initially for Soft Start



12. Click **Generate** button to generate the code. On the `main.c`, add the following line of code, `PCMC_SoftStart();`.

Figure 4-27. Inserting 'PCMC_SoftStart()' function inside main.c



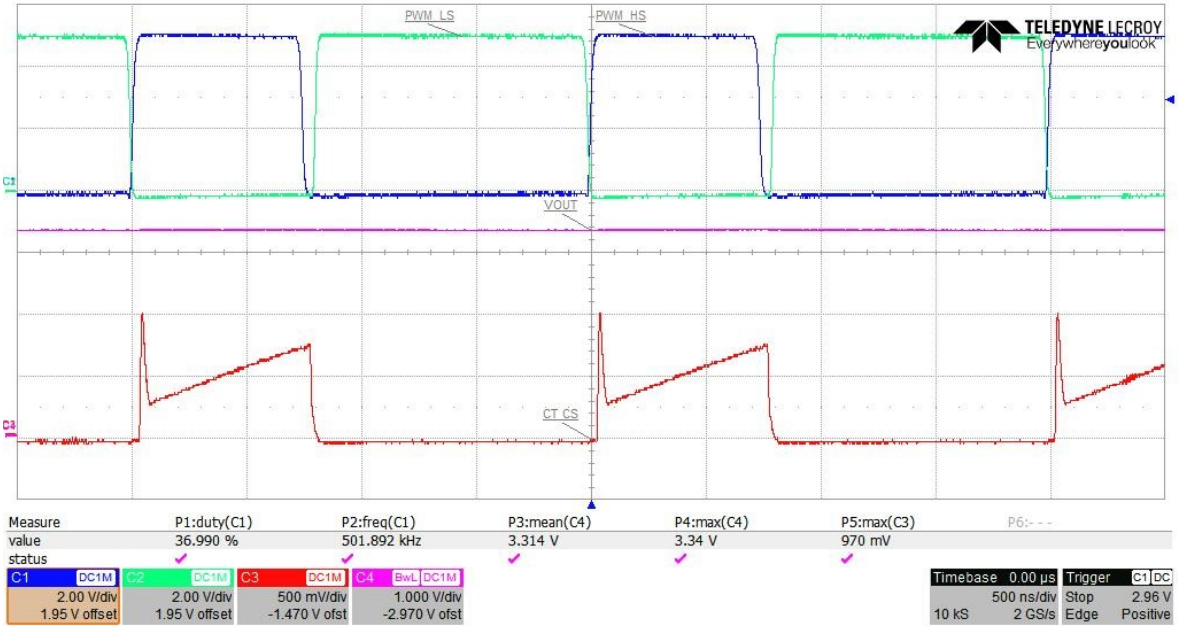
13. Program the PIC16F1779 device on the CIP Hybrid Power Starter Kit by clicking the "Make and Program Device Main Project" icon.
14. Alternatively, the user can also download the PCMC firmware to the CIP Hybrid Power Starter Kit by dragging the generated `.hex` file of the project to the CURIOSITY drive. The `.hex` file is located on the --dist\default\production folder.
15. The board is now configured for PCMC-CS operation.

4.3.2 PCMC Closed Loop Test

Below are the steps for testing the PCMC Closed Loop operation of the CIP Hybrid Power Starter Kit.

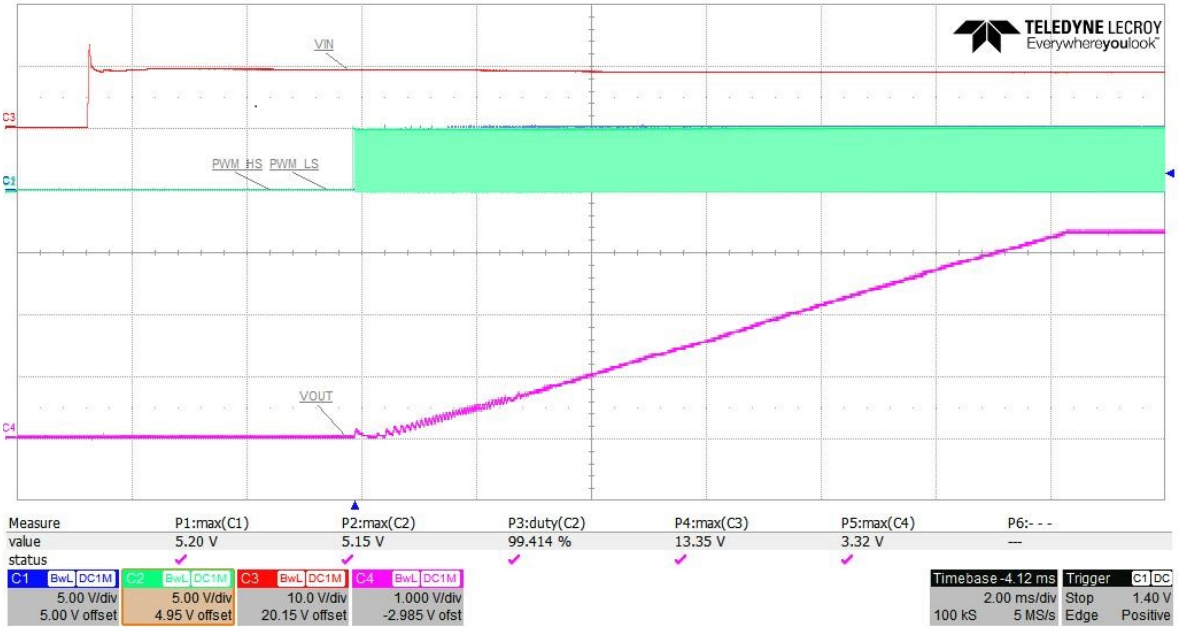
1. Remove programming interface. Place CH1 oscilloscope probe to PWM_HS test point, CH2 oscilloscope probe to PWM_LS test point, CH3 oscilloscope probe to CT_CS test point, and CH4 oscilloscope probe to VOUT test point.
2. Connect DC supply (set to 6V) and LOAD (set to 2A). Power-up the board. PWM_HS, PWM_LS and CT_CS signals and VOUT can be monitored.
3. Increase VIN up to 16V. VOUT is regulated to 3.3V.
4. Increase LOAD to 4A. VOUT is regulated to 3.3V.

Figure 4-28. PWM_HS, PWM_LS, CT_CS and VOUT at VIN = 9V; LOAD = 2A



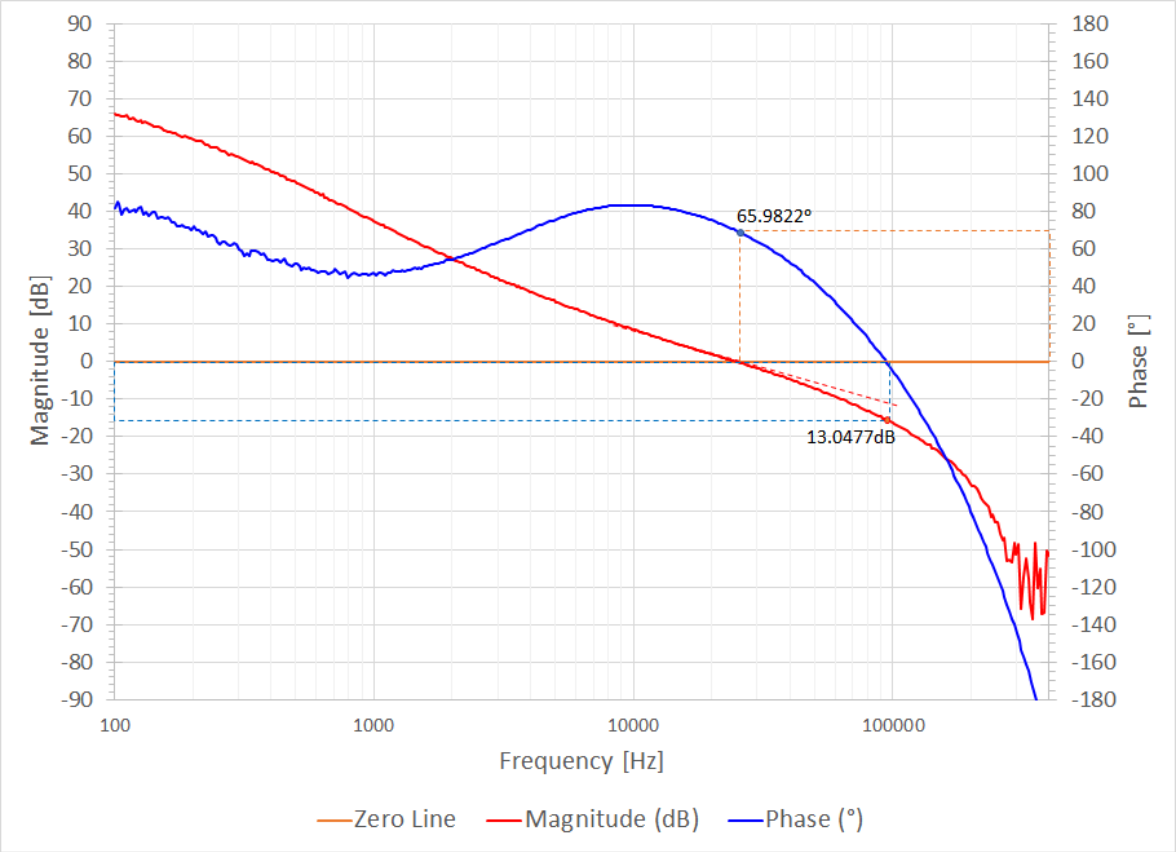
5. Connect CH3 to VIN. Capture soft start by lowering the oscilloscope time base and setting positive edge trigger source to VOUT.

Figure 4-29. Monitoring Soft Start at Start-up



6. The control loop stability is observed by measuring the frequency response of the open loop gain in the closed loop system. This magnitude/phase measurement is commonly used to determine the three main stability criteria indicators phase margin, gain margin and gain slope at the crossover frequency of the gain.

Figure 4-30. PCMC Loop Gain and Phase Measurements at VIN = 9V, LOAD = 4A



4.4 VMC Closed Loop Mode

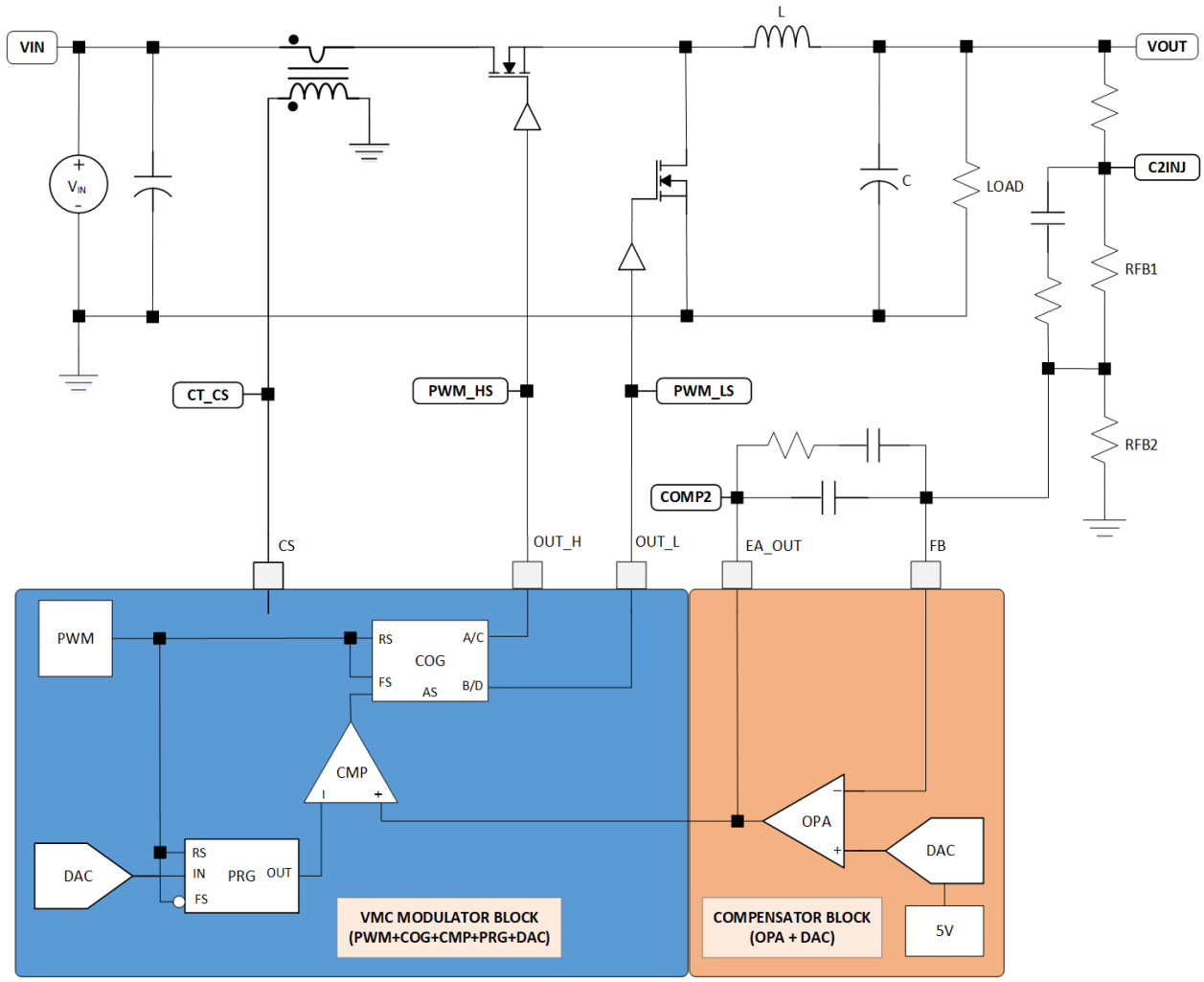
Voltage Mode Control is established by closing the voltage feedback loop through an error amplifier and analog ramp comparator CMP.

The voltage loop uses an on-chip Operational Amplifier (OPA) as differential error amplifier, comparing the output voltage feedback signal against an internal reference voltage. This reference voltage is applied by DAC, which is configured and set by firmware. The inverting input and output of the error amplifier are routed to device pins to insert an external RC compensation filter into the amplifier feedback loop.

The PRG is configured to produce a positive sawtooth waveform, which is synchronized and driven by the digital PWM generator. The peak voltage of the sawtooth is determined by the switching frequency and user-selected slew rate of the ramp voltage. An analog comparator is used to compare the PRG sawtooth waveform against the error amplifier output signal (reference). The comparator output is further routed into the PWM output generator logic COG, truncating the active on-time when the PRG sawtooth ramp exceeds the error amplifier reference signal level. The COG logic performs the function of an SR latch, preventing undesired resets until the end of the switching period.

In this setup, the digital PWM module is determining the switching period and maximum duty ratio at which the active on-time will be terminated in case the COG has not been tripped by the ramp generator comparator.

Figure 4-31. VMC Closed Loop Configuration



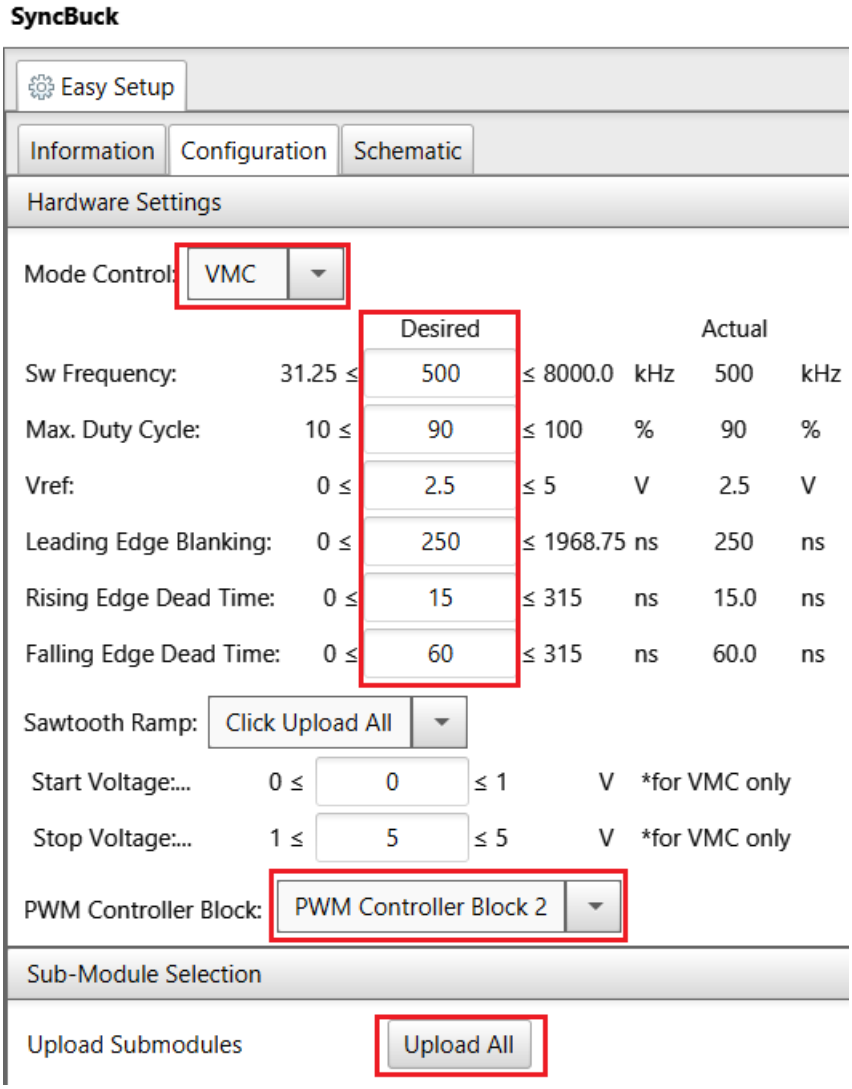
4.4.1 MCC SMPS Library Configuration for VMC Closed Loop

The following instructions show how to setup the peripherals of the CIP Hybrid Power Starter Kit to be able to operate in VMC test mode.

1. Open MPLAB X. Connect the CIP Hybrid Power Starter Kit to the computer through an on-board debugger USB port using a conventional micro-USB cable. MPLAB X will detect the CIP Hybrid Power Starter Kit and an Xplained Window appears that provides relevant information about the board.
2. Create new Standalone Project in MPLAB X. Select the PIC16F1779 device. Select the CIP Hybrid Starter Kit as programming tool. Name this project “VMC”.
3. Open MCC. Save the MCC configuration as `VMC.mc3`.
4. In the Project Resources area, change the internal oscillator clock to 8 MHz from the System Module. On the Pin Manager, change the package to QFN44.
5. Go to the Device Resources area, click **SMPS Power Controllers** and expand **Power Supply Topologies**, double click on **SyncBuck**. This action will move the SyncBuck to the Project Resources area.

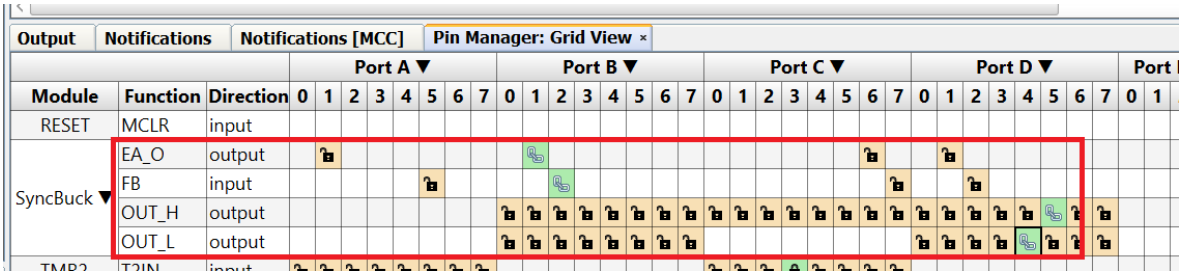
6. In the Project Resources area, click on **SyncBuck**. On the **Configuration** tab, under Hardware Settings, select VMC as control mode. Change the switching frequency to 500 kHz, the duty cycle to 90%, reference voltage to 2.5V, leading edge blanking to 250 ns, rising edge dead time to 15 ns and falling edge dead time to 60 ns. Add sawtooth ramp of 2.5V/us. Choose PWM Controller Block 2.
7. Click the **Upload All** button. This action will load all the peripherals of the PWM Controller Block 3 on the Project Resources area.

Figure 4-32. Hardware Settings for VMC Synchronous Buck Converter



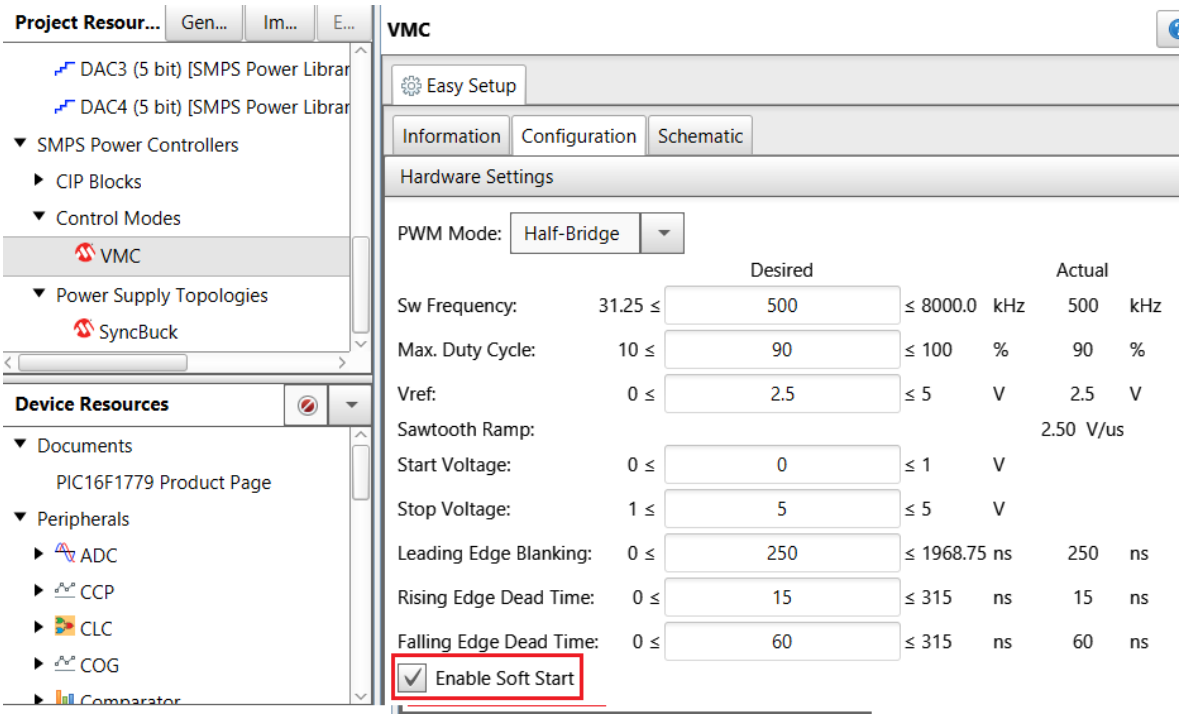
8. When all the peripherals are loaded, the sawtooth ramp slope will automatically be updated to 2.5 V/us. This is computed with start voltage of 0V, a stop voltage of 5V, and the switching frequency of 500 kHz using the formula Ramp = (stop voltage – start voltage) / (2*switching frequency).
9. Go to the Pin Manager: Grid View. Assign RB1 as output pin for signal EA_O, RB2 as input pin for signal FB, RD5 as output pin for signal OUT_H and RD4 as output pin for signal OUT_L.

Figure 4-33. Pin Assignments for Sync Buck VMC



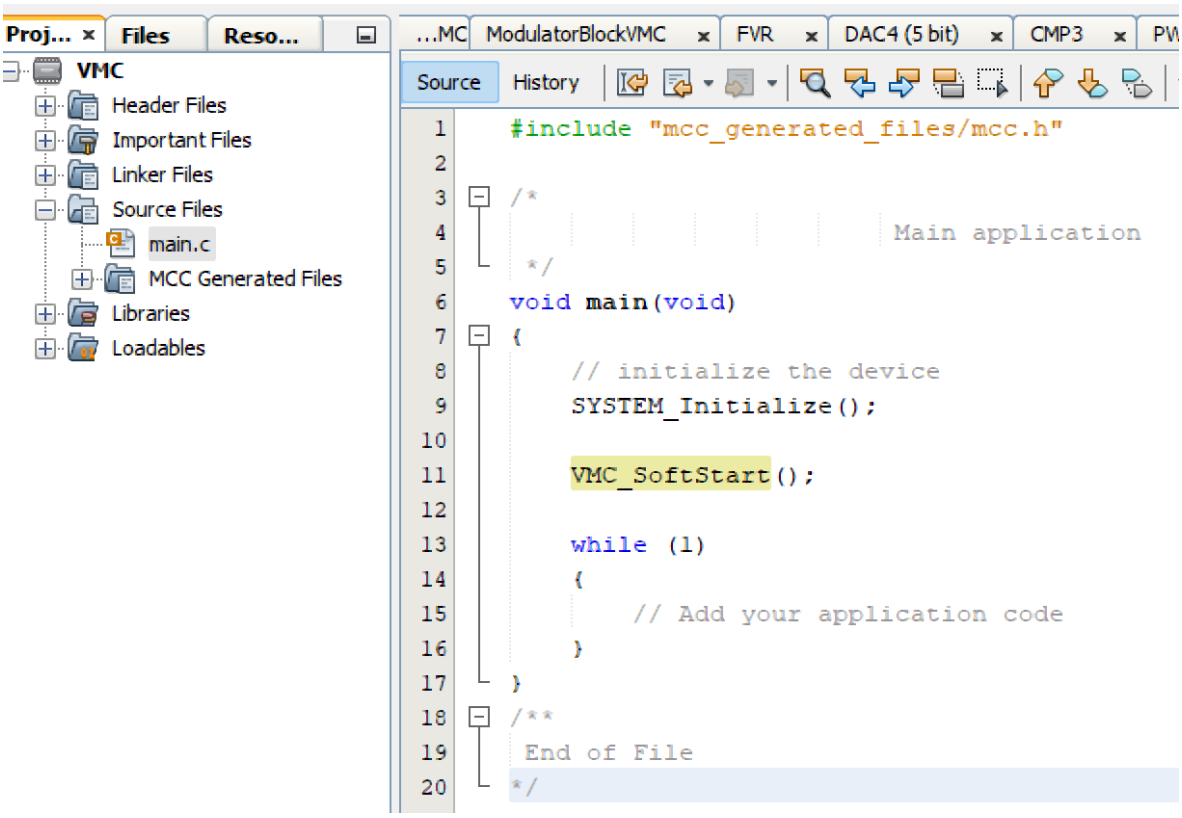
10. Soft start is enabled by default on the VMC Control Mode section.

Figure 4-34. Pin Assignments for Sync Buck VMC



11. Enabling the soft start disables the COG, PWM and OPA peripherals at power on.
12. Click the **Generate** button to generate the code. On the `main.c`, add the following line of code, `VMC_SoftStart();`.

Figure 4-35. Inserting 'VMC_SoftStart()' Function Inside main.c



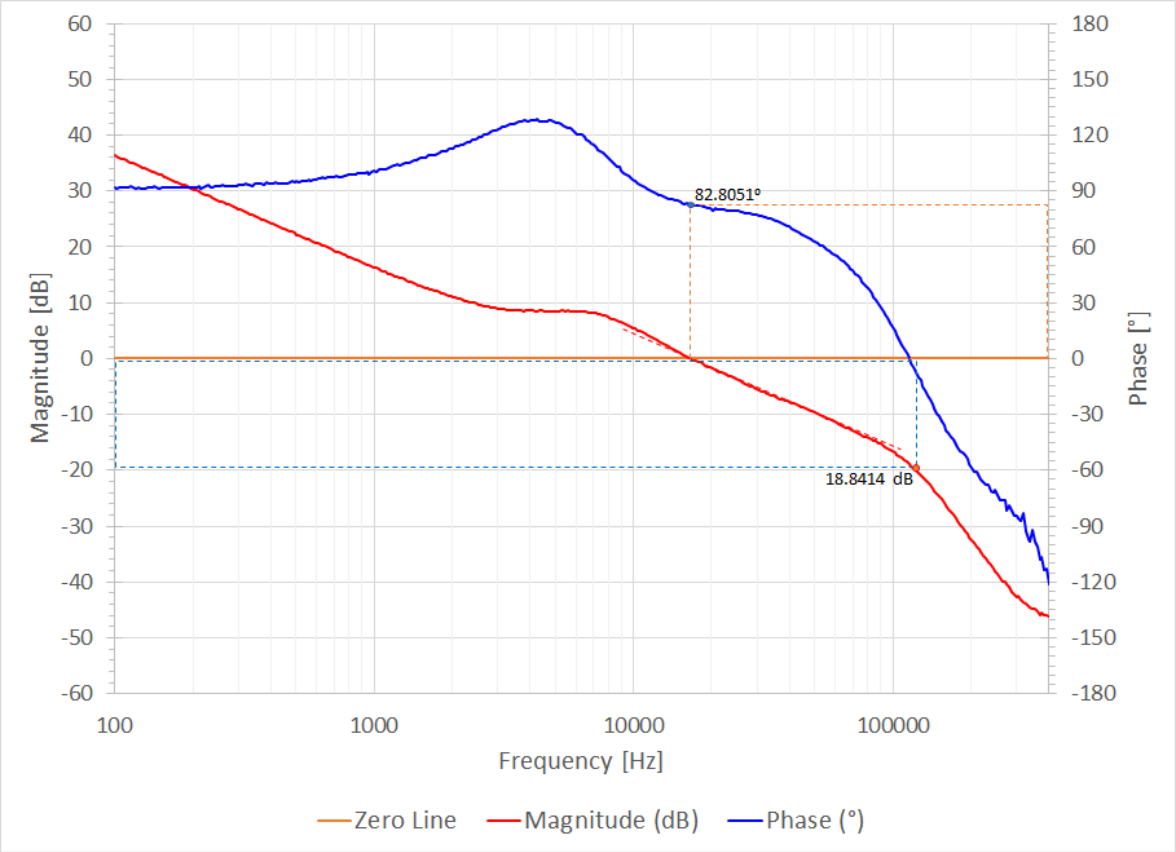
13. Program the PIC16F1779 device on the CIP Hybrid Power Starter Kit by clicking the "Make and Program Device Main Project" icon.
14. Alternatively, the user can also download the PCMC firmware to the CIP Hybrid Power Starter Kit by dragging the generated `.hex` file of the project to the CURIOSITY drive. The `.hex` file is located on the --dist\default\production folder.
15. The board is now configured in VMC operation.

4.4.2 VMC Closed Loop Test

Below are the steps for testing the VMC Closed Loop operation of the CIP Hybrid Power Starter Kit.

1. Remove programming interface. Place CH1 oscilloscope probe to PWM_HS test point, CH2 oscilloscope probe to PWM_LS test point, CH3 oscilloscope probe to CT_CS test point, and CH4 oscilloscope probe to VOUT test point.
2. Connect DC supply (set to 6V) and LOAD (set to 2A). Power-up the board. PWM_HS, PWM_LS and CT_CS signals and VOUT can be monitored.
3. Increase VIN up to 16V. VOUT is regulated to 3.3V.
4. Increase LOAD to 4A. VOUT is regulated to 3.3V.
5. Observe control loop stability is by measuring the frequency response of the open loop gain in the closed loop system. This magnitude/phase measurement is commonly used to determine the three main stability criteria indicators phase margin, gain margin and gain slope at the crossover frequency of the gain.

Figure 4-36. VMC Gain and Phase Measurements at VIN = 9V, LOAD = 4A



5. Hardware Revision History

This user guide provides the latest available revision of the kit. This chapter contains information about known issues, a revision history of older revisions, and how older revisions differ from the latest revision.

5.1 Identifying Product ID and Revision

The revision and product identifier of the CIP Hybrid Power Starter Kit can be found in two ways; either through Microchip MPLAB X or by looking at the sticker on the bottom side of the PCB.

By connecting a CIP Hybrid Power Starter Kit to a computer with Microchip MPLAB X running, an information window will pop up. The first six digits of the serial number, which is listed under kit details, contain the product identifier and revision.

The same information can be found on the sticker on the bottom side of the PCB. Most kits will print the identifier and revision in plain text as A09-nnnn\rr, where “nnnn” is the identifier and “rr” is the revision. The boards with limited space have a sticker with only a QR-code, containing the product identifier, revision and the serial number.

The serial number string has the following format:

"nnnnrrssssssssss"

n = product identifier

r = revision

s = serial number

The product identifier for CIP Hybrid Power Starter Kit is A09-3194.

5.2 Revision 3

Revision 3 is the initially released revision.

6. Document Revision History

Doc.Rev.	Date	Comments
A	12/2018	Initial document release.

7. Appendix

7.1 Appendix A: Hardware Components

The CIP Hybrid Power Starter Kit features the following hardware components:

- PIC16F1779 Hybrid Power Microcontroller
- Synchronous Buck Converter Power Board
- High-Side Current Sense Transformer for PCMC
- Temperature Sensor
- Four Light Emitting Diodes (Two Green, One Red and One Blue)
- One Mechanical Pushbutton
- I^2C Bridge PMBus
- On-board USB Programmer/Debugger

7.1.1 PIC16F1779 Hybrid Power Microcontroller

PIC16F1779 CIP Hybrid Power microcontrollers incorporate up to four digitally enhanced analog PWM controller function blocks into a low-power, 8-bit microcontroller architecture to allow users to tailor features and functions according to application specific needs. Although tightly coupled, the PWM controller functional blocks are built in as Core Independent Peripherals (CIPs), meaning that there is no dependency of the MCU core activity during the operation of the PWM controller functional block.

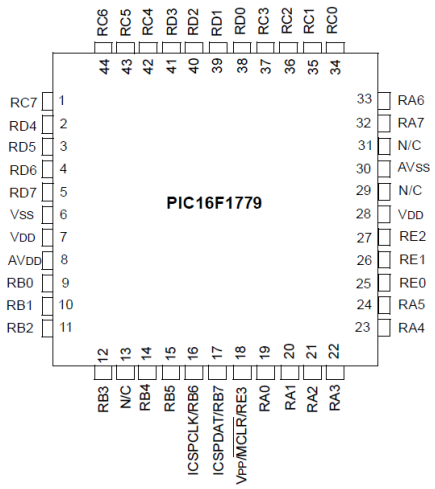
The tightly coupled system allows users to configure the PWM controller blocks at design time as well as to modify the configurations during run-time. This flexibility can be used in creating nonlinear operating profiles for applications such as programmable power supplies like USB Power delivery DC/DC converters, multi-loop control systems in battery chargers and LED drivers as well as intelligent PMIC devices for embedded systems, supporting proprietary or standardized communication, like PMBus protocols.

The tight engagement between the microcontroller and the digitally enhanced analog PWM controller blocks of the CIP Hybrid Power devices also offers considerably higher transparency of the conversion processes needed for advanced diagnostics and protection to support the ISO 26262 compliant functional safety applications.

The CIP Hybrid Power microcontrollers do not incorporate high-voltage auxiliary supplies or FET drivers. These devices are independent from application specific voltage or power levels and therefore support a very wide range of converter topologies such as Buck, Boost, non-isolated Buck-Boost, SEPIC, ZETA, Flyback, Forward, Two-Switch Forward, Half-Bridge, Full-Bridge, Phase-Shifted Full-Bridge and Resonant Converters.

The flexible PWM output configuration capabilities additionally support synchronous rectification or active clamping circuits when needed, which can be adjusted, modified and enabled or disabled during run time to optimize efficiency. The PWM generator architecture can be set up for single- and multiphase fixed frequency as well as variable frequency operation to also support hysteretic commutation modes like Constant On-Time, Constant Off-Time or Quasi-resonant operation, making these devices well suited for any kind of DC/DC and AC/DC converter or DC/AC inverter application.

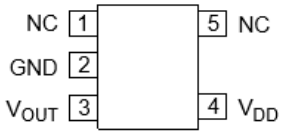
Figure 7-1. PIC16F1779



7.1.2 MCP9701A Temperature Sensor

The MCP9701A sensor with Linear Active Thermistor Integrated Circuit (IC) comprise a family of analog temperature sensors that convert temperature to analog voltage. The low-cost, low-power sensors feature an accuracy of ±2°C from 0°C to +70°C, and of ±4°C from 0°C to +70°C, while consuming 6 µA (typical) of operating current. The Voltage Output pin (VOUT) can be directly connected to the ADC input of a microcontroller. The MCP9701A temperature coefficients are scaled to provide a 1°C/bit resolution for an 8-bit ADC with a reference voltage of 5V.

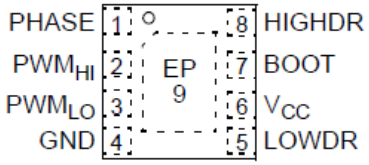
Figure 7-2. MCP9701A



7.1.3 MCP14700 Synchronous MOSFET Driver

The MCP14700 is a high-speed synchronous MOSFET driver designed to optimally drive a high-side and low-side N-Channel MOSFET. The MCP14700 has two PWM inputs to allow independent control of the external N-Channel MOSFETs. The transition thresholds for the PWM inputs are typically of 1.6V on a rising PWM input signal and typically of 1.2V on a falling PWM input signal. This makes the MCP14700 ideally suited for controllers that utilize 3.0V TTL/CMOS logic.

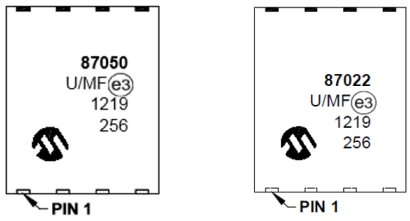
Figure 7-3. MCP14700



7.1.4 MCP87050 and MCP87022 N-Channel MOSFET

The MCP87050 and MCP87022 is an N-Channel power MOSFET in a popular PDFN 5 mm x 6 mm package. Advanced packaging and silicon processing technologies allow devices to achieve a low QG for a given RDS(on) value, resulting in a low Figure of Merit (FOM). Combined with low RG, the low FOM of the devices allow high-efficiency power conversion with reduced switching and conduction losses.

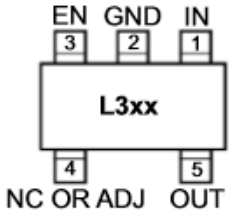
Figure 7-4. MCP87050 and MCP87022



7.1.5 MIC5233-5.0YM5 and MIC5233-3.3YMT LDO

The MIC5233 is an 100 mA, highly accurate, Low Dropout Regulator (LDO) with high-input voltage and ultra-low ground current. This combination of high-voltage and low-ground current makes the MIC5233 ideal for multi-cell Li-Ion battery systems. In a µCap LDO design, the MIC5233 is stable with either ceramic or tantalum output capacitors. It only requires a 2.2 µF output capacitor for stability. The features of the MIC5233 include enable input, thermal shutdown, current limit, reverse battery protection, and reverse leakage protection. Available in fixed and adjustable output voltage versions, the MIC5233 is offered in the SOT23-5 and SOT223-3 packages with a junction temperature range of -40°C to +125°C.

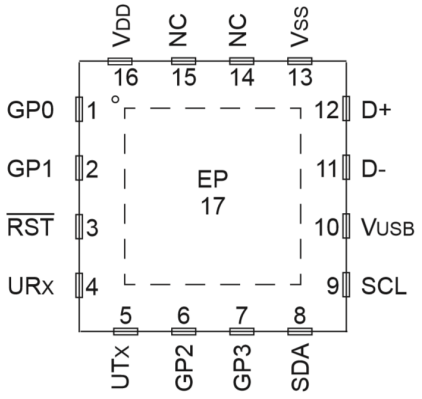
Figure 7-5. MIC5233



7.1.6 MCP2221A USB-to-UART/I²C Serial Converter

The MCP2221A is a USB-to-UART/I²C serial converter which enables USB connectivity in applications that have UART and I²C interfaces. The device reduces external components by integrating the USB termination resistors and the oscillator needed for USB operation. MCP2221A has four GP pins providing miscellaneous functionalities (GPIO, USBCFG, SSPND, Clock Output, ADC, DAC, interrupt detector).

Figure 7-6. MCP2221A



7.2 Appendix B: PCMC Test Point Measurements

Figure 7-7. Test Points: PWM_HS, PWM_LS, C1INJ, VOUT at VIN = 9V, LOAD = 2A

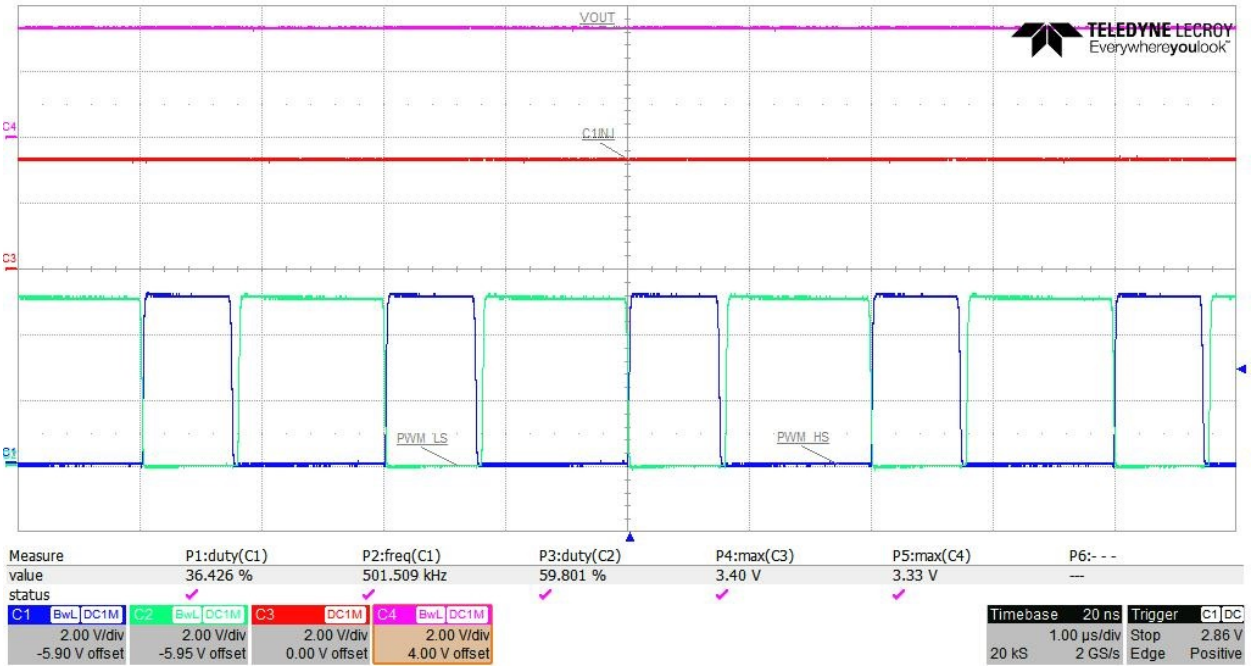


Figure 7-8. Test Points: PWM_HS, C2INJ, DCR_CS, CT_CS at VIN = 9V, LOAD = 2A

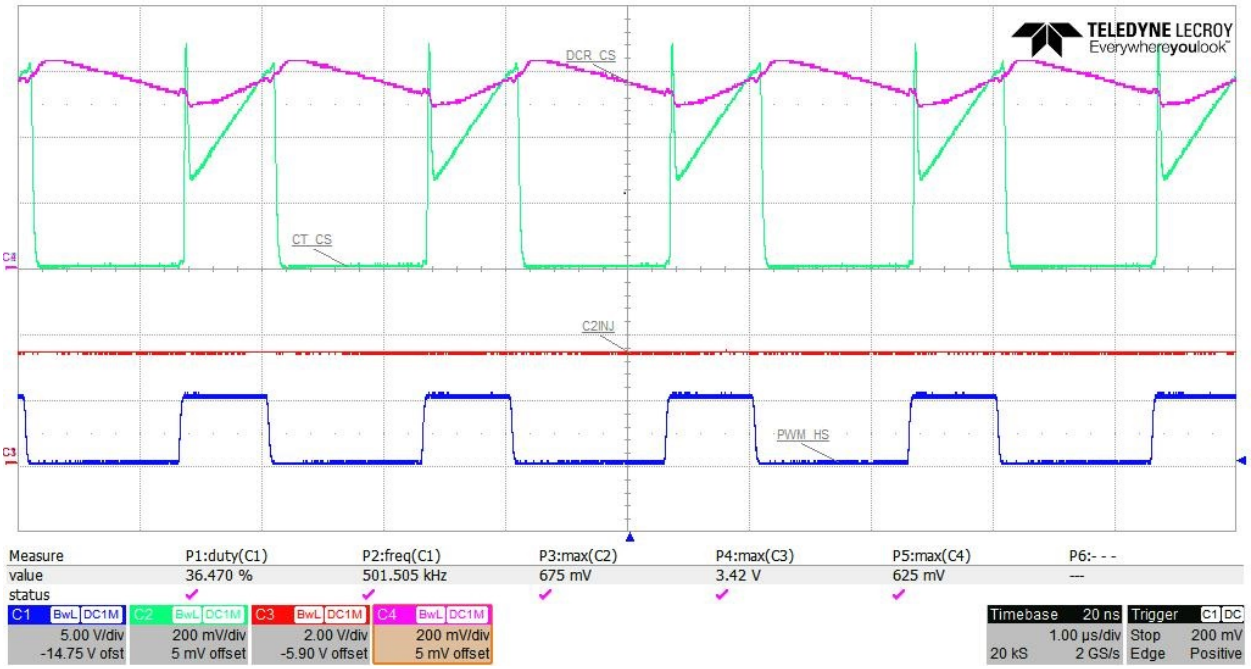


Figure 7-9. Test Points: VOUT, SW_NODE, GATE_H, GATE_L at VIN = 9V, LOAD = 2A

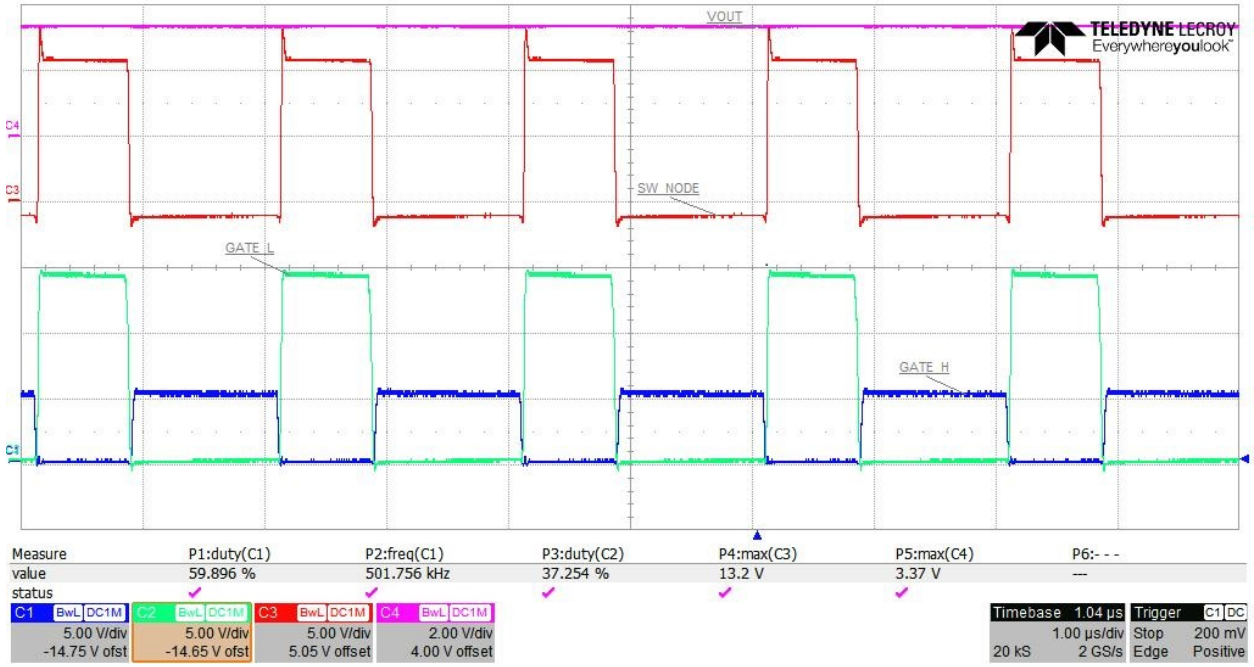
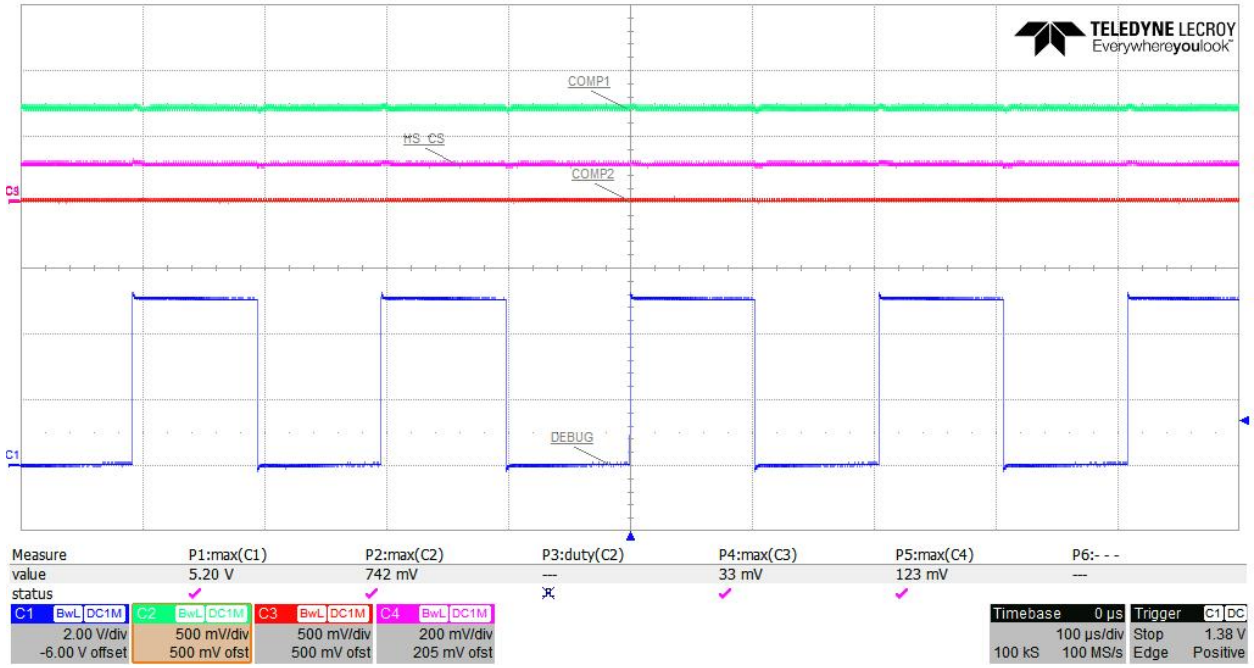


Figure 7-10. Test Points: COMP1, COMP2, HS_CS, DEBUG at VIN = 9V, LOAD = 2A



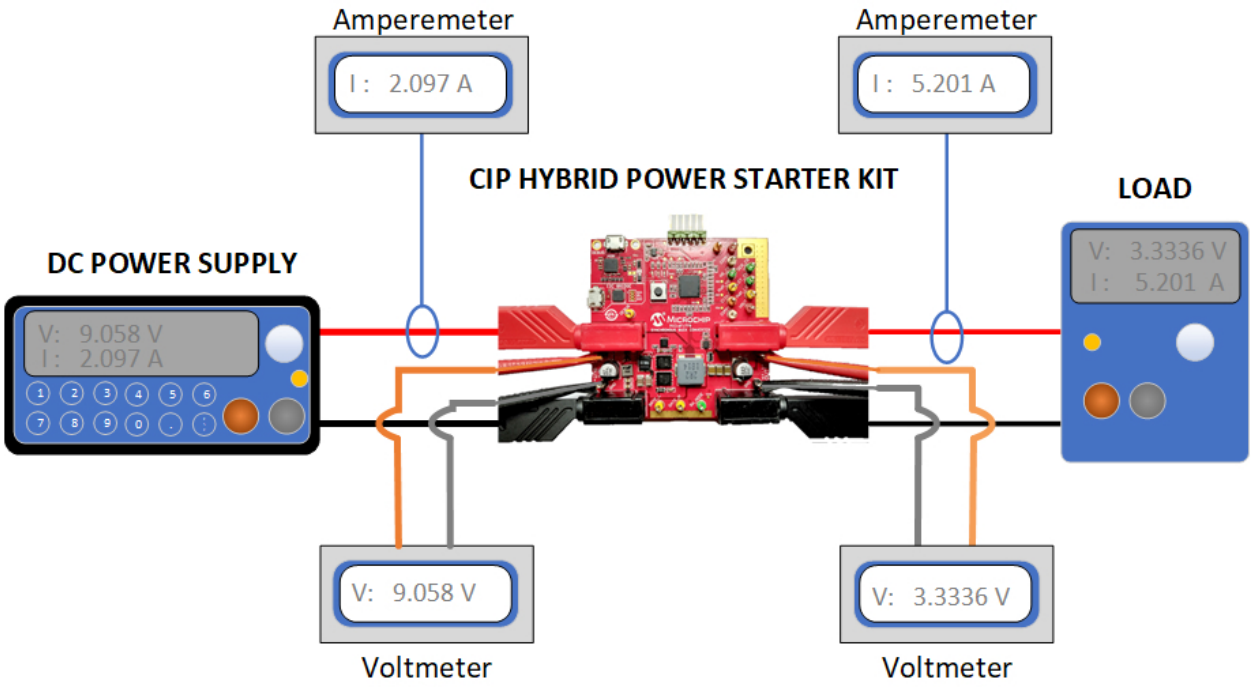
Note: The debug test point signal is a software coded scheduler in the firmware.

7.3 Appendix C: Efficiency, Line Regulation and Load Regulation in PCMC

7.3.1 Efficiency Measurements

For accurate measurements of the efficiency at varying load conditions, monitor the actual VIN and VOUT across the capacitor from the available test point VIN and test point VOUT.

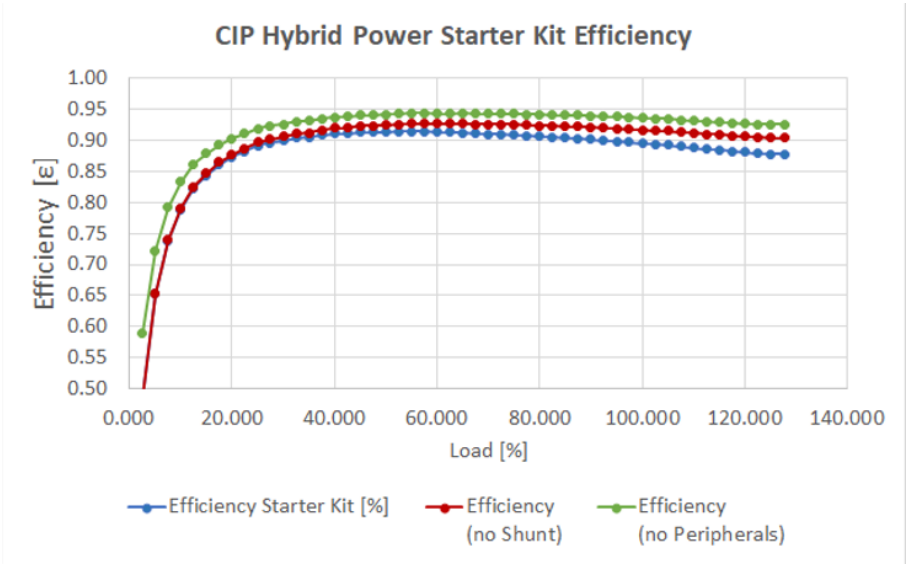
Figure 7-11. Efficiency Test Setup



The efficiency measurements are recorded in the graph below. Each line color represents different test cases for measuring efficiency on the CIP Hybrid Power Starter Kit.

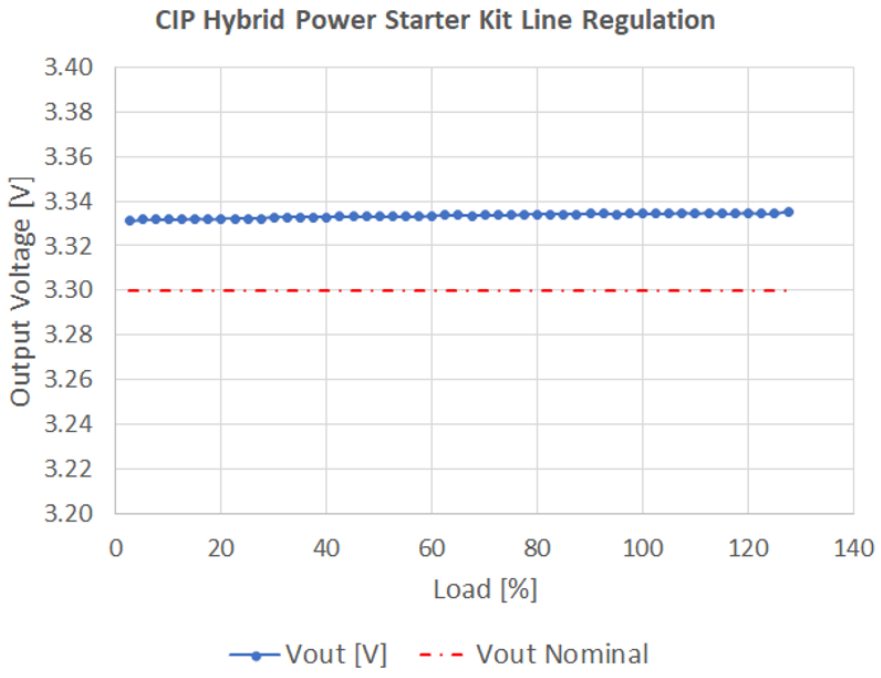
1. The blue line shows the total efficiency of the CIP Hybrid Power Starter Kit with the power LED1 on, test LED2 and LED3 off, and the on-board debugger connected.
2. The red line shows efficiency without the high-side sense shunt resistor.
3. The green line shows the efficiency of the power train and controller section without the on-board debugger and the high-side shunt resistor.

Figure 7-12. Efficiency Measurements



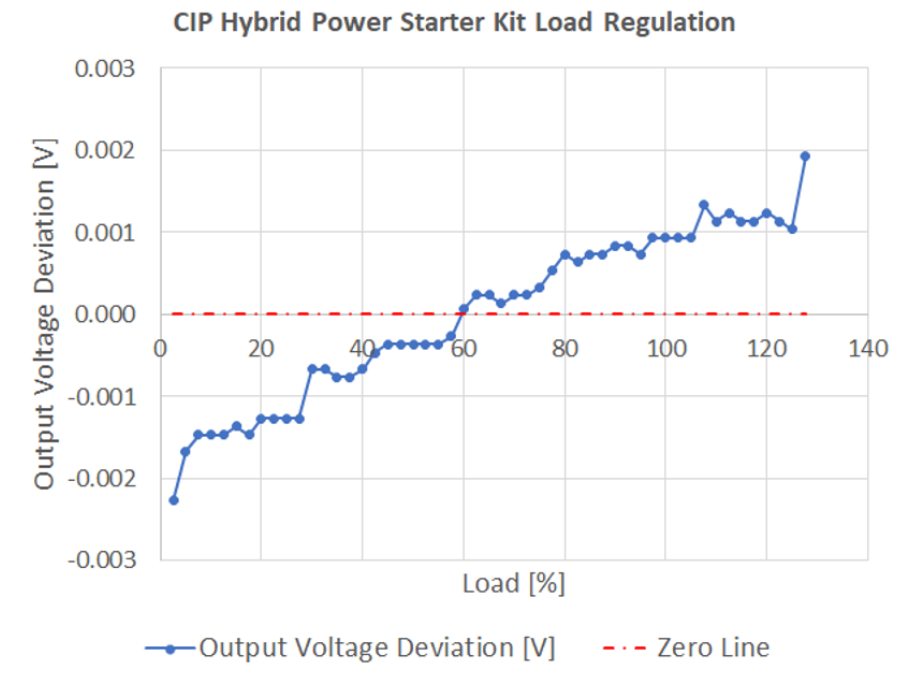
7.3.2 Line Regulation

Figure 7-13. Line Regulation Measurements



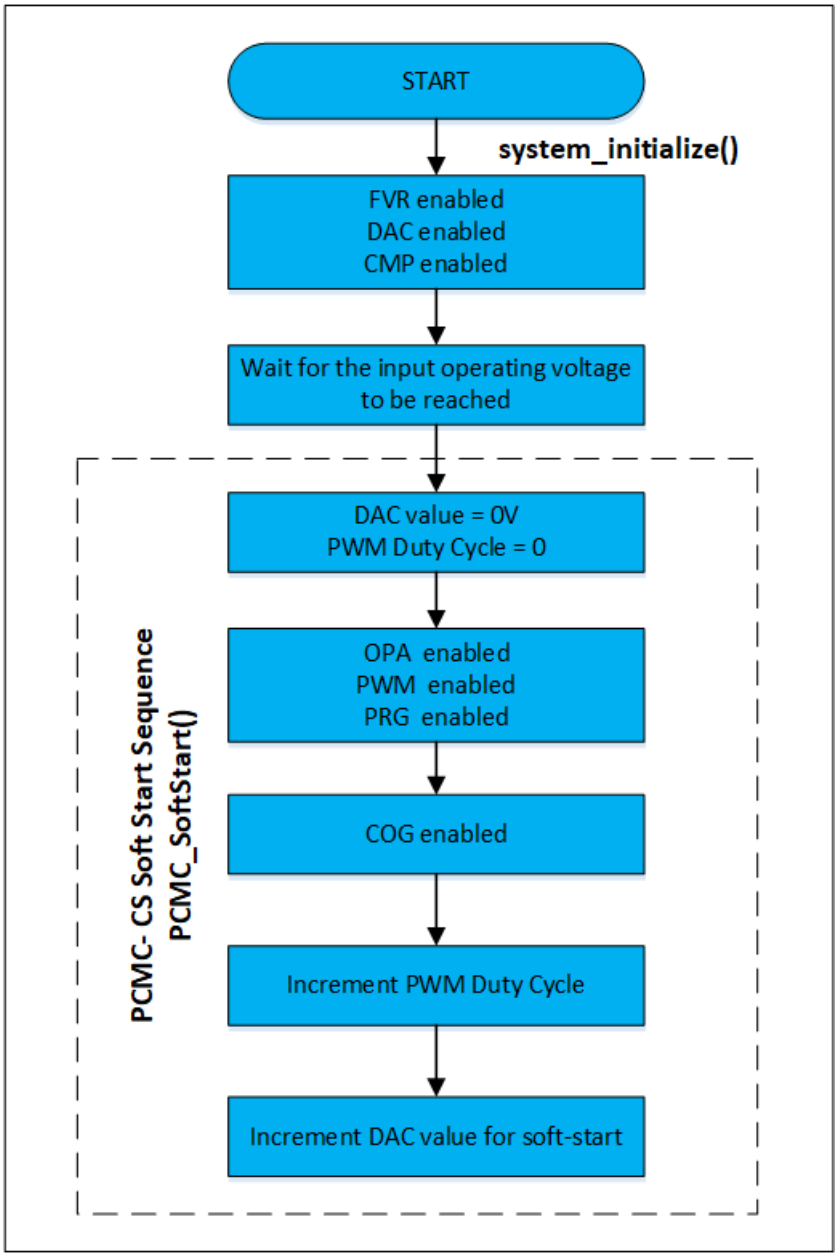
7.3.3 Load Regulation

Figure 7-14. Load Regulation Measurements



7.4 Appendix D: Firmware Flowchart

Figure 7-15. PCMC-CS Firmware Flowchart



7.5 Appendix E: Bode 100 Gain/Phase Measurement Test Setup

The following figures show the general test setup for measuring Plant, Compensator and Loop Gain using Bode 100. Note that the PCMC and VMC configurations have different signal injection and measurement test points.

Figure 7-16. Plant Measurement Test Setup

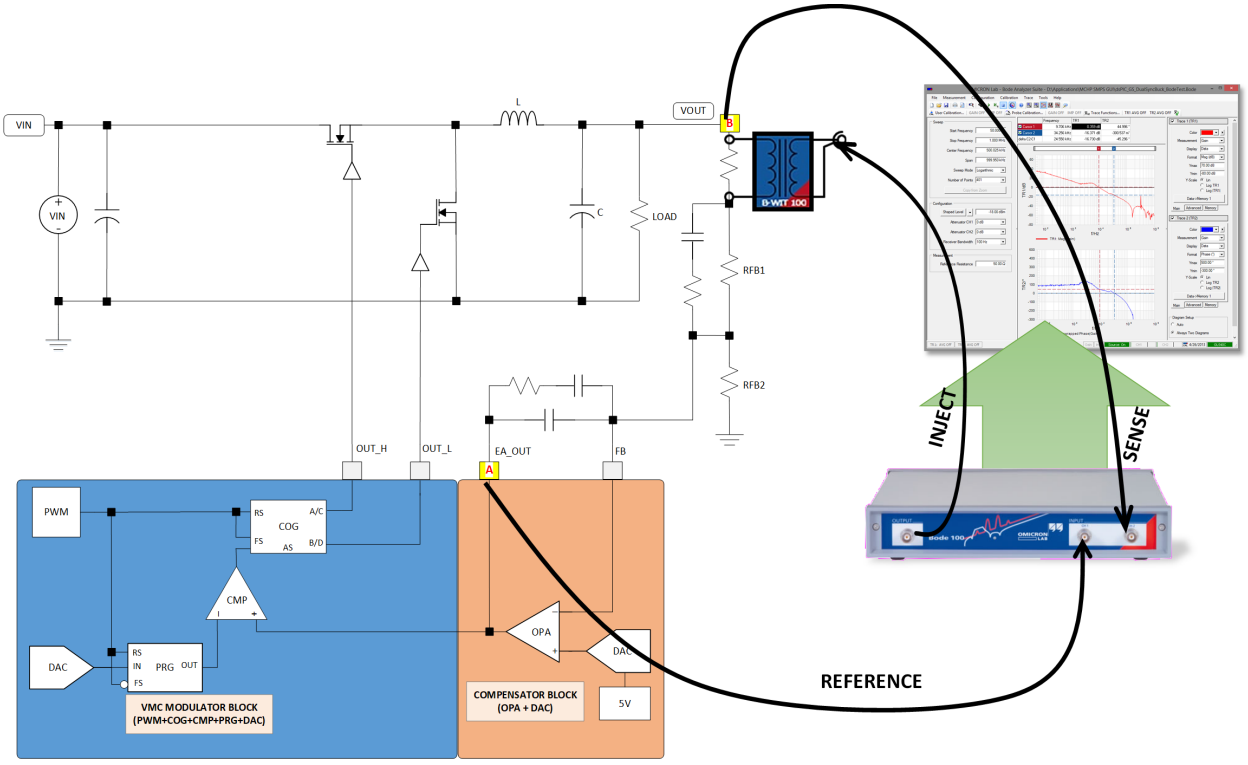


Figure 7-17. Compensator Measurement Test Setup

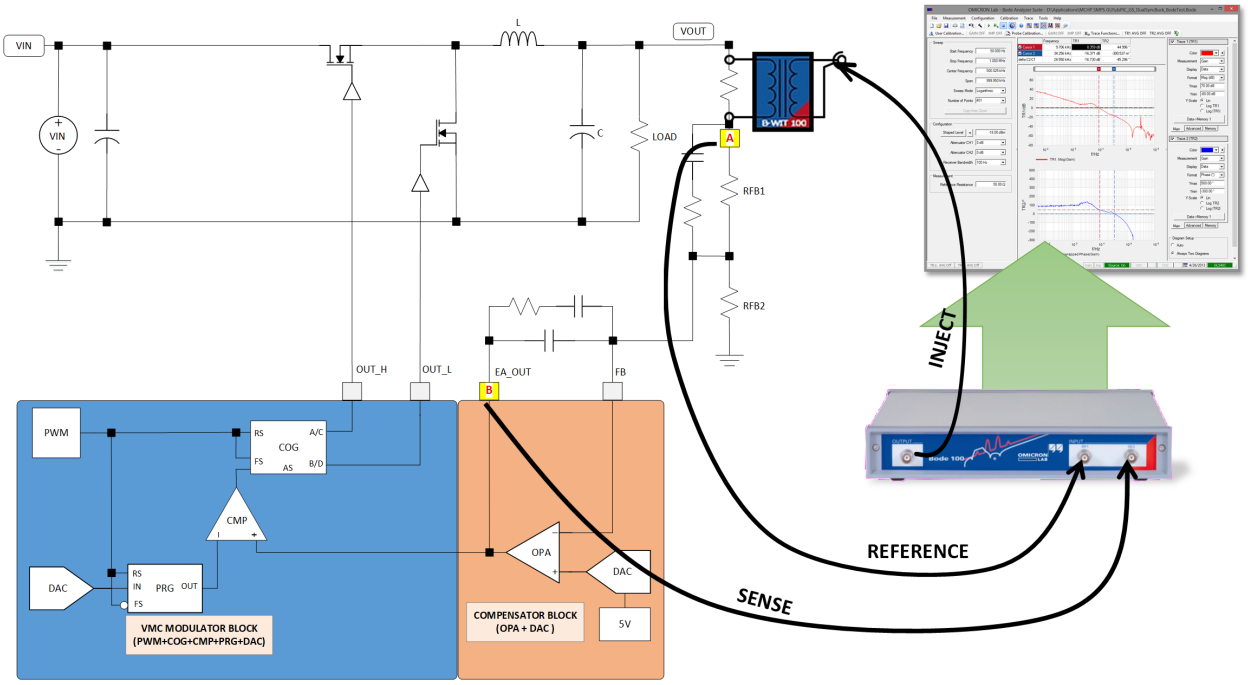
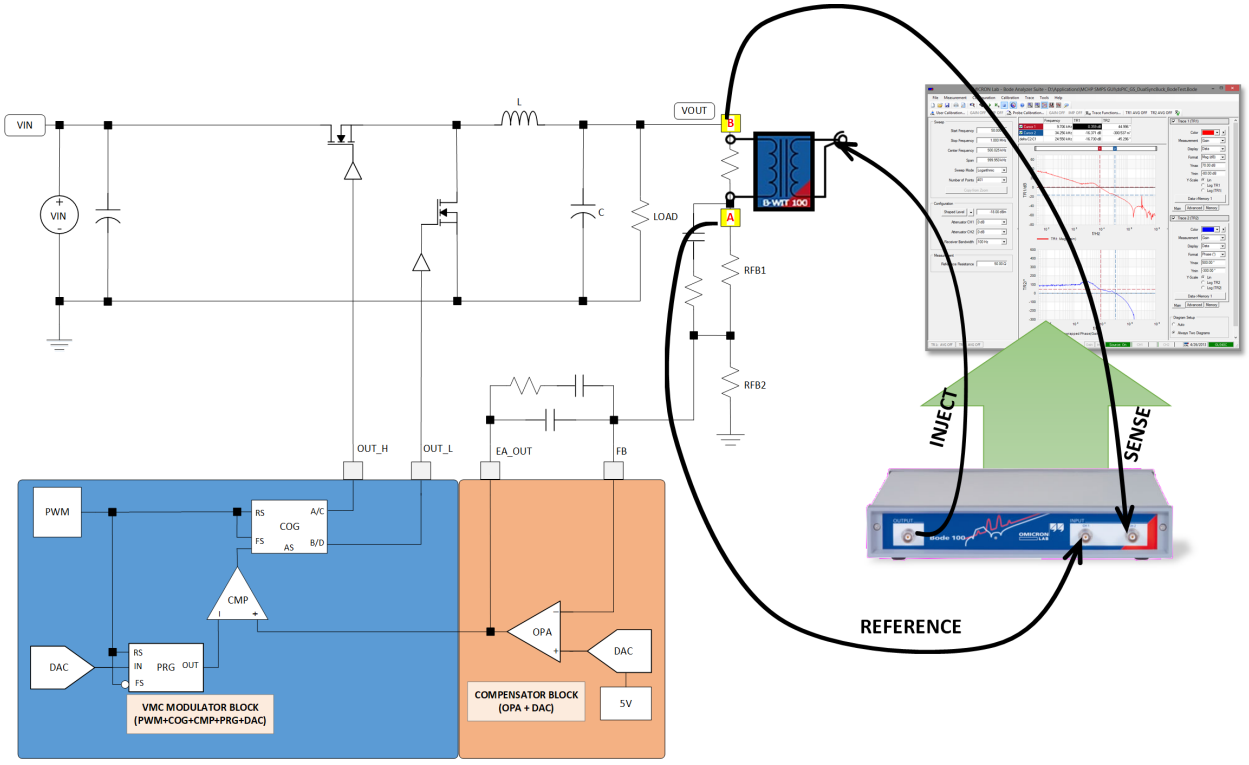


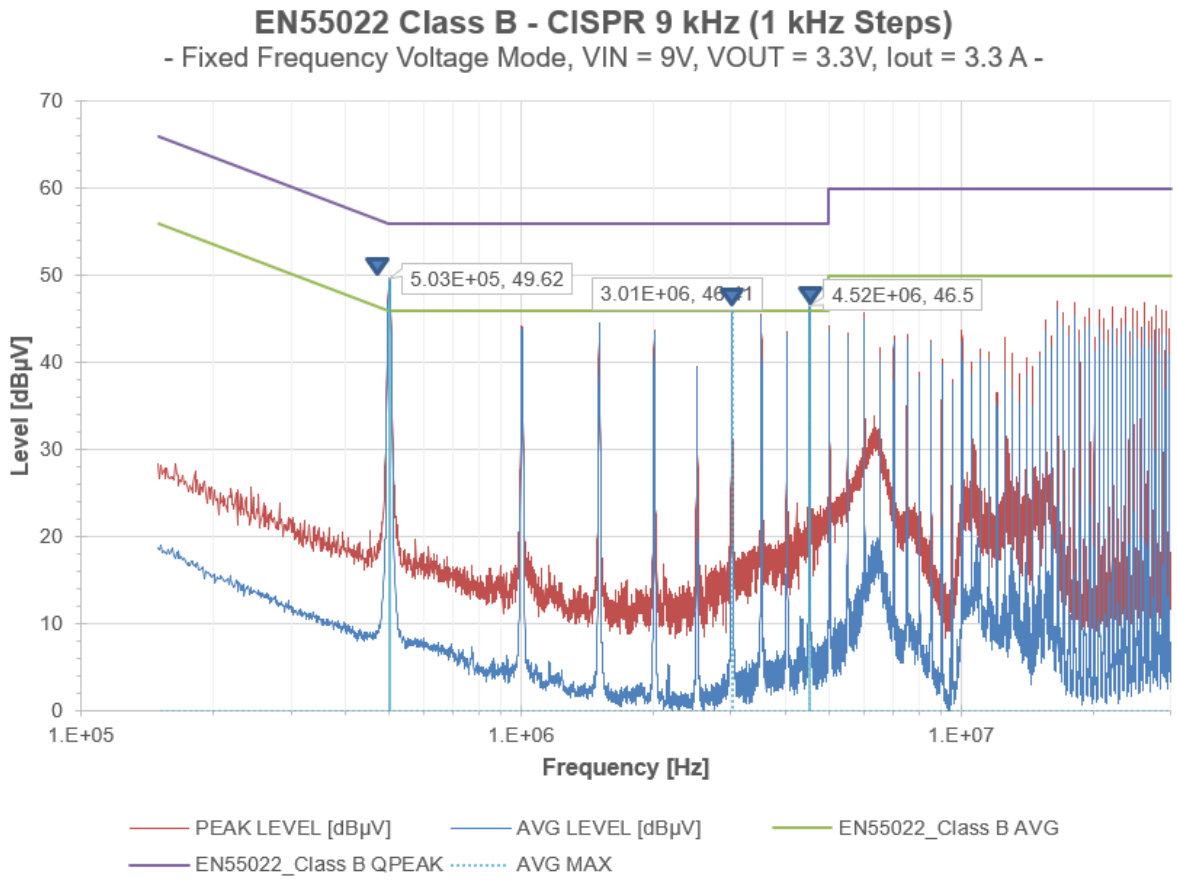
Figure 7-18. Loop Gain Measurement Test Setup



7.6 Appendix F: Pre-Compliance Conducted Noise Measurement

The Conducted EMI measurement plot of the CIP Hybrid Power Starter Kit is shown in the figure below.

Figure 7-19. Conducted EMI Measurement



7.7 Appendix G: Power Supply Design Considerations

This development board was designed as an experimental platform for users interested in exploring the capabilities and the development procedures used for designing with PIC16F176x/177x CIP Hybrid Power Controllers. Thus, the fairly conventional synchronous buck converter topology has been enhanced with additional options and features to meet this key objective. However, some of the added features may not be ideal for a real-world design. Some of the limitations introduced by these trade-offs are described below.

Current sensing

This buck converter is equipped with three different inductor current sense options:

- Current Sense Transformer CT
- Inductor DC Resistance Sensing Circuit DCR
- High-Side Shunt Amplifier HS

In a production design, only one of the above would be used. However, different current sense methods have different characteristics like different signal-to-noise ratios, phase delays or limited bandwidth which can have significant influence on the overall performance of the final design. The PIC16F1779 family of devices offers various freely configurable hardware features to compensate for specific shortcomings like phase delays or nonlinear feedback signals, which are demonstrated in example projects.

While DCR sensing is transparent and does not influence the operation of the buck converter, the high-side shunt resistor and the current sense transformer feedback circuits introduce the following limitations:

Current sense transformer feedback

The current sense transformers are very common in mid- and high-voltage designs where isolated feedback paths are required, such as power factor correction stages in AC/DC offline converters. To allow users to evaluate the tuning capabilities of specific IC features like leading edge blanking and to establish stable feedback loops by incorporating chopped feedback waveforms, a current sense transformer was also added to the CIP Hybrid Power Starter Kit. Although this feedback circuit is working well and reliably, it introduces a dominant noise source in this specific buck converter design, which results in dominant spikes in the conducted emissions spectrum (see the test results in Appendix F), and therefore may not be considered as a template for a real-world design of a buck converter.

High-Side Shunt Resistor Feedback

In addition to the CT feedback source, a high-side shunt resistor R1 of 10 mΩ was placed between L1 and the output capacitors C3, C4, C5, C7 and C42. This shunt resistor has significant influence on the efficiency of the power supply (see the test results in Efficiency Measurements figure in Appendix C) and slightly deforms the output voltage ripple due to the changing forward voltage drop across the shunt resistor dependent on the load current. In conjunction with the MCP6C02-020 high-side shunt amplifier having a fixed gain of 20, this current sense signal has an equal current feedback gain as the current sense transformer circuit of 5 A/V, to allow users to seamlessly switch between both signal sources, without having to change any additional feedback component on the board.

The high-side shunt current sense signal is routed to an alternate peak current feedback input pin where additional PIC16F1779 device configurations can be evaluated accounting for the phase-shifted, lower bandwidth signal waveform.

The high-side shunt current feedback signal is also routed to a separated error amplifier input, where it can be compensated using a type II or type III RC compensation network. By changing the PIC16F1779 device configuration accordingly, this average current feedback can be:

- Put in series with an outer voltage feedback loop to form an inner average current loop of a constant voltage source (common battery charger control system);
- Used independently as single average current control loop in a constant current source;
- Used as outer average current loop in conjunction with an inner peak current loop in a constant current source (common LED driver control system).

Note: The components of the average current compensation network have not been populated by default. The component values highly depend on the use case and may differ significantly based on the chosen type of feedback loop structure.

DCR Sense Feedback

Using inductor DC resistance sensing for generating an inductor peak current feedback signal is common practice in low-voltage, high-current designs. This current sensing options is popular as it does not directly affect the operation of the converter and also does not introduce additional sources for noise or losses like other sensing techniques. However, the signal size depends on the DC resistance of the inductor. Thus, high-current, high-efficiency DCR designs often suffer from poor signal noise ratio and, as the signal is produced by an RC filter only, also is often not very linear and distorted. Yet again, the highly flexible peripherals of PIC16F1779 allow users to experiment with various options to account for these shortcomings and help to optimize the overall performance of systems using DCR sensing as inductor current feedback.

Furthermore, as the DCR sensing method is also very cost effective by incorporating only a very small number of passive components, an on-chip amplifier is used to condition the feedback signal, showcasing further ways of how power supply designs can be optimized by utilizing PIC16F1779 features.

Input Filter

The synchronous buck converter is equipped with a small PI filter at its input to reduce incoming noise injected by attached DC sources. However, the filter design may only be partly sufficient to suppress conducted noise generated by the CIP Hybrid Power Starter Kit itself, depending on the cables and connections used. One of the major noise sources is the current sense transformer circuit described above. For this design, this trade-off was solved in advantage of the usability and value for the experimental evaluation process rather than providing a real-world design template meeting emission standards.

Main Inductor L1 Footprint

The inductor L1 component solder pads available on the CIP Hybrid Power Starter Kit have been shaped to allow users exchanging the main inductor against different components for experimental purposes. These pads support footprints for SMT inductors within the same power range of major inductor vendors.

The main inductor populated by default is composed of a compound material incorporating iron-powder and ferrite materials in a specific ratio to achieve low inductance derating overload current up to the nominal current rating while still having a relatively soft saturation characteristic at the same time. The DC-resistance was selected to be in a range of 5-10 mΩ for an optimized DCR sensing feedback signal size.

Output Bulk Capacitor C2 Footprint

The output bulk capacitor C2 solder pads available on the CIP Hybrid Power Starter Kit have been shaped to allow users exchanging the output bulk capacitor against different components for experimental purposes. These pads support footprints for SMT capacitors of major capacitor vendors.

High-Speed Switch Node

The half-bridge switch node of this synchronous buck converter is composed of a high-side MOSFET MCP87050 with less gate charge (Q_g) but slightly higher on-resistance ($R_{DS(on)}$) and a low-side MOSFET MCP87022 with higher gate charge (Q_g) and lower on-resistance ($R_{DS(on)}$) to account for the shared power losses in the nominal operating conditions at approx. 25-35% duty ratio. Microchip's MCP87xxx family of Power MOSFETs are high-speed Si-MOSFETs with rise and fall times with less than 5 ns when driven by an appropriate high-speed FET driver like MCP14700.

Please read the AN1471 - Efficiency Analysis of a Synchronous Buck Converter using Microsoft Office Excel-Based Loss Calculator application note for further information.

In the CIP Hybrid Power Starter Kit the switching edges were slowed down with the penalty of higher switching losses to account for the negative impact of the parasitic inductance introduced by the primary winding of the current sense transformer. This inductance results in a voltage overshoot when the high-side switch is closed. This switching spike is also clearly visible in the conducted emissions test results.

Although using a low-inductance current sense transformer and test results are still within a reasonable range to meet EN55022 Class B, it is recommended to take special care of a short and tight loop with minimum parasitic inductances between the input capacitors and half-bridge MOSFETs to achieve optimum results when migrating this switch node to custom designs.

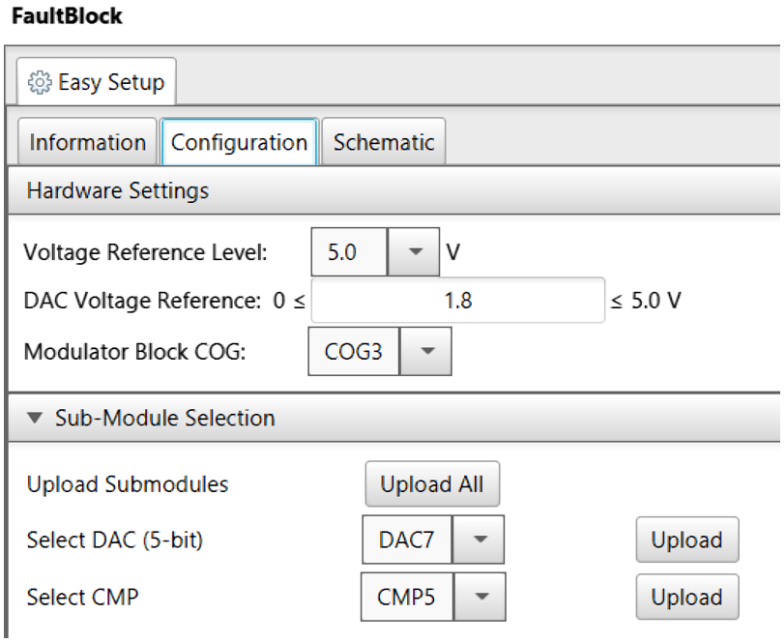
7.8 Appendix H: Additional Configuration for Fault Detection

The PCMC-CS and VMC Closed Loop configurations can be modified to add fault detection through the FaultBlock. The FaultBlock uses multiple combinations of analog comparators (CMP), 5-bit DAC and the internal FVR peripherals. Note that any CMP that is selected on the FaultBlock must be compatible with the COG auto-shutdown source (AS). The CMP that is already used in the Modulator Blocks can no longer be used. The selected 5-bit DAC module must be compatible with the selected CMP.

7.8.1 Adding Output Overvoltage Protection (OVP) in PCMC

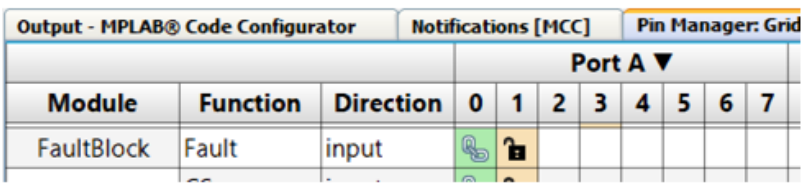
1. Open the PCMC Configuration created from the MCC SMPS Library.
2. From the Device Resources, go to CIP Blocks, and click **FaultBlock** to add it to the Project Resources area.
3. Click **FaultBlock** on the Project Resources to open the settings.
4. Set the Voltage Reference Level of the DAC to 5V.
5. The DAC output sets the DAC Voltage Reference to be used for OVP. Setting this to 1.8V gives an OVP of 3.6V due to the equal resistors on the voltage divider network at the voltage output terminal.
6. In the submodule selection, select CMP5 since this is compatible with the auto-shutdown source of the COG3 used in the PWM Controller Block 3 in **ModulatorBlockPCMC**.
7. Select DAC7 since this is compatible with the CMP5 positive input. Click **Upload All**.

Figure 7-20. FaultBlock Settings in PCMC

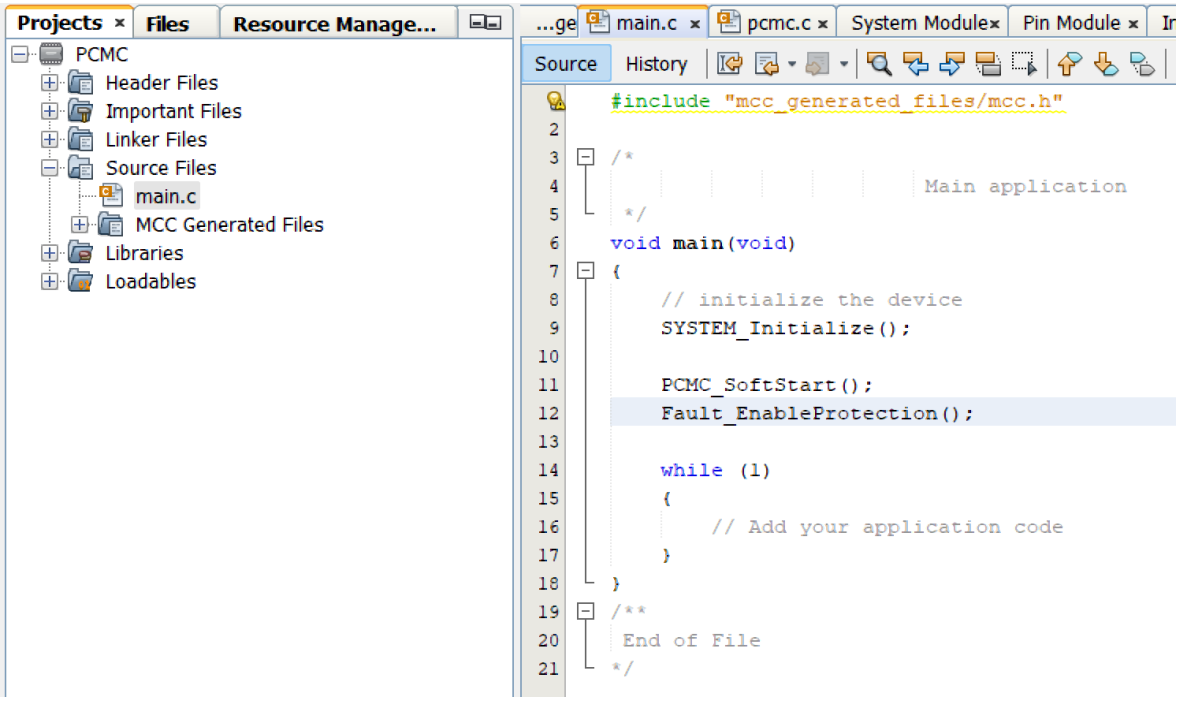


8. On the pin manager, set RA0 as the FAULT pin. Click **Generate Code**.

Figure 7-21. Pin Assignment of Fault Signal

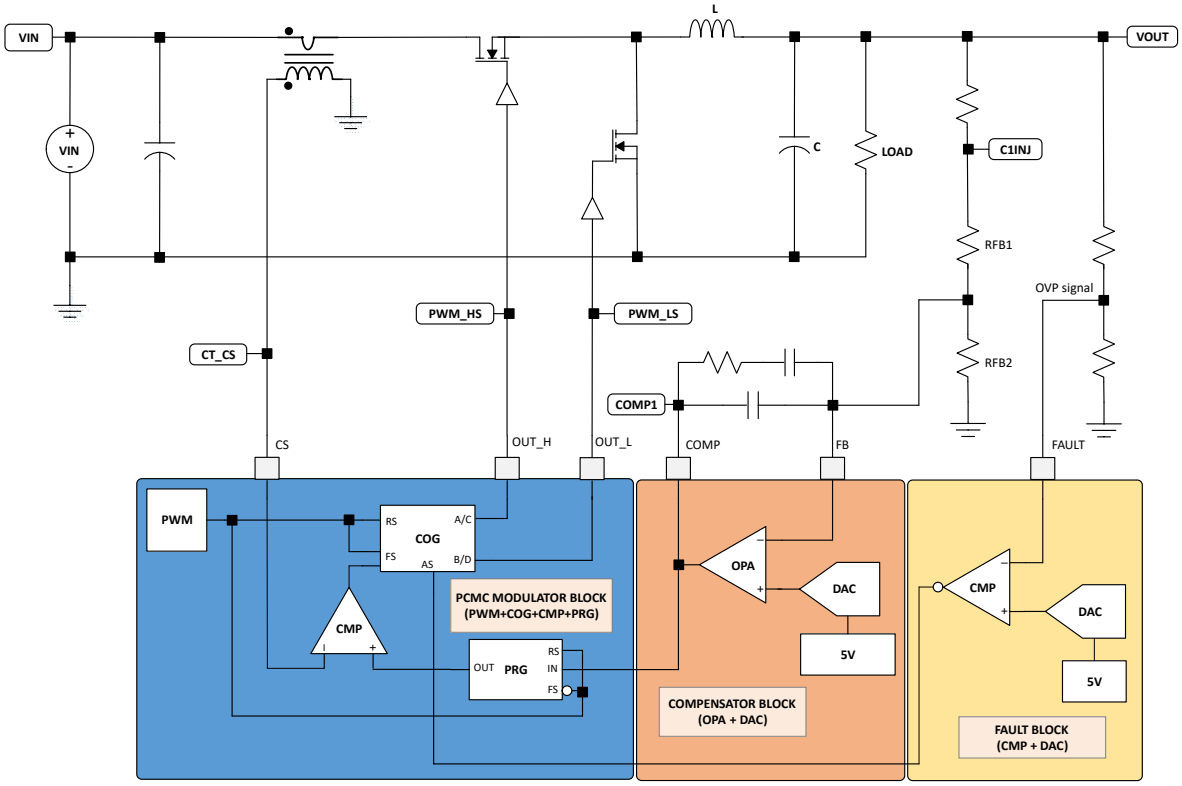


9. To enable fault protection, add on `main.c` the line of code `Fault_EnableProtection();`.



10. The board has now overvoltage protection in PCMC mode.

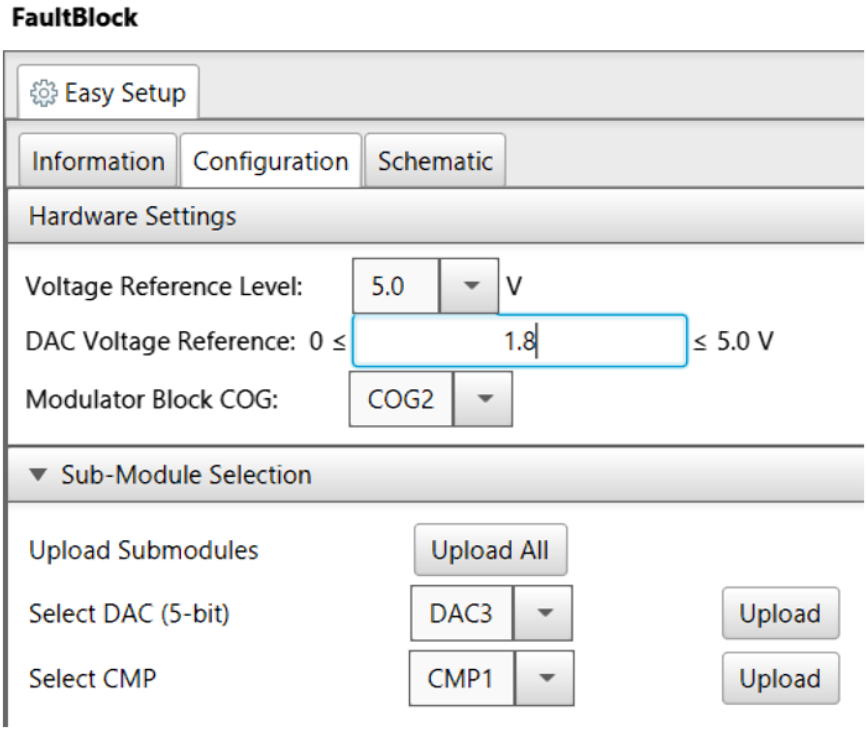
Figure 7-22. Added OVP Detection in PCMC



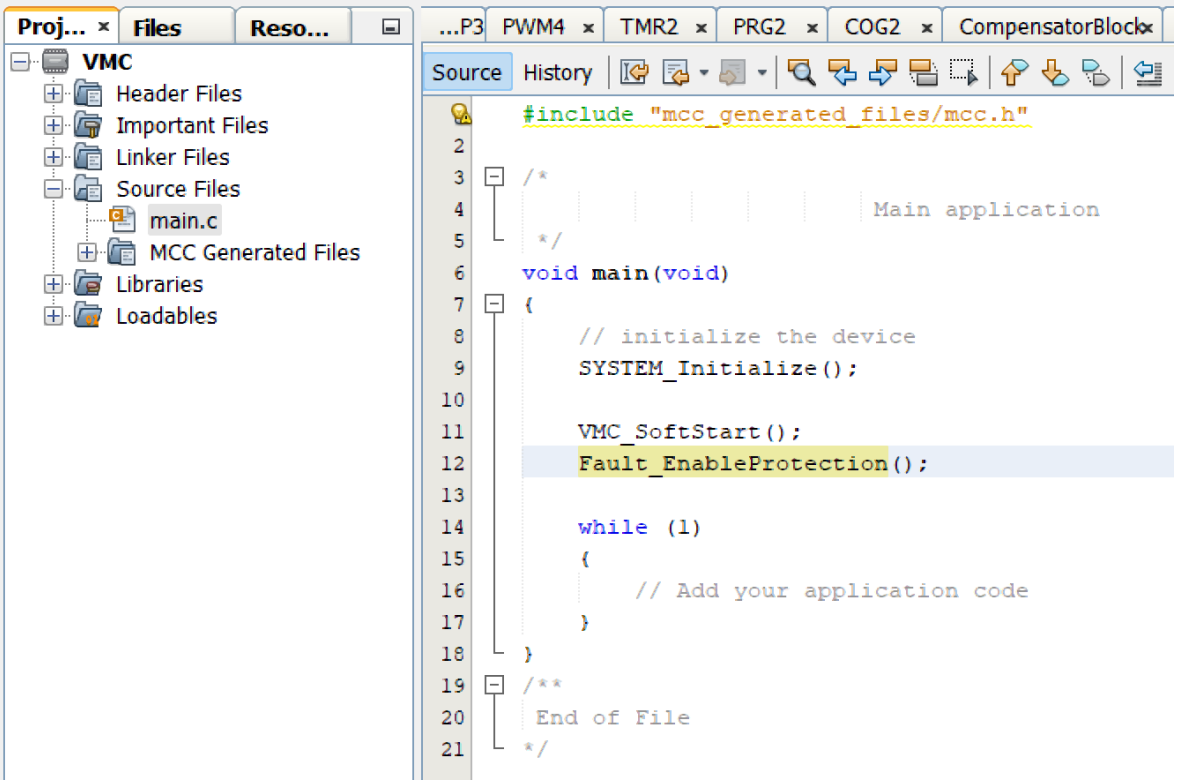
7.8.2 Adding Output Overvoltage Protection (OVP) in VMC

1. Open the VMC Configuration created from the MCC SMPS Library.
2. From the Device Resources, go to CIP Blocks, and click **FaultBlock** to add it to the Project Resources area.
3. Click **FaultBlock** on the Project Resources to open the settings.
4. The DAC output sets the DAC Voltage Reference to be used for OVP. Setting this to 1.8V gives an OVP of 3.6V due to the equal resistors on the voltage divider network at the voltage output terminal.
5. In the submodule selection, select CMP1 since this is compatible with the auto-shutdown source of the COG2 used by the PWM Controller Block 2 in the **ModulatorBlockVMC**.
6. Select DAC3 since this is compatible with CMP1 positive input. Click **Upload All**.

Figure 7-23. FaultBlock Settings in VMC

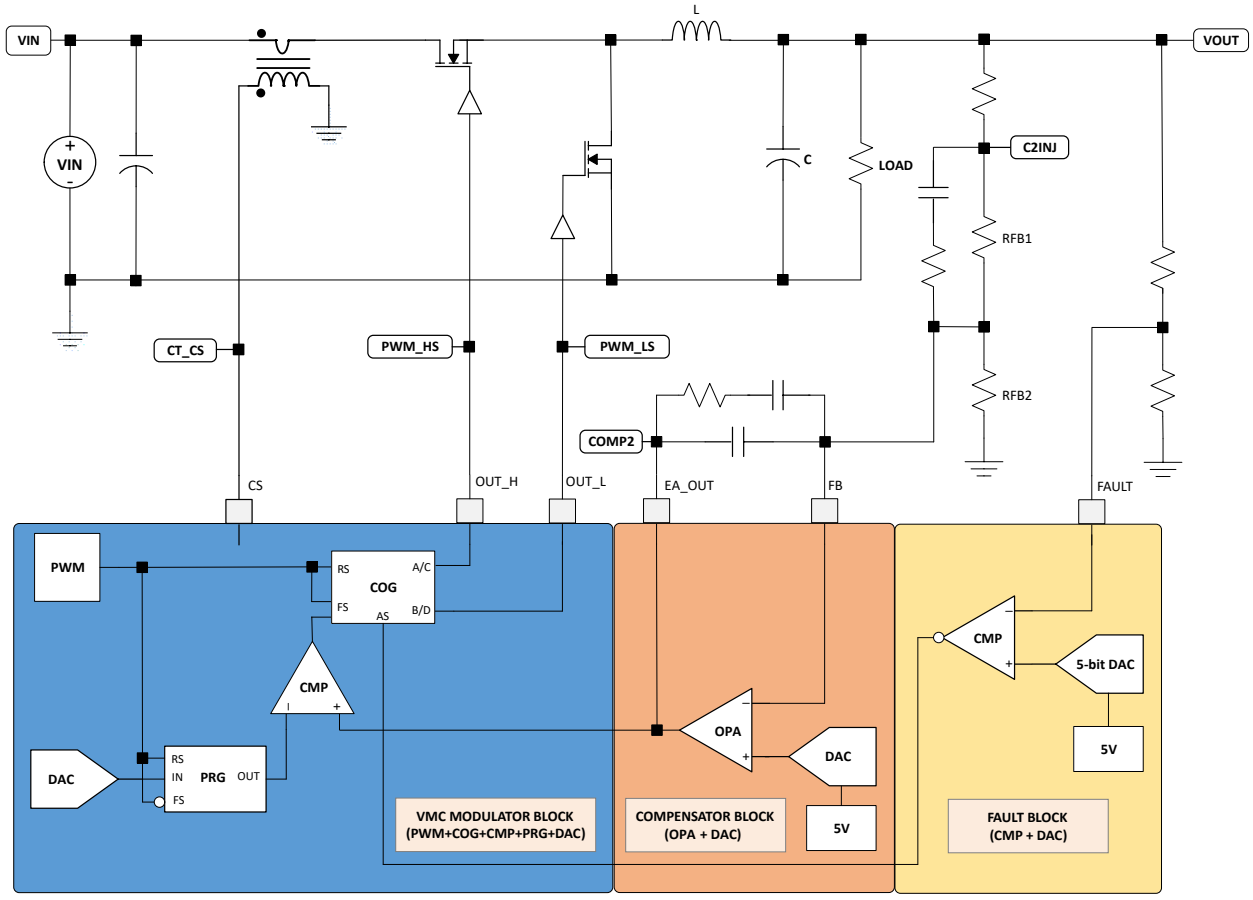


7. On the pin manager, set RA0 as the FAULT pin. Click **Generate Code**.
8. To enable fault protection, add on `main.c` the line of code `Fault_EnableProtection();`.



9. The board has now overvoltage protection in VMC mode.

Figure 7-24. Added OVP Detection in VMC



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ISBN: 978-1-5224-3997-4

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