

MOSFET - Power, Single N-Channel, PQFN8

100 V, 10.8 mΩ, 83 A

Product Preview

NTMFS010N10G

Features

- Wide SOA for Linear Mode Operation
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- High Peak UIS Current Capability for Ruggedness
- Small Footprint (5x6 mm) for Compact Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- 48 V Hot Swap System, Load Switch, Soft Start, E-Fuse

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	100	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	I_D 83 A
		$T_C = 100^\circ\text{C}$	I_D 58 A
Power Dissipation $R_{\theta JC}$ (Note 2)		$T_C = 25^\circ\text{C}$	P_D 150 W
		$T_C = 100^\circ\text{C}$	P_D 75 W
Continuous Drain Current $R_{\theta JA}$ (Note 1, 2)	Steady State	$T_C = 25^\circ\text{C}$	I_D 11 A
		$T_C = 100^\circ\text{C}$	I_D 8 A
Power Dissipation $R_{\theta JA}$ (Note 1, 2)		$T_C = 25^\circ\text{C}$	P_D 3 W
		$T_C = 100^\circ\text{C}$	P_D 1.5 W
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	I_{DM} 1247	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	125	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{AV} = 38.8 \text{ A}$, $L = 0.3 \text{ mH}$)	E_{AS}	226	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

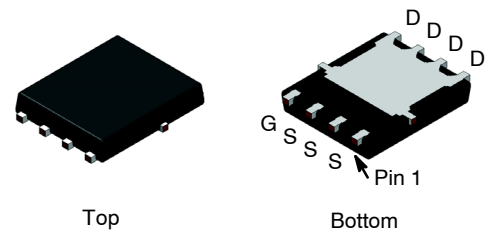
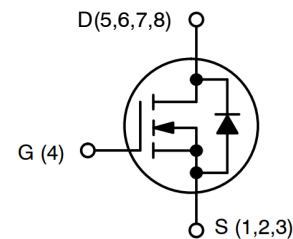


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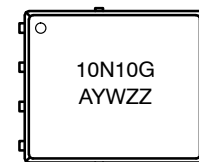
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	10.8 mΩ @ 10 V	83 A

N-Channel MOSFET



PQFN8 5x6
(Power 56)
CASE 483AE

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State	1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State	50	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
$V_{(BR)DSS} / T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, ref to 25°C		87.9		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		100	
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 164\ \mu\text{A}$	2.0	3.0	4.0	V
$V_{GS(TH)} / T_J$	Negative Threshold Temperature Coefficient	$I_D = 164\ \mu\text{A}$, ref to 25°C		-9.2		mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 31\text{ A}$		8.6	10.8	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 31\text{ A}$		21		S
R_G	Gate-Resistance	$V_{GS} = 0\text{ V}, f = \text{MHz}$		0.52		Ω

CHARGES & CAPACITANCES

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		3950		pF
C_{OSS}	Output Capacitance			430		
C_{RSS}	Reverse Transfer Capacitance			60		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 31\text{ A}$		58.5		nC
Q_{GS}	Gate-to-Source Charge			22		
Q_{GD}	Gate-to-Drain Charge			14		
Q_{OSS}	Output Charge	$V_{GS} = 0\text{ V}, V_{DD} = 50\text{ V}$		41		

SWITCHING CHARACTERISTICS (Note 3)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 31\text{ A}, R_G = 4.7\ \Omega$		23		ns
t_r	Rise Time			14		
$t_{d(OFF)}$	Turn-Off Delay Time			34		
t_f	Fall Time			9		

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 31\text{ A}$	$T_J = 25^\circ\text{C}$		0.83	1.2	V
			$T_J = 125^\circ\text{C}$		0.7		
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, dI_S/dt = 300\text{ A}/\mu\text{s}, I_S = 15\text{ A}$		36		ns	
Q_{RR}	Reverse Recovery Charge			147		nC	
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, dI_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 15\text{ A}$		24		ns	
Q_{RR}	Reverse Recovery Charge			288		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

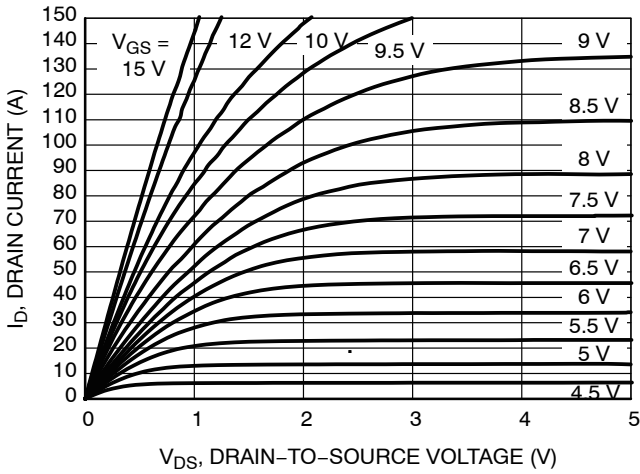


Figure 1. On-Region Characteristics

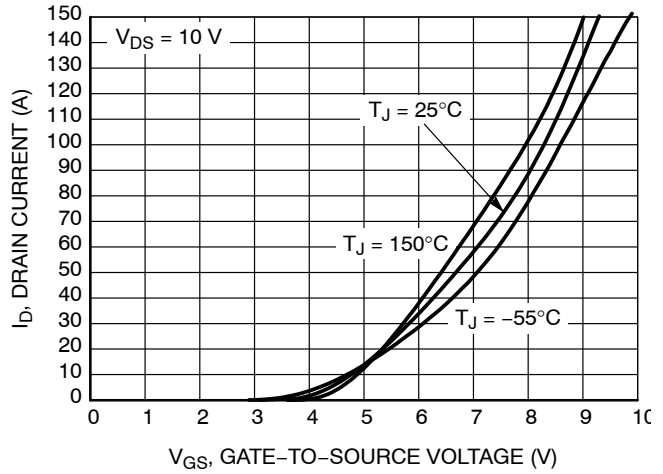


Figure 2. Transfer Characteristics

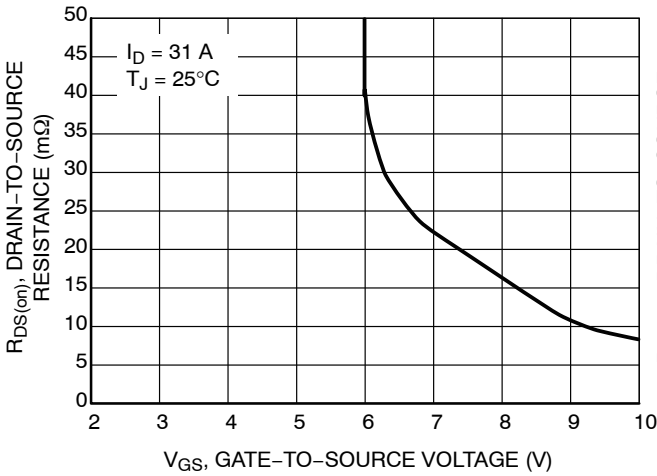


Figure 3. On-Resistance vs. Gate-to-Source Voltage

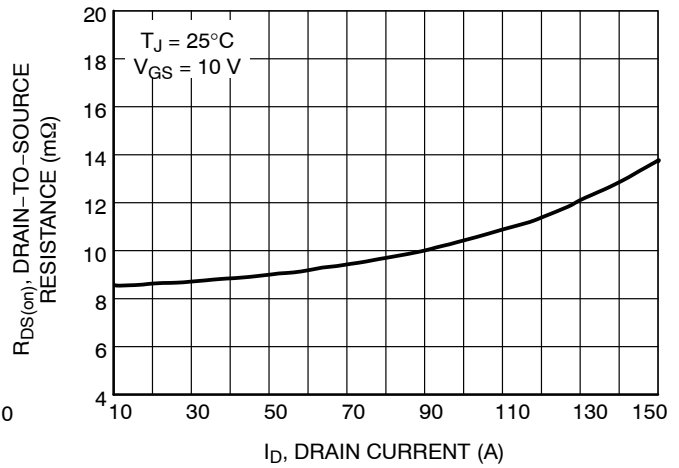


Figure 4. On-Resistance versus Drain Current and Gate Voltage

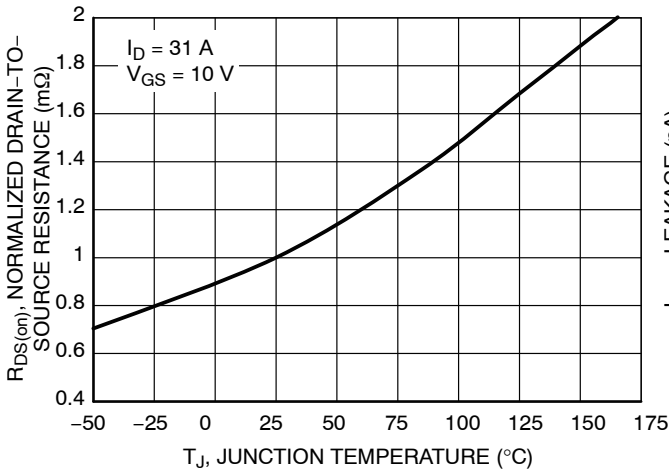


Figure 5. On-Resistance Variation with Temperature

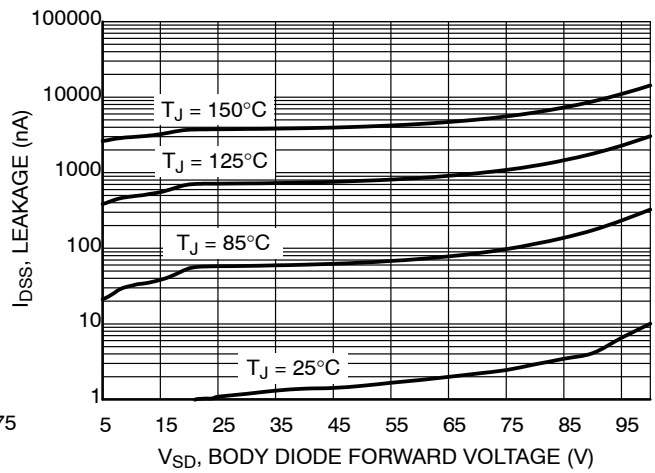


Figure 6. Drain-to-Source Leakage Current versus Voltage

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TYPICAL CHARACTERISTICS

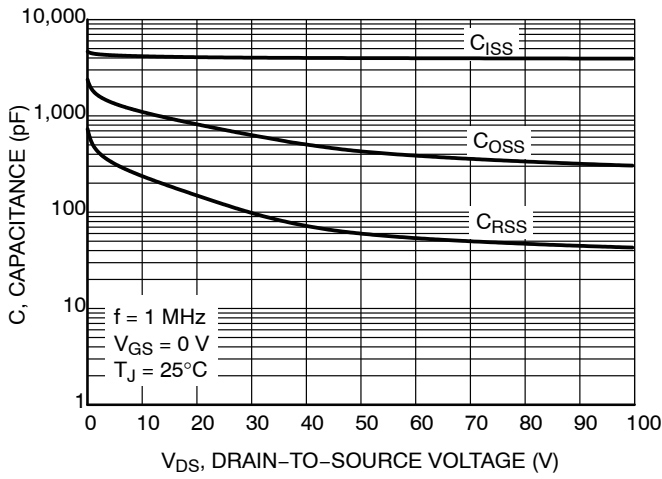


Figure 7. Capacitance Variation

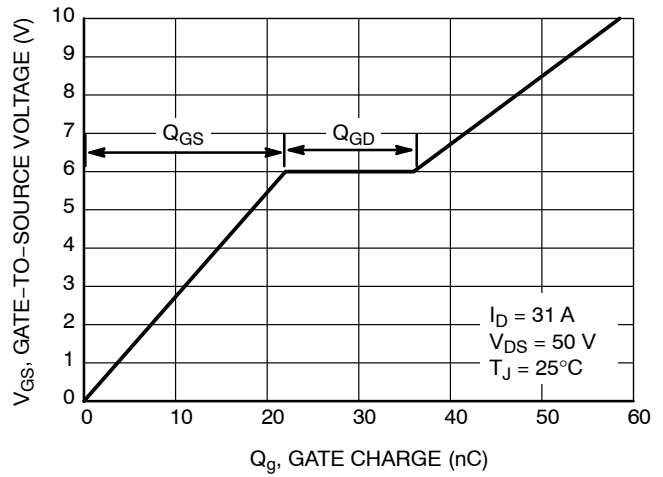


Figure 8. Gate-to-Source vs. Total Charge

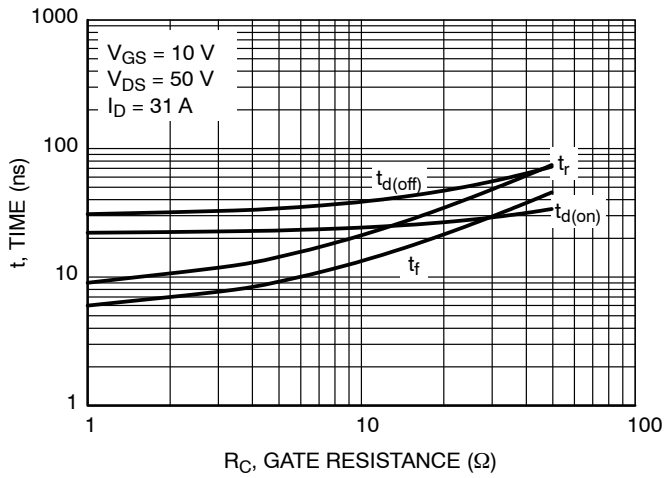


Figure 9. Resistive Switching Time Variation versus Gate Resistance

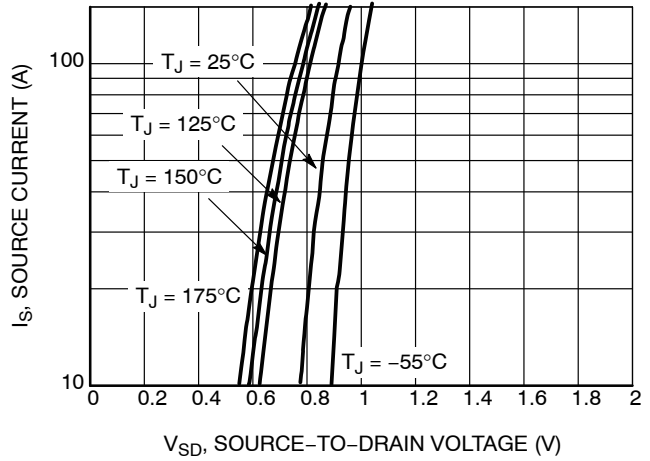


Figure 10. Diode Forward Voltage Versus Current

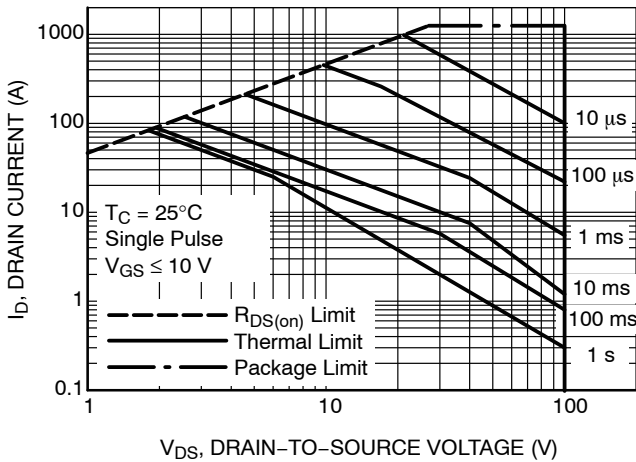


Figure 11. Forward Bias Safe Operating Area

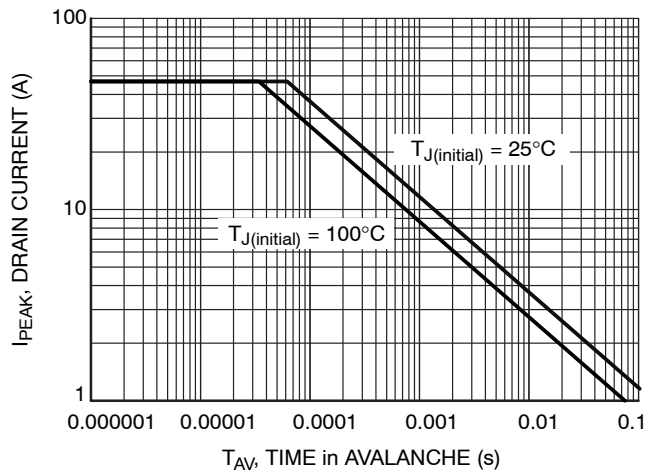


Figure 12. Maximum Drain Current Versus Time in Avalanche

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TYPICAL CHARACTERISTICS

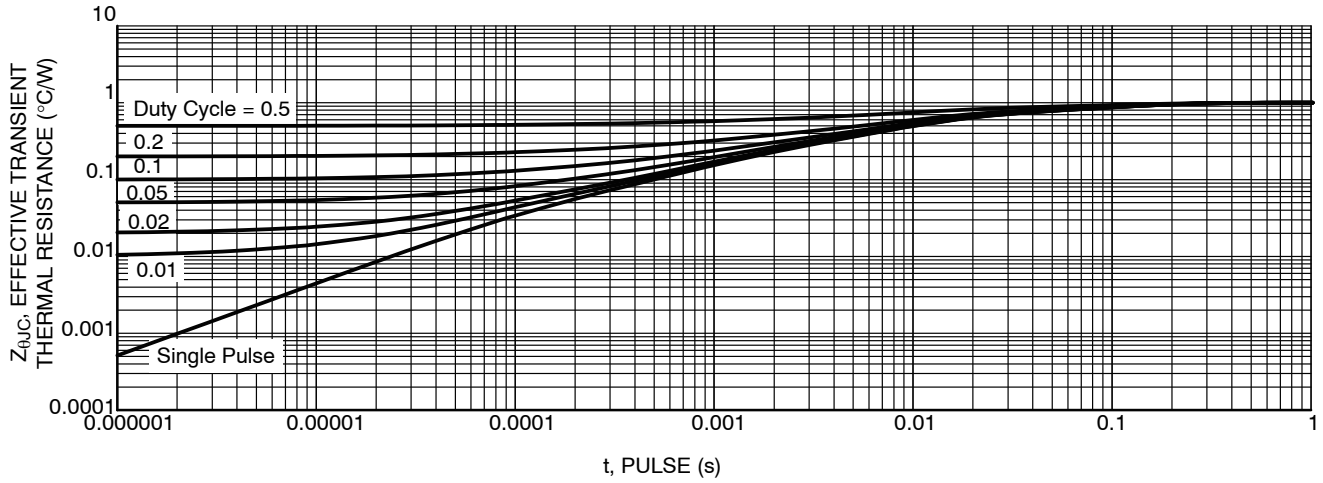


Figure 13. Transient Thermal Impedance

ORDERING INFORMATION

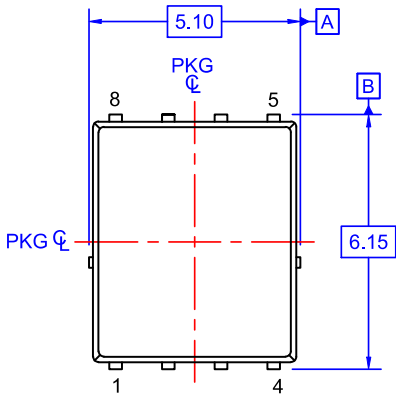
Device	Device Marking	Package	Shipping (Qty / Packing) [†]
NTMFS010N10GTWG	10N10G	PQFN8 (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

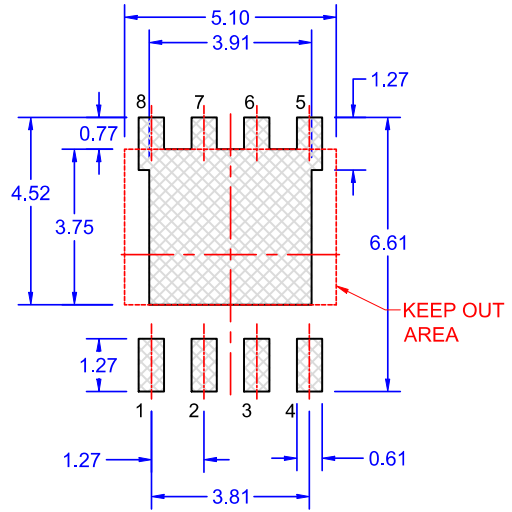
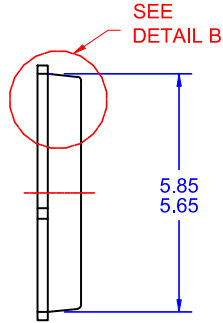
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PACKAGE DIMENSIONS

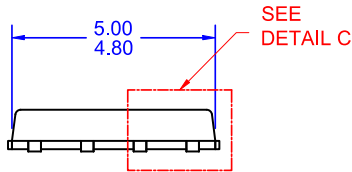
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE A



TOP VIEW

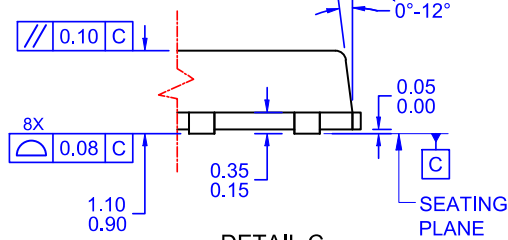


LAND PATTERN RECOMMENDATION

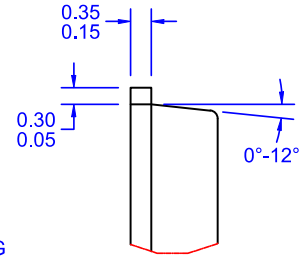


SIDE VIEW

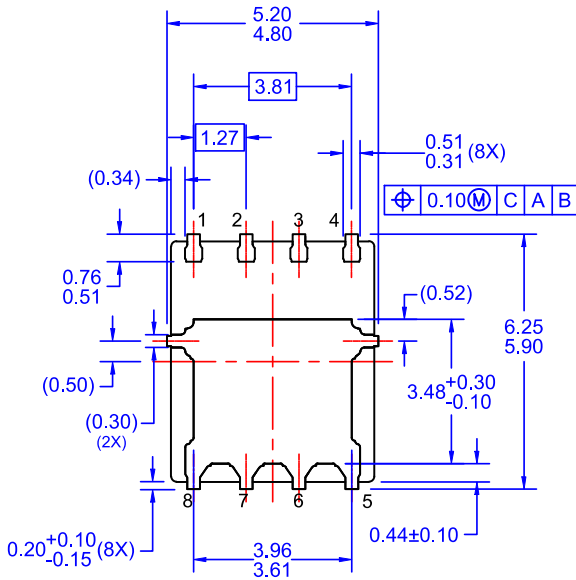
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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