Design Example Report

Title	***45 W Power Supply Using InnoSwitch3™-CP PowiGaN™ INN3279C-H222***
Specification	100 VAC – 135 VAC Input; 5 V / 6.5 A, 9 V / 5 A, 15 V / 3 A Output
Application	AC Outlet with USB Ports
Author	Applications Engineering Department
Document Number	DER-748
Date	November 11, 2019
Revision	1.0

Summary and Features

- 45 W compact power supply for high power USB Type-A/C port charging
- >91% average efficiency at nominal AC input
- Component temperatures <100 °C with up to 50 °C ambient temperature operation
- <30 mW no-load input power
- All the benefits of secondary side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
- Synchronous rectification for higher efficiency
- Accurate thermal protection with hysteretic shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection
- Meets IEC 2.0 kV common mode surge, 1.0 kV differential surge and EN55022 conducted EMI

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5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a power supply intended for USB wall outlet applications. The power supply can deliver up to 45 W output (selectable 5 V / 6.5 A or 9 V / 5 A or 15 V / 3 A) and is designed for high power USB charging with Type-A or Type-C ports. The design utilizes INN3279C from the InnoSwitch3-CP family of ICs. This design shows high power density and efficiency made possible by InnoSwitch3-CP switcher ICs.

DER-748 is a low-line input flyback converter design. The key design goals were high power density, high efficiency, low no load consumption, and best in class thermal performance.

This document contains the power supply specification, schematic diagram, bill of materials, printed circuit layout, and performance data.

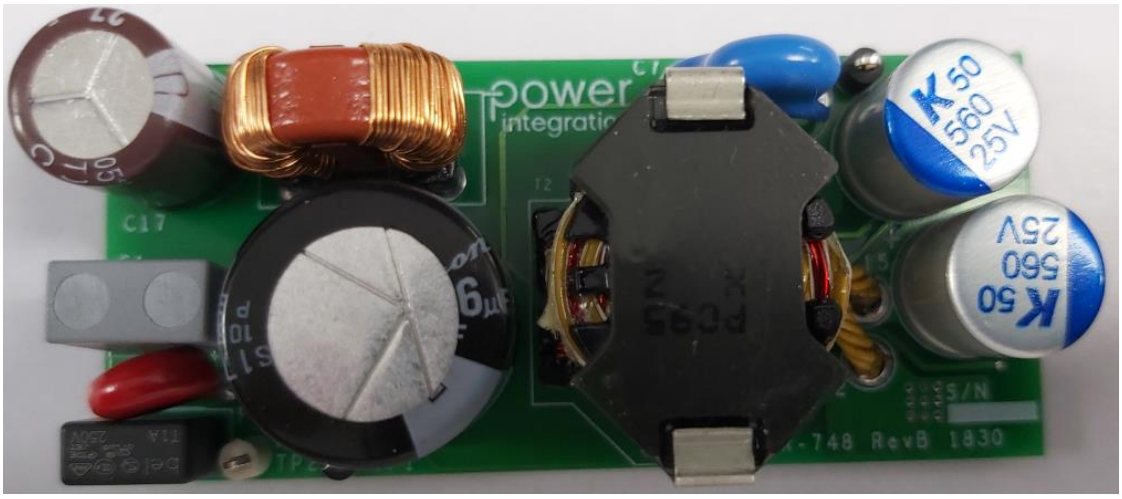

Figure 1 – Populated Circuit Board, Top View.

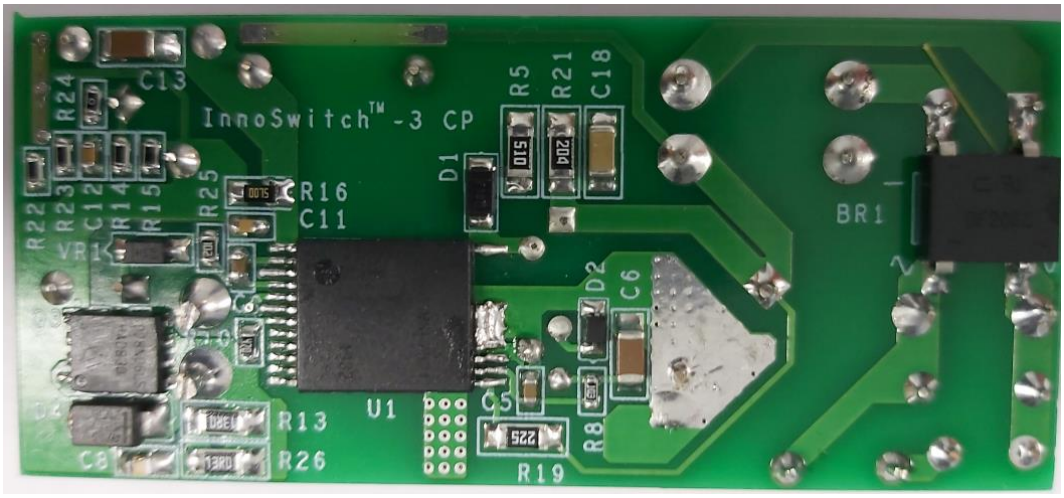

Figure 2 – Populated Circuit Board, Bottom View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	100	115	135	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	60	63	Hz	
No-load Input Power (115 VAC)				20	mW	Measured at 115 VAC.
5 V Output						
Output Voltage	V_{OUT}		5		V	±3%
Output Ripple Voltage	V_{RIPPLE}			150	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT}			6.5	A	20 MHz Bandwidth.
9 V Output						
Output Voltage	V_{OUT}		9		V	±5%
Output Ripple Voltage	V_{RIPPLE}			180	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT}			5.0	A	20 MHz Bandwidth.
15 V Output						
Output Voltage	V_{OUT}		15		V	±5%
Output Ripple Voltage	V_{RIPPLE}			300	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT}			3.0	A	20 MHz Bandwidth.
Continuous Output Power	P_{OUT}			45	W	At 15 V and 9 V Output.
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC60950 / UL1950 Class II				
Ambient Temperature	T_{AMB}	0		50	°C	Free Convection, Sea Level.

3 Schematic

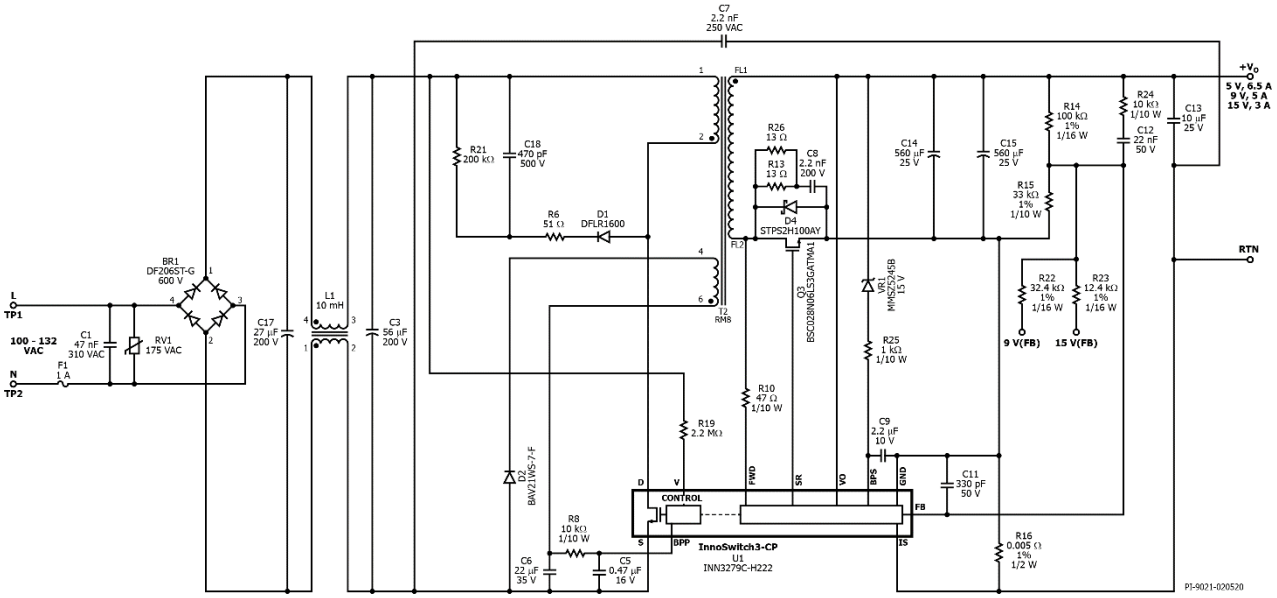

Figure 3 – Schematic.

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4 Circuit Description

The InnoSwitch3-CP IC combines primary, secondary and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates the primary MOSFET with low RDS, the primary-side controller, the secondary-side controller for synchronous rectification and the Fluxlink™ technology that eliminates the need for an optocoupler needed on a secondary sensed feedback system.

4.1 *Input Circuit Description*

Fuse F1 isolates the circuit and provides protection from component failure, and the capacitor C1 provides attenuation for EMI. Common mode inductor L1 and capacitors C3 and C17 form a π–filter that provides filtering for both common mode and differential mode noise. Bridge rectifiers BR1 rectifies the AC line voltage and provides a full wave rectified DC across the input capacitors C3 and C17.

4.2 *Primary-Side Circuit*

One end of the transformer T2 primary is connected to the rectified DC bus; the other is connected to the drain terminal of the MOSFET inside the INN3279C (U1).

A low cost RCD clamp formed by diode D1, resistors R5 and R21, and capacitor C18 limits the peak Drain voltage of U1 at the instant turn-off of the MOSFET. The clamp helps dissipate the energy stored in the leakage reactance of transformer T2.

The IC is kick-started by an internal high-voltage current source that charges the BPP pin capacitor C5 when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C6. Resistor R8 limits the current being supplied to the BPP pin of the InnoSwitch3 (U1). An R-C network can be placed across D2 to offer damping of the high frequency ringing, which can reduce radiated EMI.

The primary-side controller has a current limit threshold ramp that is inversely proportional to time from the end of the last primary switching cycle. The nature of this characteristic introduces a primary current limit that reduces as the switching frequency reduces. It is similar to the state machine of ON/OFF control but the reduction is now linear in nature rather than the discrete jumps in current limit that the ON/OFF state machine introduces. This produces a primary MOSFET switching pulse train that looks similar to a traditional PWM waveform under steady state conditions with consistent time and peak current between cycles rather than the ON/OFF cycle skipping.

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information where the start of the next switching cycle is immediate when a feedback switching cycle request is received.

Resistor R19 provides line voltage sensing and supplies a current to the V pin of U1, which is proportional to the DC voltage across capacitor C3. At approximately 55 V DC, the current through this resistor exceeds the line undervoltage threshold, which results in enabling of U1. At approximately 250 V DC, the current through this resistor exceeds the line overvoltage threshold, which results in disabling of U1.

4.3 *Secondary-Side Circuit*

The secondary-side of the INN3279C IC provides output voltage, output current sensing and drive a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by MOSFET Q3 and filtered by capacitors C14 and C15. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via RC snubber, R26, R13, and C8.

The gate of Q3 is turned on by the secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R10 and fed into the FWD pin of the IC.

In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on at the same time with the synchronous rectification MOSFET on time. The MOSFET drive signal is the output on the SR pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device then fed into VO pin and charges the decoupling capacitor C9 via an internal regulator.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary-side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C9 via resistor R10 and an internal regulator. This allows output current regulation to be maintained down to ~3.0 V. Below this level the unit enters auto-restart until the output load is reduced.

Output current is sensed by monitoring the voltage drop across resistors R16 between the IS and GND pins with a threshold of approximately 30 mV to reduce losses. Once the internal current sense threshold is exceeded the device enters into auto-restart mode.

Below the internal current sense threshold, the device operates in constant voltage mode. Output voltage is regulated so as to achieve an internal reference voltage of 1.265 V on the FB pin. Capacitor C12 form a phase-lead network that ensures stable operation and minimizes output voltage overshoot and undershoot during transient load conditions. Capacitor C11 provides noise filtering of the signal at the FB pin.

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Resistors R14 and R15 form the feedback divider network to sense the output voltage. To change the output to 9 V, resistor R22 is added in parallel to the bottom resistor R15. And to change the output to 15 V, resistor R23 is added in parallel to the bottom resistor R15. To vary the output voltage using a USB PD interface, the ports must be connected to the terminals 9V_FB and GND to make it a 9 V output and to the terminals 15V_FB and GND to make it a 15 V output.

Zener diode VR1 protects the power supply from output overvoltage. If the output voltage exceeds VR1 + BPS voltage, current will flow through the BPS pin that will result to auto-restart. A 15 V Zener regulator was used to not exceed the voltage rating of the output capacitors.

In order to improve conversion efficiency and reduce switching losses, InnoSwitch3 introduces a secondary-based QR functionality. The secondary controller has a means to allow switching when the voltage across the primary switch is near its minimum voltage when the converter operates in critical (CRM) or discontinuous conduction mode (DCM). Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FW pin voltage as it rises above the output voltage level is used to gate secondary request to initiate the switch "on" cycle in the primary controller.

4.4 *Design Key Points*

The design targets greater than 91% average efficiency for the 3 outputs. Efficiency was optimized with transformer design, chosen active devices and bias voltages. For the transformer design, it is best to keep the reflected voltage (VOR) low to decrease the RMS current on the secondary-side. Lower VOR also means lower drain to source voltage on the primary side MOSFET that can reduce switching loss. In this design, the VOR was set to 45 V for the 5 V output. The operation for the 5 V outputs at full load is in deep continuous mode (CCM) while the other output is in DCM with valley switching on the first or second valley. Always note that further lowering the VOR can lead to a very large leading edge spike on the primary current because of very deep CCM operation. This can trigger the SOA peak limit protection that will result to auto-restart.

Aside from the VOR consideration it is also important to lower the leakage inductance of the transformer. The energy being stored in the leakage inductance which is dissipated on the clamping circuit contributes to lower efficiency. Reducing the leakage is an utmost important in this design, to significantly increase the efficiency. A sandwich winding was used to lower the leakage inductance to a value less than 5 μH (<2% of magnetizing inductance). Detailed transformer construction is described on section 7 of this report.

For higher efficiency, it is also necessary to choose the active devices that offer lower conduction losses. For the InnoSwitch3 family, INN3279C offers the lowest $R_{DS(ON)}$. For the secondary rectifier (SR), a MOSFET was chosen instead of a Schottky diode. A MOSFET of 2.8 mΩ $R_{DS(ON)}$ was used in the design. An added Schottky diode in parallel with the SR FET gives a slight improvement on the efficiency. This diode conducts

instead of the MOSFET body diode during the start of secondary MOSFET ON and before the secondary current reaches zero or secondary MOSFET OFF. These delays on transition are needed to avoid cross-conduction with the primary MOSFET.

The sweet spot (efficiency and small form factor consideration) for switching frequency operation is at the range from 70 kHz to 80 kHz. An RM8 transformer with AE of 64 mm^2 is enough without saturating the core. The design chooses the minimum number of secondary turns at 390 mT flux density.

Auxiliary bias voltage was chosen at range from 7 V to 9 V at no-load condition. This helps improves no load consumption as well as light load efficiency.

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5 PCB Layout

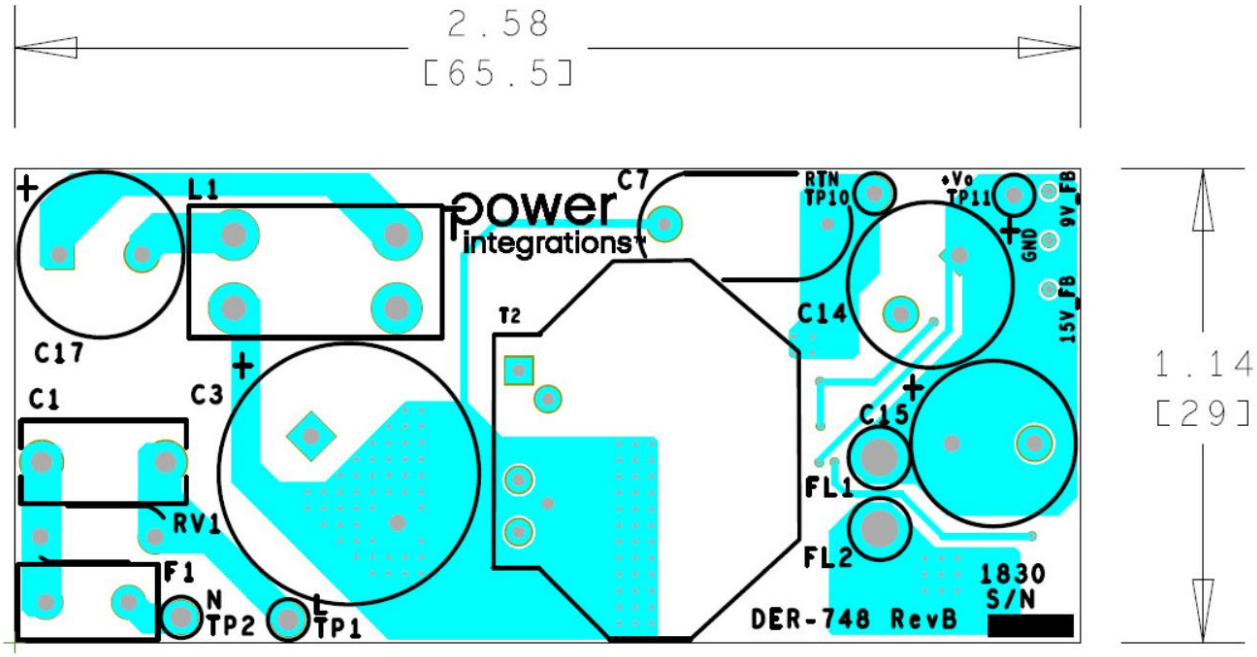

Figure 4 – Top Side.

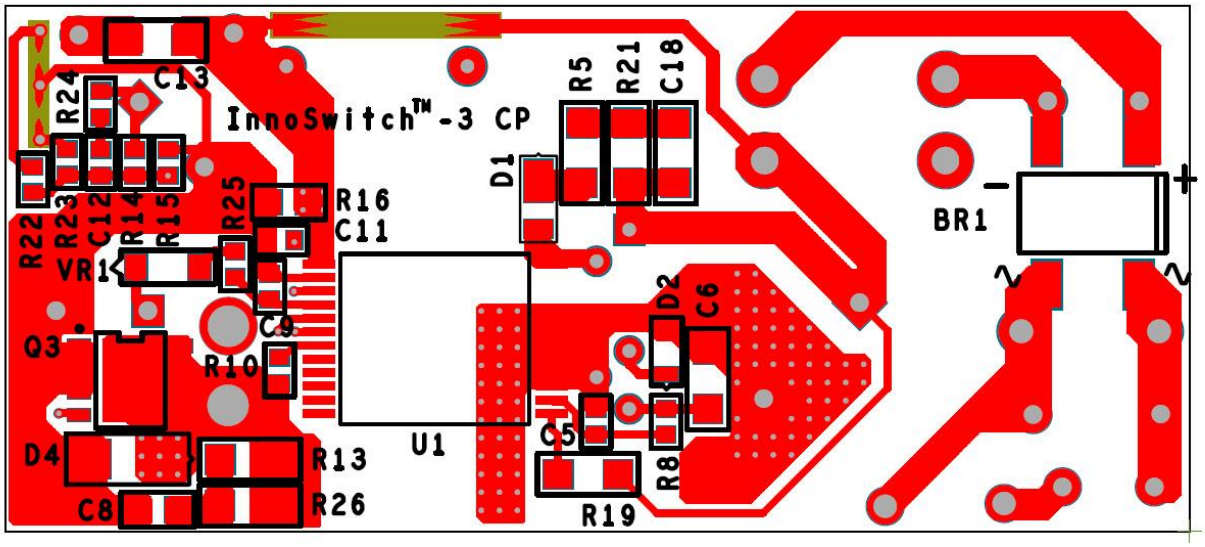

Figure 5 – Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg	Mfg Part Number
1	1	BR1	600 V, 2 A, Bridge Rectifier, SMD, DFS	DF206ST-G	Comchip
2	1	C1	47 nF, 310 VAC, Polyester Film, X2	BFC233920473	Vishay
3	1	C3	CAP, 56 μF, ±20%, 200 V, Aluminum, Radial, Can, 10000 Hrs @ 105 °C, (16 x16mm) LS (7.50mm),	200BXF56M16X16	Rubycon
4	1	C5	0.47 μF, 10%, 16V, X7R, 0603	GRM188R71C474KA88D	Murata
5	1	C6	22 μF, 35 V, Ceramic, X5R, 1206	C3216X5R1V226M160AC	TDK
6	1	C7	2.2 nF, Ceramic, Y1	KJN222MQ47FAFZA	KEMET
7	1	C8	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX
8	1	C9	2.2 μF, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
9	1	C11	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
10	1	C12	22 nF 50 V, Ceramic, X7R, 0603	06035C223KAT2A	AVX
11	1	C13	10 μF, 25 V, Ceramic, X7R, 1206	C3216X7R1E106M160AB	TDK
12	1	C14	560 μF, 25 V,±20%, Al Organic Polymer, Gen. Purpose, Can, 15 mΩ, 2000 Hrs @ 105°C	A750MS567M1EAAE015	KEMET
13	1	C15	560 μF, 25 V,±20%, Al Organic Polymer, Gen. Purpose, Can, 15 mΩ, 2000 Hrs @ 105°C	A750MS567M1EAAE015	KEMET
14	1	C17	27 μF, 200 V, Electrolytic, (10 x 16),	EKXJ201ELL270MJ16S	Nippon Chemi-Con
15	1	C18	470 pF, ±10%, 500 V, X7R, Ceramic, SMT, MLCC 1206 (3216 Metric)	CC1206KKX7RBBB471	Yageo
16	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
17	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
18	1	D4	100 V, 2 A, Schottky, SMA	STPS2H100AY	ST Micro
19	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
20	1	L1	10 mH, 0.7 A, Common Mode Choke	744821110	Wurth
21	1	Q3	MOSFET, N-CH, 60V, 23A (Ta), 100A (Tc), 100A (Tc) 2.5W (Ta), 139W (Tc), SMD, PG-TSDSON-8	BSC028N06LS3GATMA1	Infineon
22	1	R5	RES, 51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
23	1	R8	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
24	1	R10	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
25	1	R13	RES, 13 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ130V	Panasonic
26	1	R14	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
27	1	R15	RES, SMD, 33 KΩ, 1%, 1/10 W, ±100ppm/°C, 0603	RC0603FR-0733KL	Yageo
28	1	R16	RES, 0.005 Ω, 0.5 W, 1%, 0805	PMR10EZPFU5L00	Rohm
29	1	R19	RES, 2.2 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ225V	Panasonic
30	1	R21	RES, 200 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
31	1	R22	RES, 32.4 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3242V	Panasonic
32	1	R23	RES, 12.4 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1242V	Panasonic
33	1	R24	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
34	1	R25	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
35	1	R26	RES, 13 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ130V	Panasonic
36	1	RV1	175 VAC, 17 J, 7 mm, RADIAL	ERZ-V07D271	Panasonic
37	1	T2	Bobbin, RM8, Vertical, 8 pins (6 x 2)	RM8(SX-814)	ShenZhen SanXiangYuan
38	1	TP1	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
39	1	TP2	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
40	1	TP10	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
41	1	TP11	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
42	1	U1	InnoSwitch-3, InSOP24D	INN3279C-H222	Power Integrations
43	1	VR1	15 V, 5%, 500 mW, SOD-123	MMSZ5245B-E3-08	Vishay

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7 Transformer (T2) Specification

7.1 *Electrical Diagram*

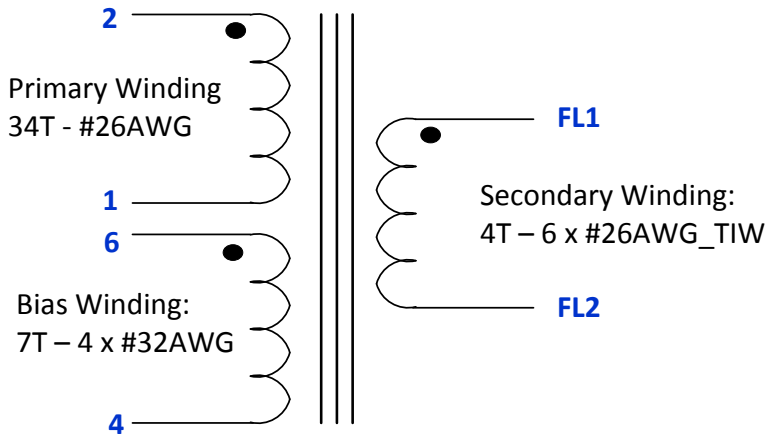

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Electrical Strength	1 second, 60 Hz, from pins 1, 2, 4 and 6 to FL1, FL2.	3000 VAC
Primary Inductance	Pins 1-2, all other open, measured at 100 kHz, 0.4 V_{RMS}.	380 µH, ±5%
Primary Leakage	Pins 1-2, with FL1-FL2 shorted, measured at 100 kHz, 0.4 V_{RMS}.	7µH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: RM8, PC95.
[2]	Bobbin: RM8, Vertical, 8 Pins.
[3]	Magnet Wire: #26 AWG Double Coated, Solderable.
[4]	Magnet Wire: #32 AWG Double Coated, Solderable.
[5]	Magnet Wire: #26 AWG Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 8 mm Wide.
[7]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

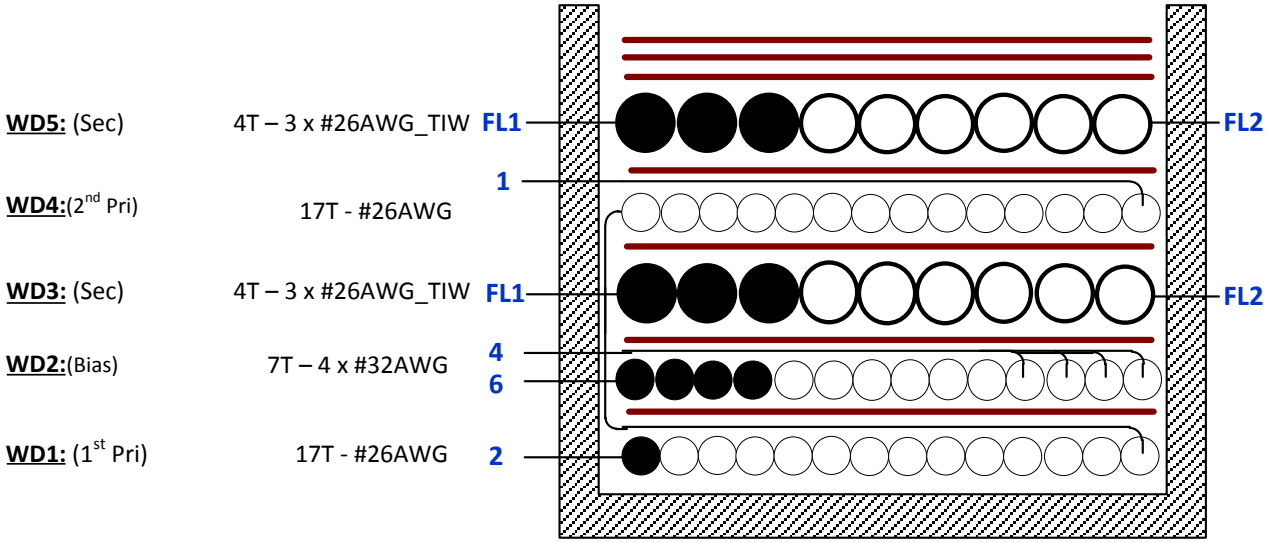

Figure 7 – Transformer Build Diagram.

7.5 *Transformer Construction*

Winding Preparation	Place the bobbin Item [2] on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
WD1 1st Primary	Start at pin 2, wind 17 turns of wire Item [3] in 1 layer. At the last turn, bring wire back to the left side (floating).
Insulation	Place 1 layer of tape Item [6] for insulation.
WD2 Bias/Shield	Start at pin 6, wind 7 (4-filars) turns of wire Item [4] in 1 layer. At the last turn, bring bifilar wire back to the left finish at pin 4.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD3 Secondary	Start at FL1 from the left side of the bobbin, wind 4 trifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD4 2nd Primary	Continue primary winding of 17 turns from left to right. At the last turn finish at pin 1.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD5 Secondary	Start at FL1 from the left side of the bobbin, wind 4 trifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.
Insulation	Place 3 layers of tape Item [6] for insulation and secure the windings.
Core Inductance	Gap core halves to get 380 μH inductance.
Finish Assembly	Cover core with 2 layers of tape. Varnish Item [7].

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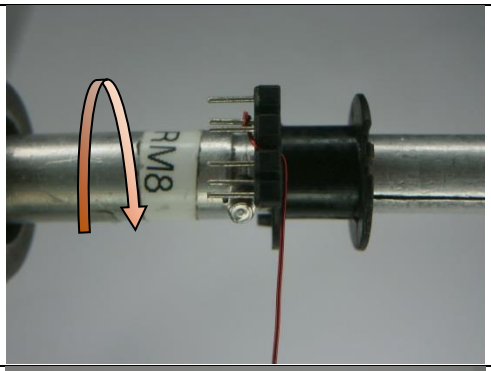
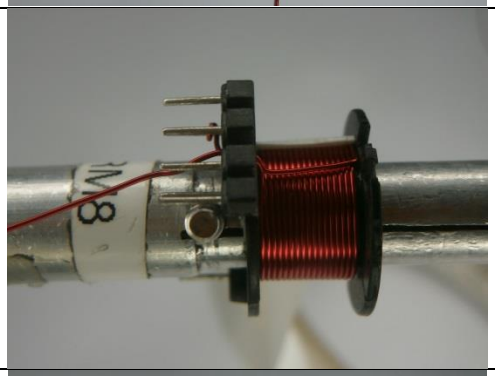
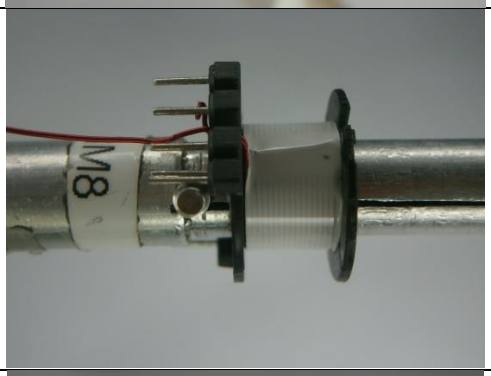
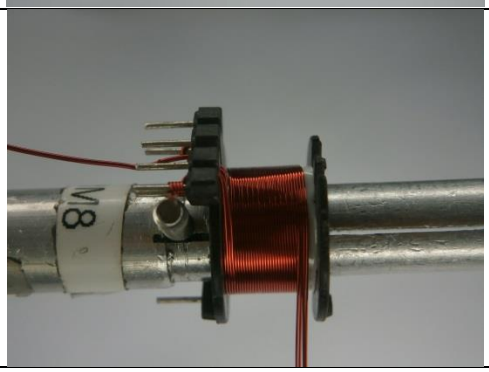
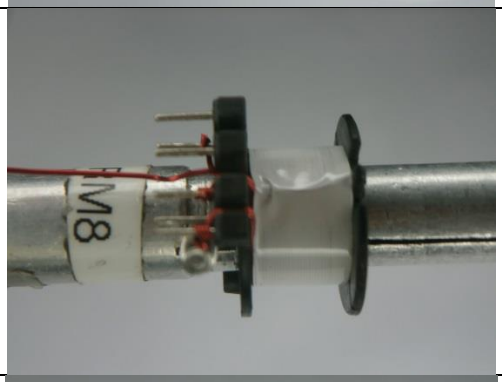
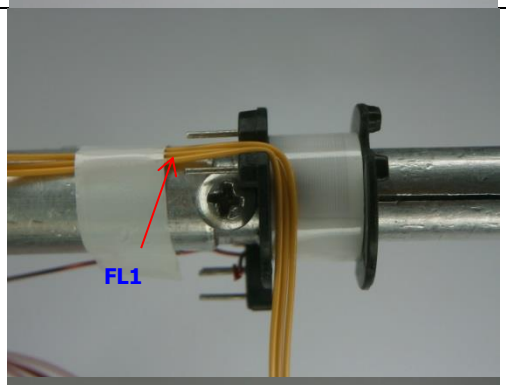
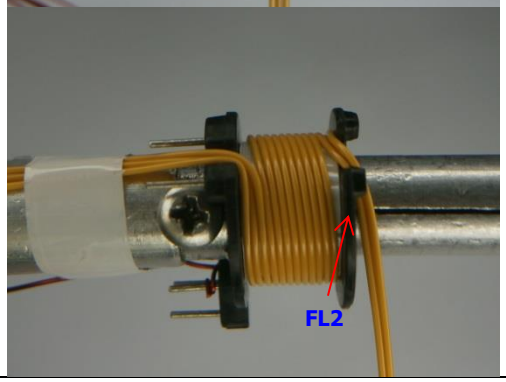
7.6 *Winding Illustrations*

Winding Preparation		Place the bobbin Item [2] on the mandrel with the pin side is on the left side Winding direction is clockwise direction.
WD1 **1st Primary**		Start at pin 2, wind 17 turns of wire Item [3] in 1 layer. At the last turn, bring wire back to the left side (floating).
Insulation		Place 1 layer of tape Item [6] for insulation.
WD2 **Bias/Shield**		Start at pin 6, wind 7 (4-filars) turns of wire Item [4] in 1 layer. At the last turn, bring bifilar wire back to the left finish at pin 4.

		
Insulation		Place 1 layer of tape Item [6] for insulation.
WD3 Secondary	 	Start at FL1 from the left side of Start at FL1 from the left side of the bobbin, wind 4 trifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.the bobbin, wind 4 bifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.

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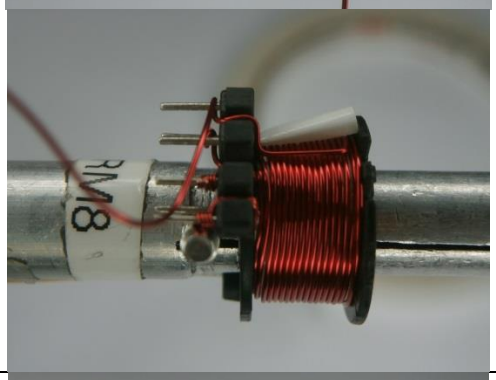
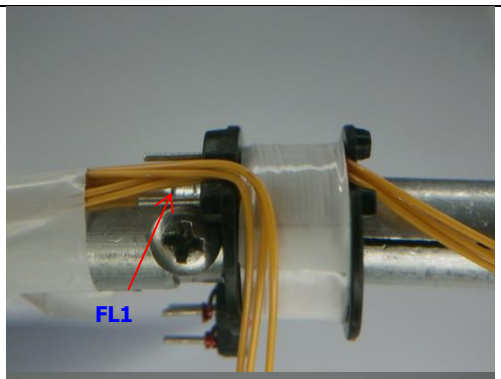
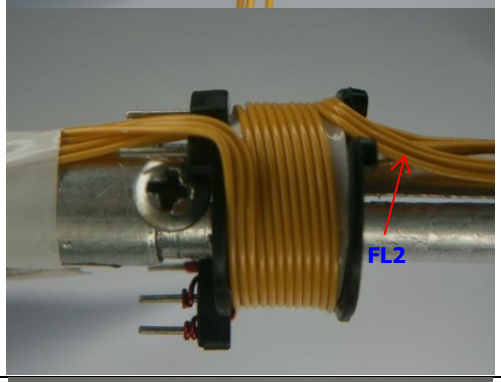
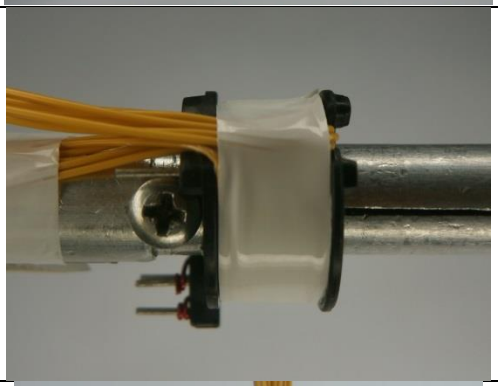
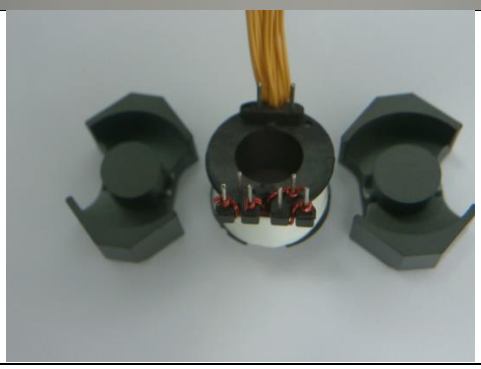
Insulation		Place 1 layer of tape Item [6] for insulation.
WD4 **2nd Primary**	 	Continue primary winding of 17 turns from left to right. At the last turn finish at pin 1.
Insulation		Place 1 layer of tape Item [6] for insulation.

WD5 Secondary	 	Start at FL1 from the left side of the bobbin, wind 4 trifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.
Insulation		Place 3 layers of tape Item [6] for insulation and secure the windings.
Core Inductance		Gap core halves to get 380 µH inductance. Use clip to fix.

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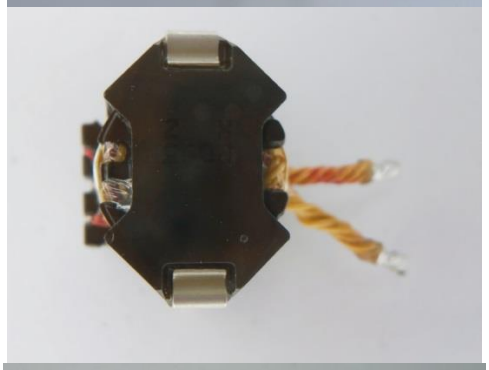
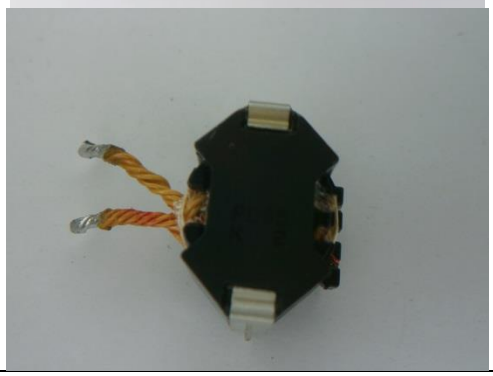
Finish Assembly	  	Cover core with 2 layers of tape. Varnish Item [7].

8 Inductor Design Spreadsheet

Copyright Power Integrations 2018	INPUT	OUTPUT	UNITS	Flyback Design Spreadsheet
APPLICATION VARIABLES				
VAC_MIN	100	100	V	Minimum AC line voltage
VAC_MAX	135	135	V	Maximum AC input voltage
VAC_RANGE		LOW LINE		AC line voltage range
FLINE	60	60	Hz	AC line voltage frequency
CAP_INPUT	80.0	80.0	uF	Input capacitance
SETPOINT 1				
VOUT1	15.00	15.00	V	Output voltage 1, should be the highest output voltage required
IOUT1	3.000	3.000	A	Output current 1
POUT1		45.00	W	Output power 1
EFFICIENCY1	0.92	0.92		Converter efficiency for output 1
Z_FACTOR1	0.50	0.50		Z-factor for output 1
SETPOINT 2				
VOUT2	9.00	9.00	V	Output voltage 2
IOUT2	5.000	5.000	A	Output current 2
POUT2		45.00	W	Output power 2
EFFICIENCY2	0.92	0.92		Converter efficiency for output 2
Z_FACTOR2	0.50	0.50		Z-factor for output 2
SETPOINT 3				
VOUT3	5.00	5.00	V	Output voltage 3
IOUT3	6.500	6.500	A	Output current 3
POUT3		32.50	W	Output power 3
EFFICIENCY3	0.90	0.90		Converter efficiency for output 3
Z_FACTOR3	0.50	0.50		Z-factor for output 3
PERCENT_CDC		0%		Percentage (of output voltage) cable drop compensation desired at full load
PRIMARY CONTROLLER SELECTION				
ENCLOSURE	OPEN FRAME	OPEN FRAME		Power supply enclosure
ILIMIT_MODE	STANDARD	STANDARD		Device current limit mode
VDRAIN_BREAKDOWN		750	V	Device breakdown voltage
DEVICE_GENERIC	AUTO	INN3279C		Device selection
DEVICE_CODE		INN3279C		Device code
PDEVICE_MAX		75	W	Device maximum power capability
RDSON_25DEG		0.34	Ω	Primary switch on-time resistance at 25°C
RDSON_100DEG		0.53	Ω	Primary switch on-time resistance at 100°C
ILIMIT_MIN		1.767	A	Primary switch minimum current limit
ILIMIT_TYP		1.900	A	Primary switch typical current limit
ILIMIT_MAX		2.033	A	Primary switch maximum current limit
VDRAIN_ON_SWITCH		0.23	V	Primary switch on-time voltage drop
VDRAIN_OFF_SWITCH		389.49	V	Peak drain voltage on the primary switch during turn-off
WORST CASE ELECTRICAL PARAMETERS				
FSWITCHING_MAX	88000	88000	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
VOR	130.0	130.0	V	Voltage reflected to the primary winding (corresponding to setpoint 1) when the primary switch turns off
VMIN		110.06	V	Valley of the rectified minimum input AC voltage at full load
KP		0.723		Measure of continuous/discontinuous mode of operation
MODE_OPERATION		CCM		Mode of operation
DUTYCYCLE		0.496		Primary switch duty cycle
TIME_ON		7.00	us	Primary switch on-time

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TIME_OFF		5.93	us	Primary switch off-time
LPRIMARY_MIN		362.0	uH	Minimum primary magnetizing inductance
LPRIMARY_TYP		381.1	uH	Typical primary magnetizing inductance
LPRIMARY_TOL		5.0	%	Primary magnetizing inductance tolerance
LPRIMARY_MAX		400.1	uH	Maximum primary magnetizing inductance
PRIMARY CURRENT				
IAVG_PRIMARY		0.428	A	Primary switch average current
IPEAK_PRIMARY		1.945	A	Primary switch peak current
IPEDESTAL_PRIMARY		0.465	A	Primary switch current pedestal
IRIPPLE_PRIMARY		1.945	A	Primary switch ripple current
IRMS_PRIMARY		0.746	A	Primary switch RMS current
SECONDARY CURRENT				
IPEAK_SECONDARY		17.021	A	Secondary switch peak current
IPEDESTAL_SECONDARY		4.067	A	Secondary switch pedestal current
IRMS_SECONDARY		8.725	A	Secondary switch RMS current
IRIPPLE_CAP_OUT		5.890	A	Output capacitor ripple current
TRANSFORMER CONSTRUCTION PARAMETERS				
CORE SELECTION				
CORE	RM8	RM8		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
CORE NAME		B65811J0000R095		Core code
AE		64.0	mm^2	Core cross sectional area
LE		38.0	mm	Core magnetic path length
AL		4100	nH	Ungapped core effective inductance per turns squared
VE		2430	mm^3	Core volume
BOBBIN NAME		B65812N1012D001		Bobbin name
AW		30.0	mm^2	Bobbin window area
BW		10.03	mm	Bobbin width
MARGIN		0.0	mm	Bobbin safety margin
PRIMARY WINDING				
NPRIMARY		35		Primary winding number of turns
BPEAK		3717	Gauss	Peak flux density
BMAX		3435	Gauss	Maximum flux density
BAC		1717	Gauss	AC flux density (0.5 x Peak to Peak)
ALG		311	nH	Typical gapped core effective inductance per turns squared
LG		0.239	mm	Core gap length
LAYERS_PRIMARY		2		Primary winding number of layers
AWG_PRIMARY		25		Primary wire gauge
OD_PRIMARY_INSULATED		0.518	mm	Primary wire insulated outer diameter
OD_PRIMARY_BARE		0.455	mm	Primary wire bare outer diameter
CMA_PRIMARY		429.7	Cmils/A	Primary winding wire CMA
SECONDARY WINDING				
NSECONDARY		4		Secondary winding number of turns
AWG_SECONDARY		17		Secondary wire gauge
OD_SECONDARY_INSULATED		1.454	mm	Secondary wire insulated outer diameter
OD_SECONDARY_BARE		1.150	mm	Secondary wire bare outer diameter
CMA_SECONDARY		234.8	Cmils/A	Secondary winding wire CMA
BIAS WINDING				
NBIAS		7		Bias winding number of turns
PRIMARY COMPONENTS SELECTION				
LINE UNDERVOLTAGE				
BROWN-IN REQURED	45.00	45.00	V	Required line brown-in threshold

RLS		2.26	MΩ	Connect two 1.13 MOhm resistors to the V-pin for the required UV/OV threshold
BROWN-IN ACTUAL		45.49	V	Actual brown-in threshold using standard resistors
BROWN-OUT ACTUAL		41.16	V	Actual brown-out threshold using standard resistors
LINE OVERVOLTAGE				
OVERVOLTAGE_LINE		189.03	V	Actual AC RMS line over-voltage threshold
BIAS WINDING				
VBIAS	8.00	8.00	V	The rectified bias voltage maybe too low to supply the BP pin: Increase the rectified bias voltage to a value higher than 9V
VF_BIAS		0.70	V	Bias winding diode forward drop
VREVERSE_BIASDIODE		45.90	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
CBIAS		22	uF	Bias winding rectification capacitor
CBPP		0.47	uF	BPP pin capacitor
SECONDARY COMPONENTS SELECTION				
RECTIFIER				
VDRAIN_OFF_SRFET		36.66	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
SRFET	AUTO	AON6244		Secondary rectifier (Logic MOSFET)
VBREAKDOWN_SRFET		60	V	Secondary rectifier breakdown voltage
RDSON_SRFET		6.2	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
FEEDBACK COMPONENTS				
RFB_UPPER		100.00	kΩ	Upper feedback resistor (connected to the output terminal)
RFB_LOWER		34.00	kΩ	Lower feedback resistor required to obtain the output for cable drop compensation
CFB_LOWER		330	pF	Lower feedback resistor decoupling capacitor
SETPOINTS ANALYSIS				
TOLERANCE CORNER				
USER_VAC	115	115	V	Input AC RMS voltage corner to be evaluated
USER_ILIMIT	TYP	1.900	A	Current limit corner to be evaluated
USER_LPRIMARY	TYP	381.1	uH	Primary inductance corner to be evaluated
SETPOINT SELECTION				
SETPOINT	1	1		Select the setpoint which needs to be evaluated
FSWITCHING		73247.1	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
VOR		130.0	V	Voltage reflected to the primary winding when the primary switch turns off
VMIN		135.40	V	Valley of the minimum input AC voltage
KP		1.578		Measure of continuous/discontinuous mode of operation
MODE_OPERATION		DCM		Mode of operation
DUTYCYCLE		0.379		Primary switch duty cycle
TIME_ON		5.17	us	Primary switch on-time
TIME_OFF		8.48	us	Primary switch off-time
PRIMARY CURRENT				
IAVG_PRIMARY		0.347	A	Primary switch average current
IPEAK_PRIMARY		1.834	A	Primary switch peak current
IPEDESTAL_PRIMARY		0.000	A	Primary switch current pedestal
IRIPPLE_PRIMARY		1.834	A	Primary switch ripple current

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IRMS_PRIMARY		0.652	A	Primary switch RMS current
SECONDARY CURRENT				
IPEAK_SECONDARY		16.050	A	Secondary switch peak current
IPEDESTAL_SECONDARY		0.000	A	Secondary switch pedestal current
IRMS_SECONDARY		5.815	A	Secondary switch RMS current
IRIPPLE_CAP_OUT		4.982	A	Output capacitor ripple current
MAGNETIC FLUX DENSITY				
BPEAK		3308	Gauss	Peak flux density
BMAX		3121	Gauss	Maximum flux density
BAC		1560	Gauss	AC flux density (0.5 x Peak to Peak)
SETPOINT	2	2		Select the setpoint which needs to be evaluated
FSWITCHING		73306.5	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
VOR		78.3	V	Voltage reflected to the primary winding when the primary switch turns off
VMIN		135.40	V	Valley of the minimum input AC voltage
KP		0.968		Measure of continuous/discontinuous mode of operation
MODE_OPERATION		CCM		Mode of operation
DUTYCYCLE		0.367		Primary switch duty cycle
TIME_ON		5.10	us	Primary switch on-time
TIME_OFF		8.64	us	Primary switch off-time
PRIMARY CURRENT				
IAVG_PRIMARY		0.347	A	Primary switch average current
IPEAK_PRIMARY		1.834	A	Primary switch peak current
IPEDESTAL_PRIMARY		0.059	A	Primary switch current pedestal
IRIPPLE_PRIMARY		1.776	A	Primary switch ripple current
IRMS_PRIMARY		0.652	A	Primary switch RMS current
SECONDARY CURRENT				
IPEAK_SECONDARY		16.051	A	Secondary switch peak current
IPEDESTAL_SECONDARY		0.515	A	Secondary switch pedestal current
IRMS_SECONDARY		7.495	A	Secondary switch RMS current
IRIPPLE_CAP_OUT		5.584	A	Output capacitor ripple current
MAGNETIC FLUX DENSITY				
BPEAK		3308	Gauss	Peak flux density
BMAX		3121	Gauss	Maximum flux density
BAC		1510	Gauss	AC flux density (0.5 x Peak to Peak)
SETPOINT	3	3		Select the setpoint which needs to be evaluated
FSWITCHING		58684.4	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
VOR		43.9	V	Voltage reflected to the primary winding when the primary switch turns off
VMIN		142.27	V	Valley of the minimum input AC voltage
KP		0.846		Measure of continuous/discontinuous mode of operation
MODE_OPERATION		CCM		Mode of operation
DUTYCYCLE		0.236		Primary switch duty cycle
TIME_ON		4.53	us	Primary switch on-time
TIME_OFF		13.02	us	Primary switch off-time
PRIMARY CURRENT				
IAVG_PRIMARY		0.241	A	Primary switch average current
IPEAK_PRIMARY		1.773	A	Primary switch peak current
IPEDESTAL_PRIMARY		0.273	A	Primary switch current pedestal
IRIPPLE_PRIMARY		1.500	A	Primary switch ripple current
IRMS_PRIMARY		0.540	A	Primary switch RMS current
SECONDARY CURRENT				
IPEAK_SECONDARY		15.511	A	Secondary switch peak current
IPEDESTAL_SECONDARY		2.386	A	Secondary switch pedestal current

IRMS_SECONDARY		8.494	A	Secondary switch RMS current
IRIPPLE_CAP_OUT		5.467	A	Output capacitor ripple current
MAGNETIC FLUX DENSITY				
BPEAK		3308	Gauss	Peak flux density
BMAX		3016	Gauss	Maximum flux density
BAC		1276	Gauss	AC flux density (0.5 x Peak to Peak)

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9 Performance Data

9.1 *Efficiency*

Note: Output voltage measured at PCB end.

9.1.1 Efficiency vs. Line

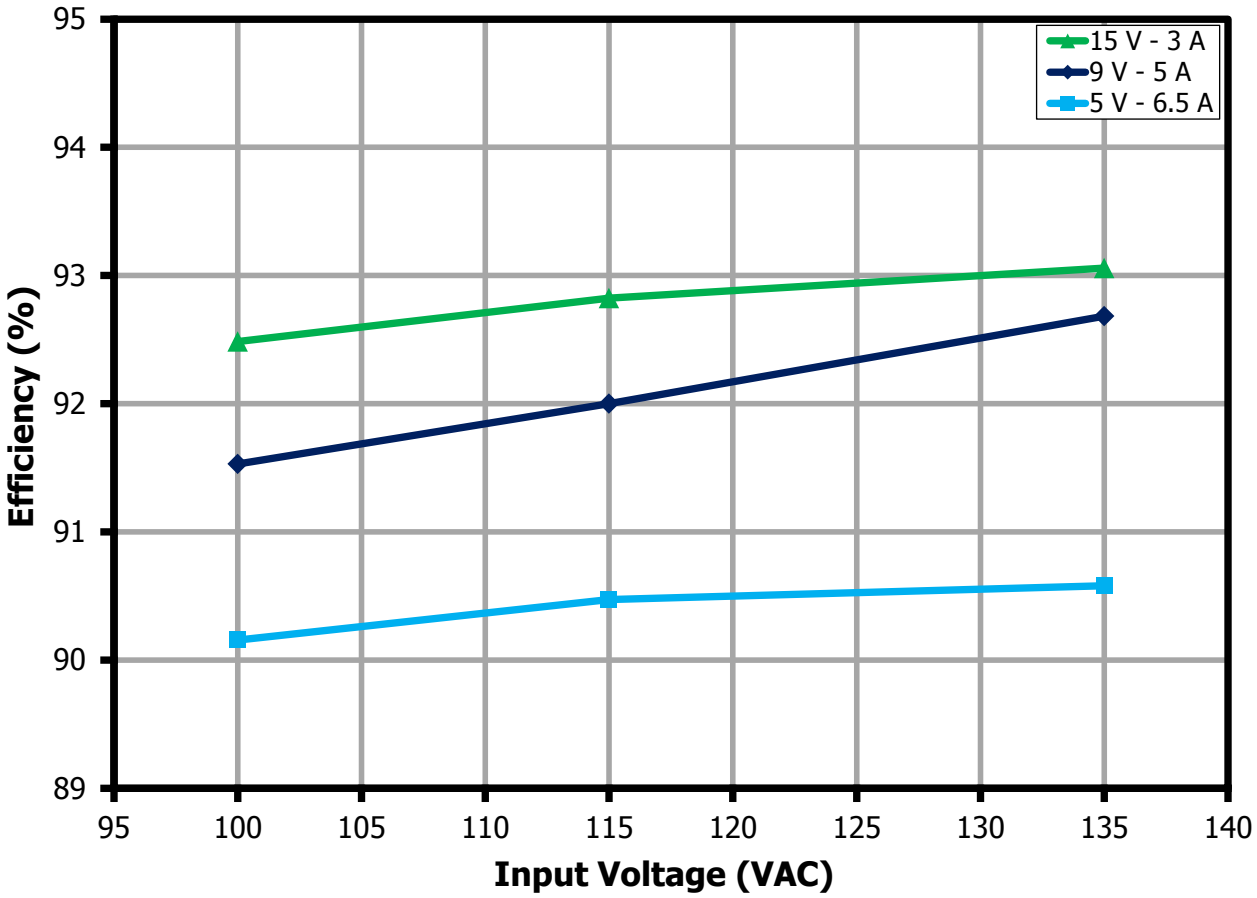

Figure 8 – Efficiency vs. Input Line Voltage.

9.1.2 Efficiency vs. Load

Note: Output voltage measured at PCB end.

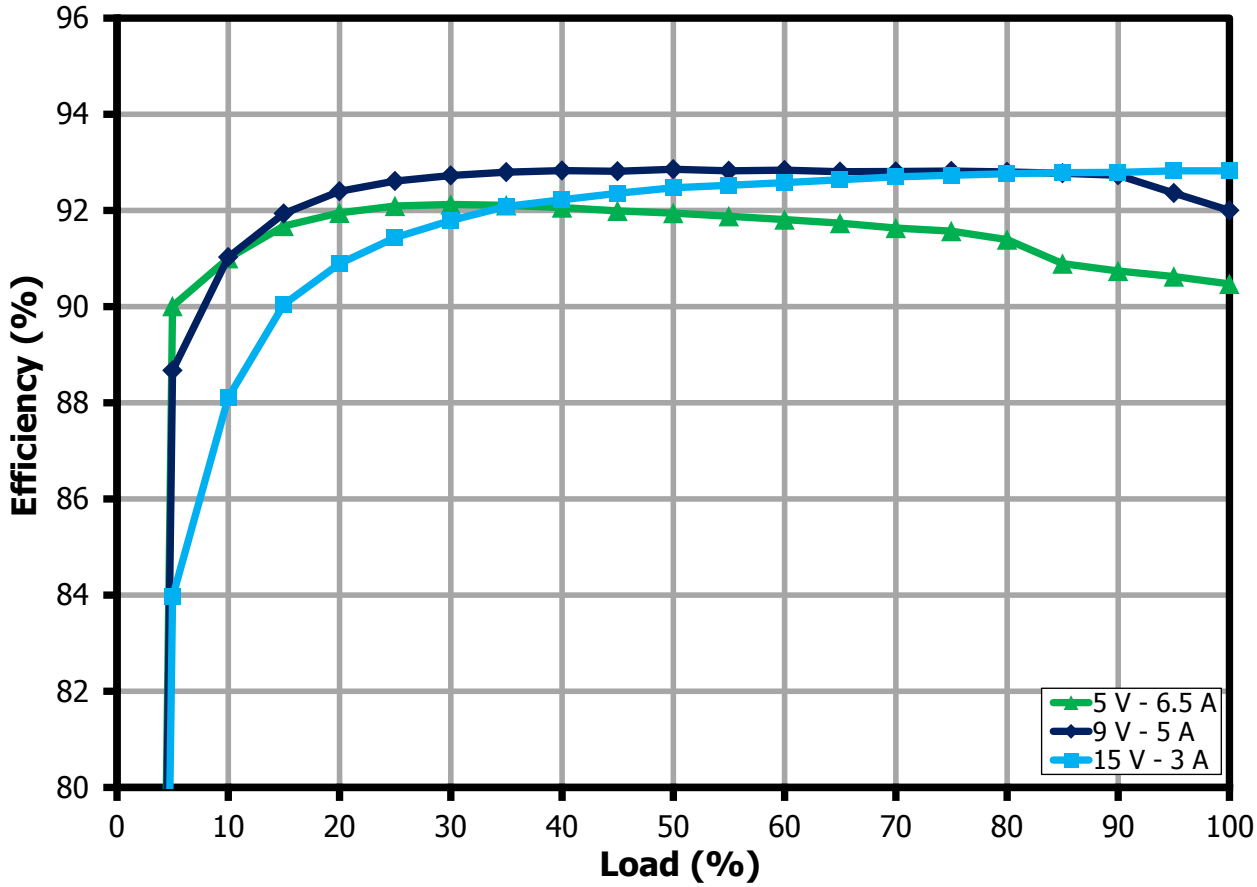

Figure 9 – Efficiency vs. Percent Load.

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9.1.3 No-Load Input Power

Note: 5 V output at no-load.

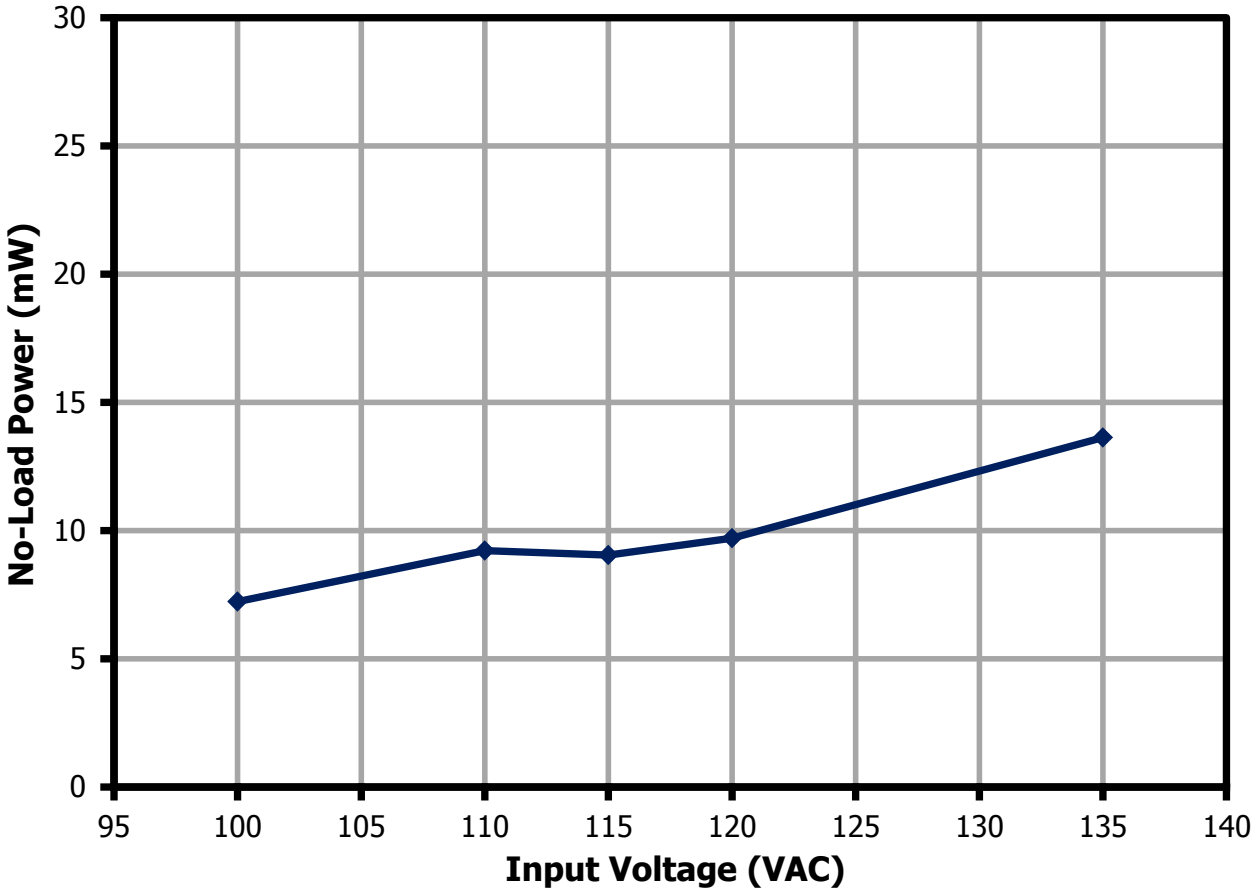

Figure 10 – No-Load Power vs. Input Line Voltage.

9.2 *Line and Load Regulation*

9.2.1 5 V Line Regulation at 6.5 A Load

Note: Output voltage measured at PCB end.

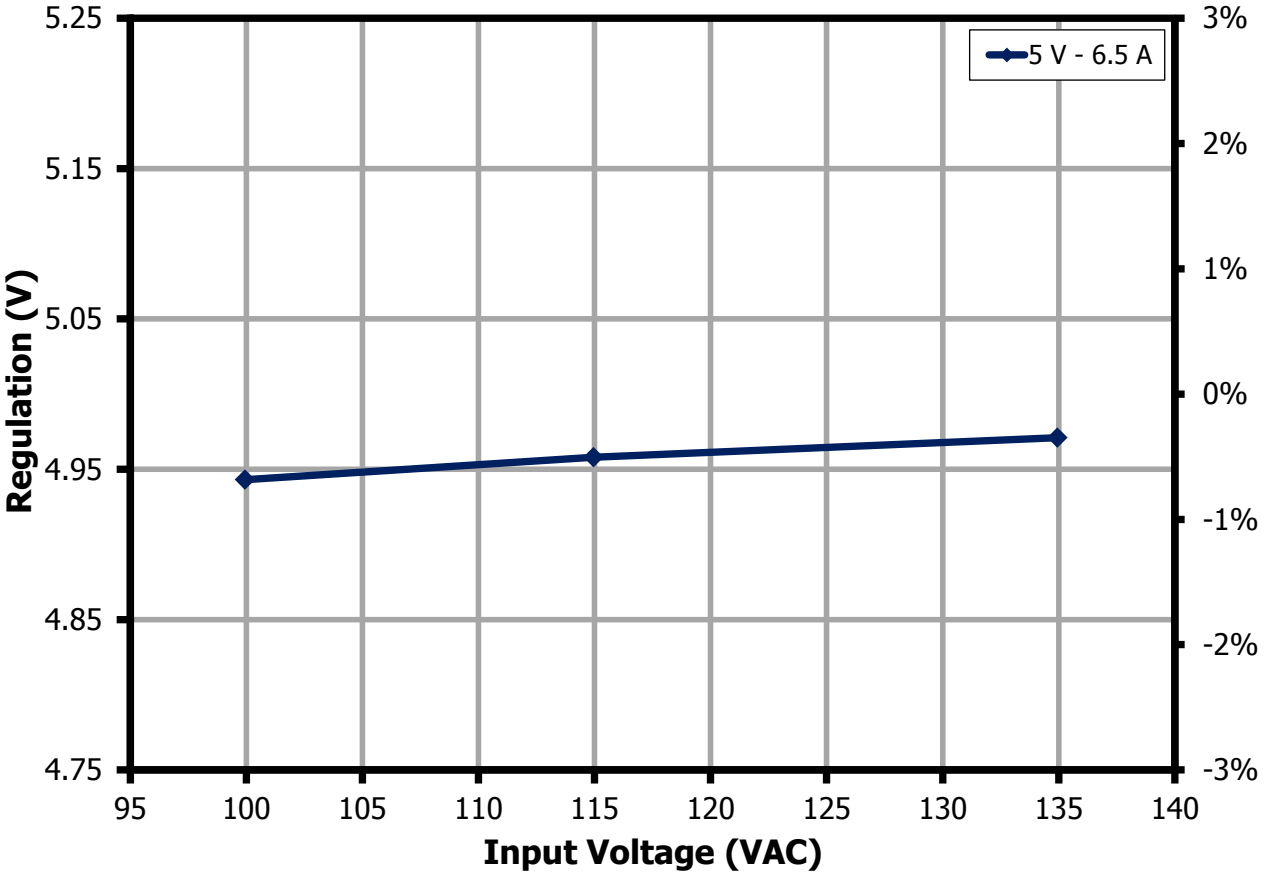

Figure 11 – 5 V Output Regulation vs. Input Line Voltage.

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9.2.2 9 V Line Regulation at 5 A Load

Note: Output voltage measured at PCB end.

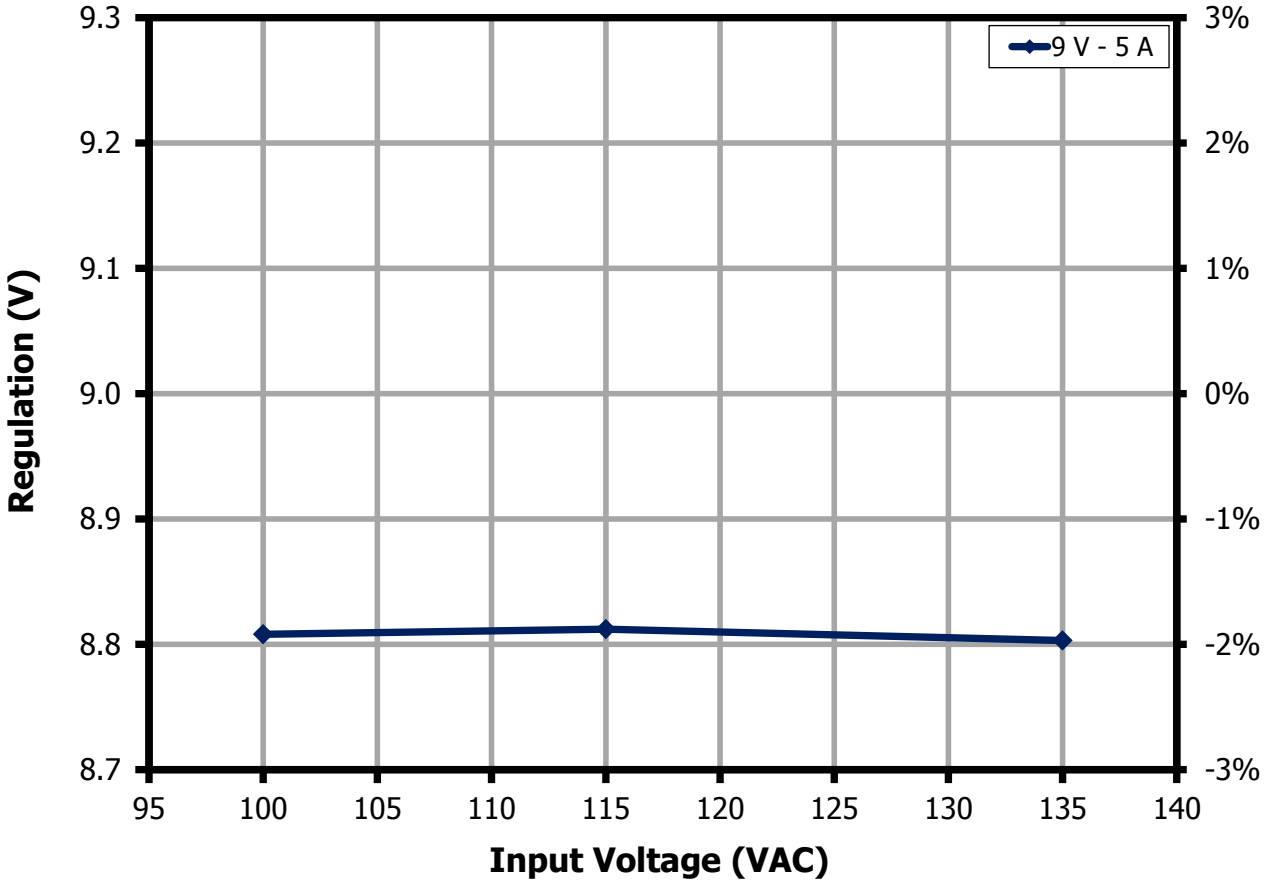

Figure 12 – 9 V Output Regulation vs. Input Line Voltage.

9.2.3 15 V Line Regulation at 3 A Load

Note: Output voltage measured at PCB end.

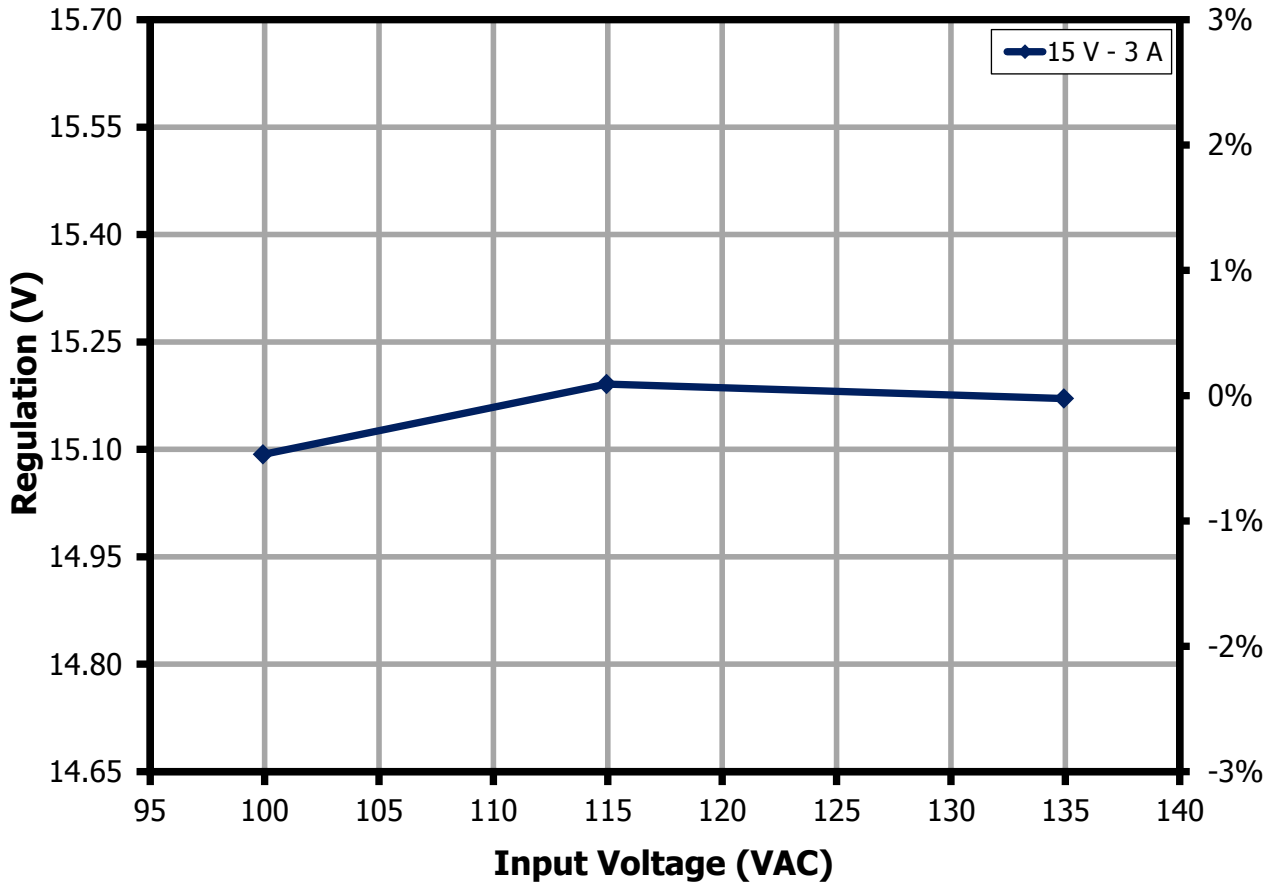

Figure 13 – 15 V Output Regulation vs. Input Line Voltage.

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9.2.4 5 V Load Regulation

Note: Output voltage measured at PCB end.

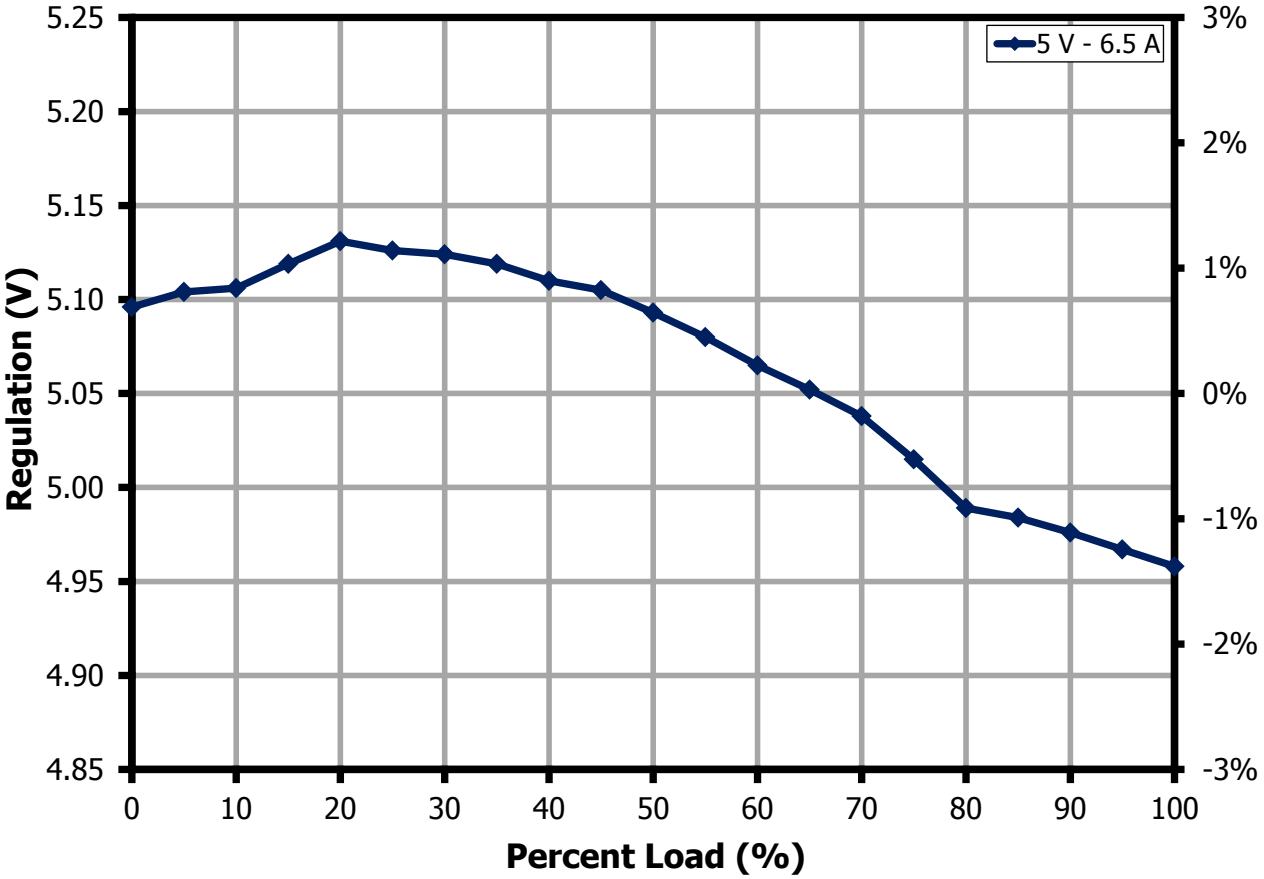

Figure 14 – 5 V Output Regulation vs. Percent Load.

9.2.5 9 V Load Regulation

Note: Output voltage measured at PCB end.

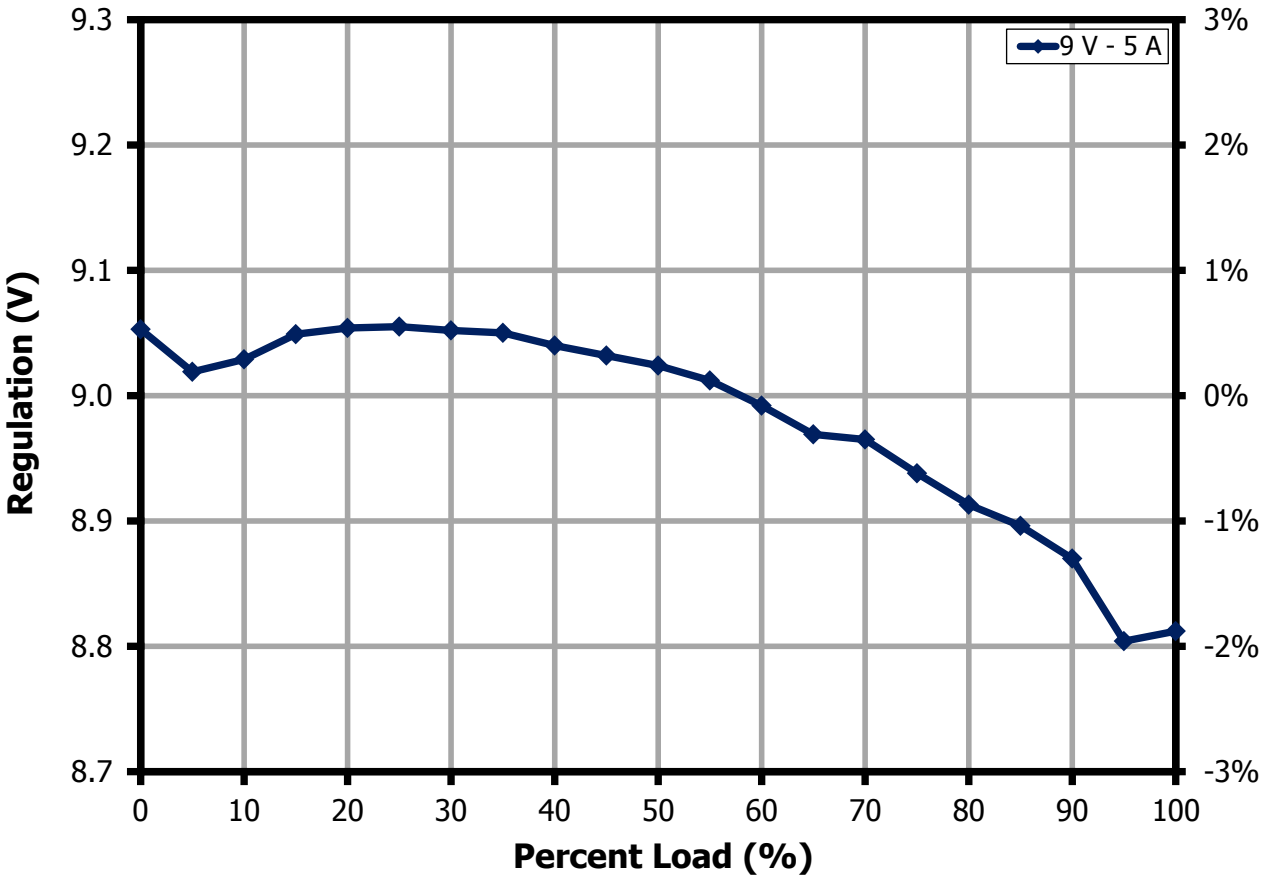

Figure 15 – 9 V Output Regulation vs. Percent Load.

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9.2.6 15 V Load Regulation

Note: Output voltage measured at PCB end.

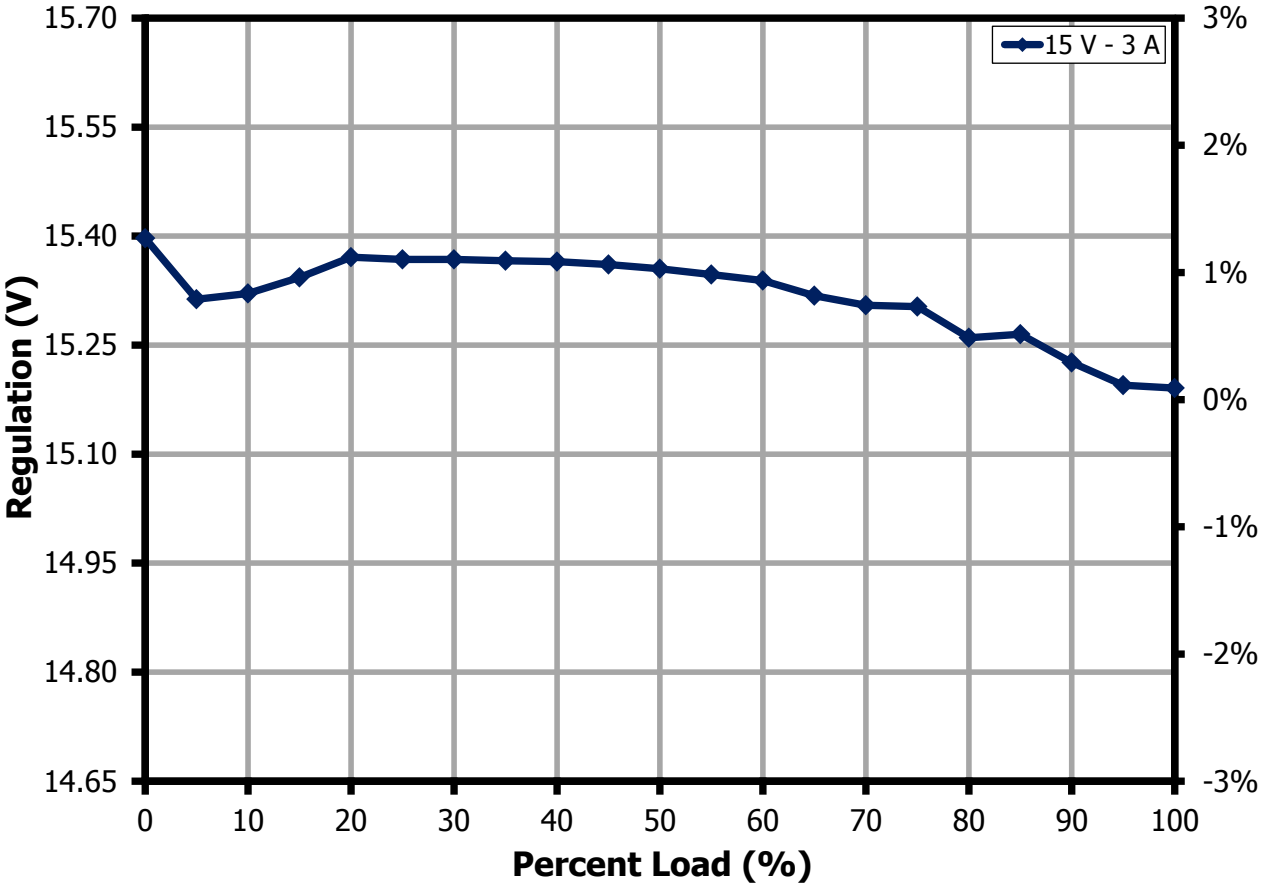

Figure 16 – 15 V Output Regulation vs. Percent Load.

9.2.7 CP Profile vs. Line (5 V / 6.5 A)

Note: Output voltage measured at PCB end.

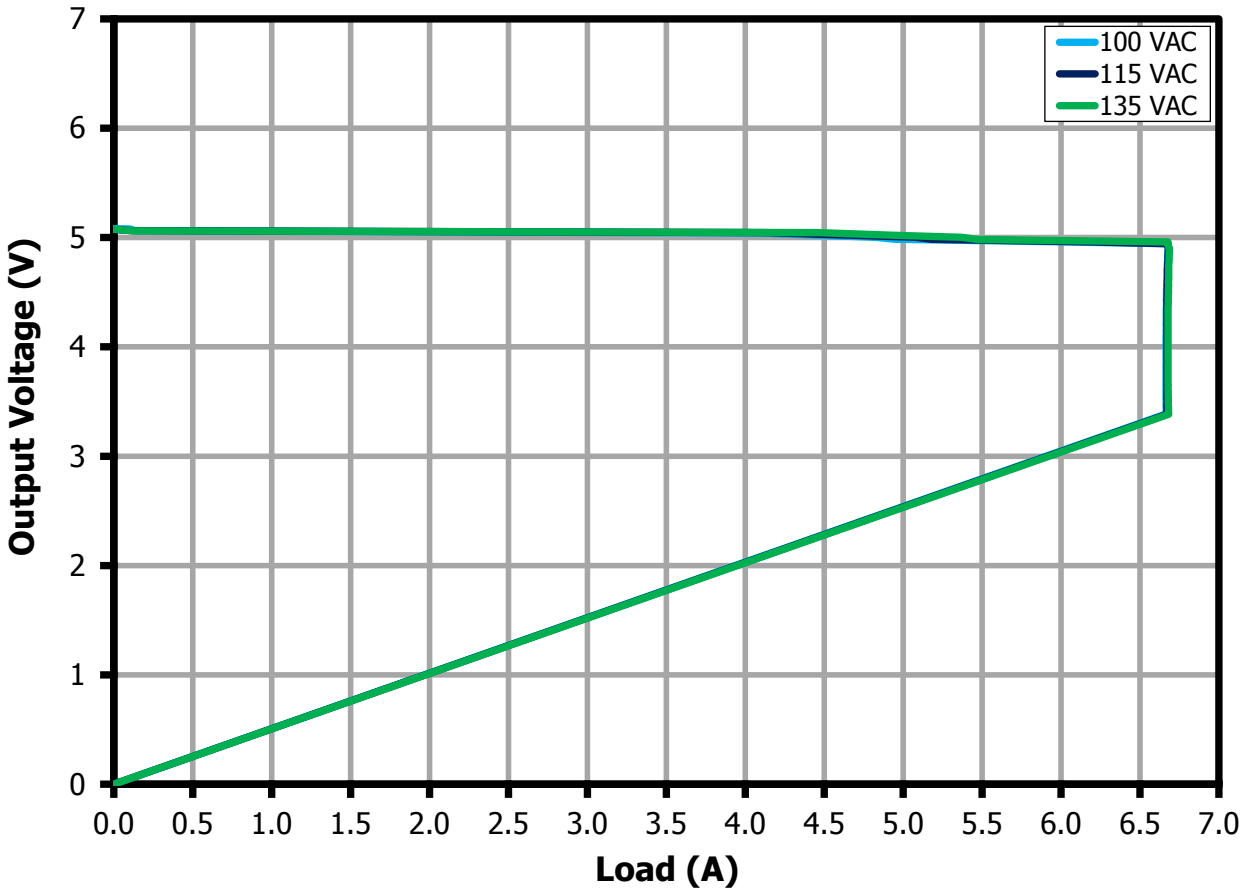

Figure 17 – CP Profile for 5 V Output at Different Input Line.

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9.2.8 CP Profile vs. Line (9 V / 5 A)

Note: Output voltage measured at PCB end.

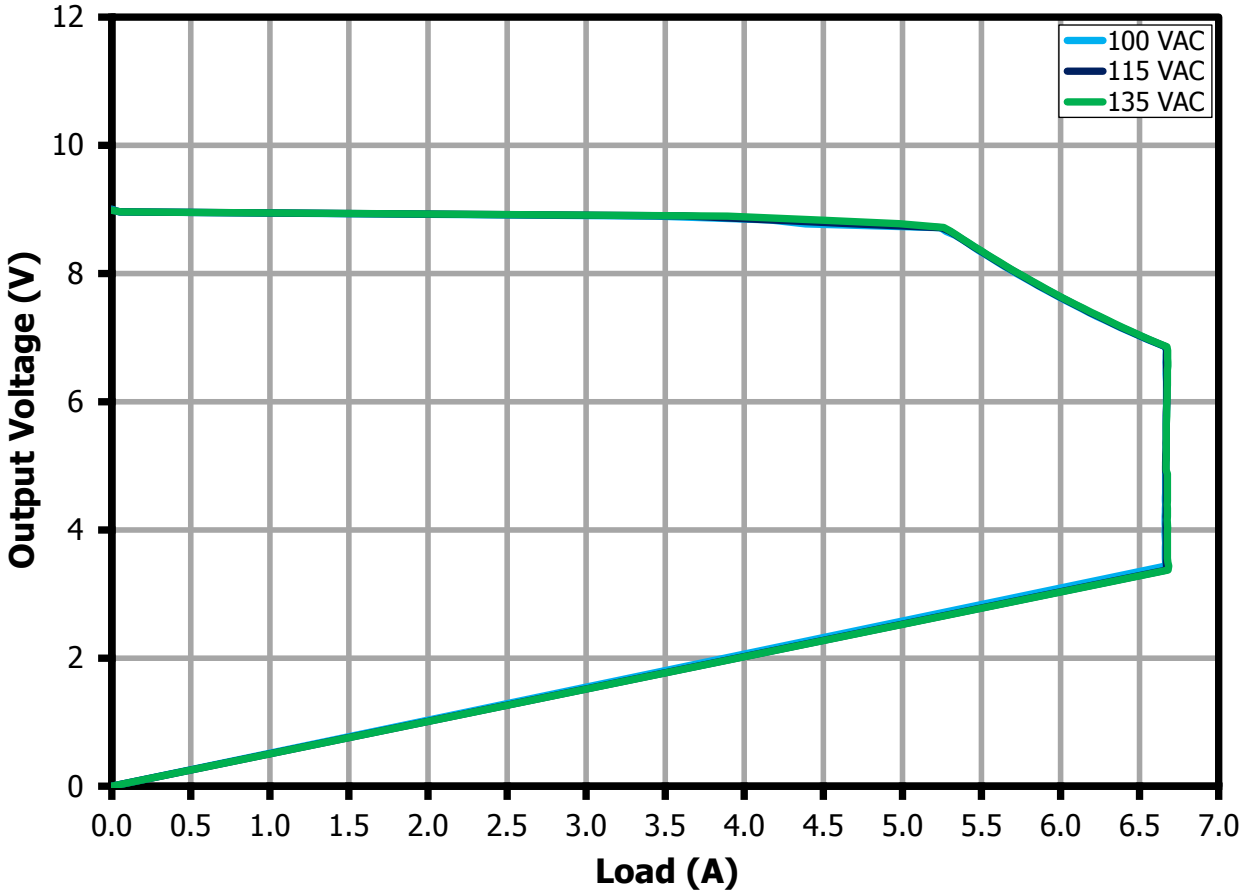

Figure 18 – CP Profile for 9 V Output at Different Input Line.

9.2.9 CP Profile vs. Line (15 V / 3 A)

Note: Output voltage measured at PCB end.

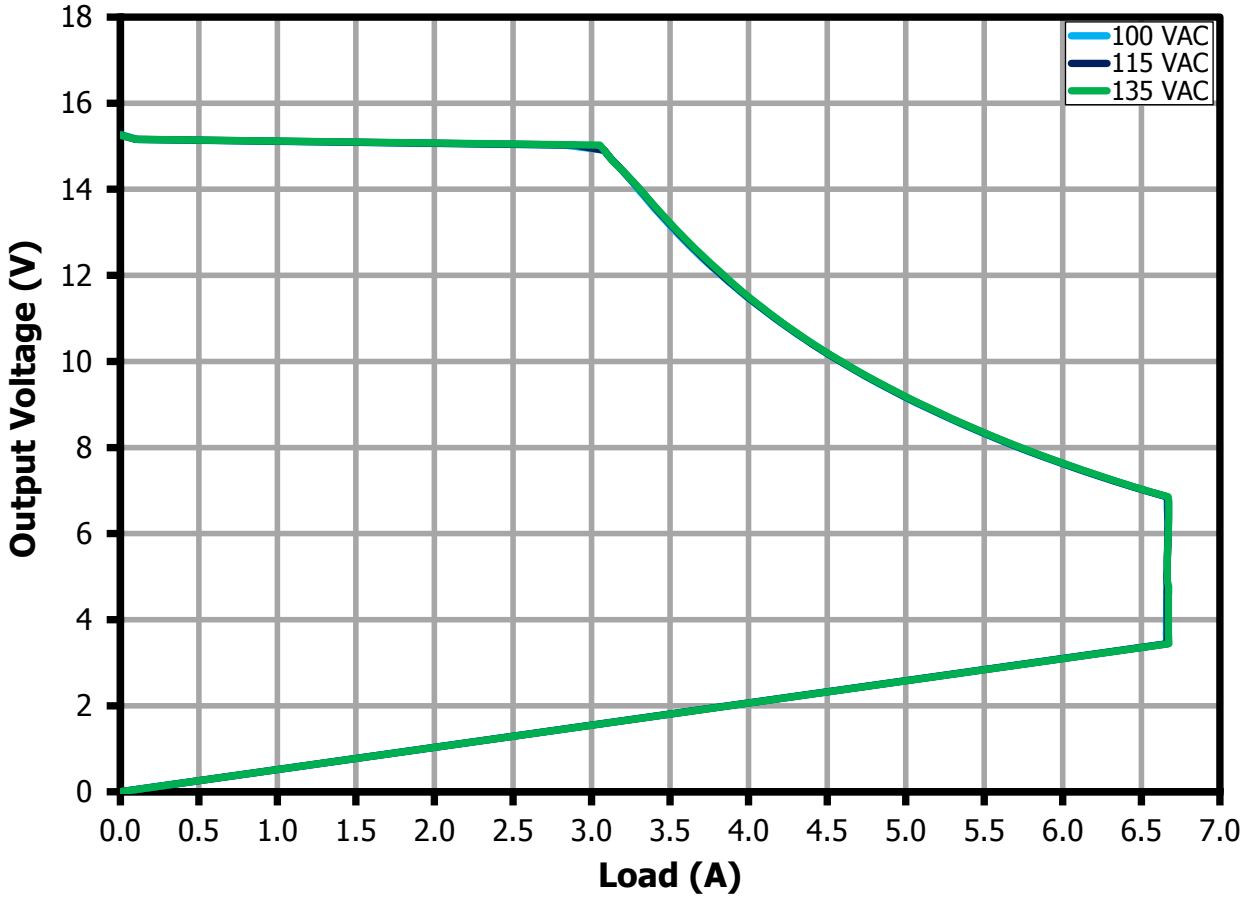

Figure 19 – CP Profile for 15 V Output at Different Input Line.

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10 Test Data

10.1 *Test Data Efficiency vs. Line, 5 V / 6.5 A (PCB End)*

Input		Input Measurement			5 V / 6.5 A			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
100	60	100	681.2	35.63	4.94	6498	32.123	90.2
115	60	115	629.0	35.61	4.96	6498	32.217	90.5
135	60	135	576.5	35.66	4.97	6498	32.301	90.6

10.2 *Test Data Efficiency vs. Line, 9 V / 5 A (PCB End)*

Input		Input Measurement			9 V / 5 A			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
100	60	100	875.5	48.10	8.81	4999	44.026	91.5
115	60	115	799.1	47.88	8.81	4999	44.050	92.0
135	60	135	723.6	47.48	8.80	4999	44.006	92.7

10.3 *Test Data Efficiency vs. Line, 15 V / 3 A (PCB End)*

Input		Input Measurement			15 V / 3 A			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
100	60	100	886.1	48.94	15.09	2999	45.262	92.5
115	60	115	813.7	49.08	15.19	2999	45.558	92.8
135	60	135	739.6	48.89	15.17	2999	45.496	93.1

10.4 *Test Data Efficiency vs Percent Load, 5 V / 6.5 A @ 115 VAC (PCB End)*

Load Settings	Input Measurement			5 V / 6.5 A Measurement Variable			Efficiency (%)
% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	
100	115	629.0	35.61	5.0	6498	32.217	90.5
95	115	604.1	33.83	5.0	6173	30.659	90.6
90	115	579.2	32.07	5.0	5849	29.101	90.7
85	115	553.8	30.29	5.0	5524	27.531	90.9
80	115	526.3	28.38	5.0	5199	25.938	91.4
75	115	501.7	26.69	5.0	4874	24.440	91.6
70	115	476.9	25.01	5.0	4549	22.918	91.6
65	115	450.8	23.26	5.1	4224	21.338	91.7
60	115	424.2	21.51	5.1	3899	19.748	91.8
55	115	396.8	19.76	5.1	3574	18.155	91.9
50	115	368.7	18.00	5.1	3249	16.550	91.9
45	115	340.2	16.23	5.1	2925	14.930	92.0
40	115	310.6	14.43	5.1	2600	13.284	92.1
35	115	280.7	12.64	5.1	2274	11.642	92.1
30	115	250.0	10.84	5.1	1950	9.990	92.1
25	115	217.2	9.04	5.1	1625	8.328	92.1
20	115	182.0	7.25	5.1	1300	6.670	92.0
15	115	143.2	5.44	5.1	975	4.990	91.7
10	115	100.9	3.65	5.1	650	3.319	91.0
5	115	0.09	1.87	5.2	0.33	1.68	89.9

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10.5 *Test Data Efficiency vs Percent Load, 9 V / 5 A @ 115 VAC (PCB End)*

Load Settings	Input Measurement			9 V / 5 A Measurement Variable			Efficiency (%)
% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	
100	115	799.1	47.88	8.8	4999	44.050	92.0
95	115	763.8	45.27	8.8	4749	41.811	92.4
90	115	733.2	43.03	8.9	4499	39.902	92.7
85	115	702.3	40.74	8.9	4249	37.796	92.8
80	115	670.1	38.41	8.9	3999	35.644	92.8
75	115	638.3	36.10	8.9	3749	33.507	92.8
70	115	605.9	33.80	9.0	3499	31.370	92.8
65	115	571.8	31.40	9.0	3249	29.141	92.8
60	115	538.0	29.05	9.0	2999	26.970	92.8
55	115	503.6	26.69	9.0	2749	24.775	92.8
50	115	468.1	24.29	9.0	2500	22.555	92.9
45	115	431.5	21.89	9.0	2250	20.317	92.8
40	115	393.6	19.47	9.0	2000	18.074	92.8
35	115	355.0	17.06	9.1	1750	15.831	92.8
30	115	315.3	14.64	9.1	1500	13.575	92.7
25	115	274.7	12.22	9.1	1250	11.317	92.6
20	115	232.2	9.80	9.1	1000	9.052	92.4
15	115	185.3	7.38	9.1	750	6.784	91.9
10	115	132.5	4.96	9.0	500	4.514	91.0
5	115	69.8	2.54	9.0	250	2.254	88.7

10.6 *Test Data Efficiency vs Percent Load, 15 V / 3 A @ 115 VAC (PCB End)*

Load Settings	Input Measurement			15 V / 3 A Measurement Variable			Efficiency (%)
% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	
100	115	813.7	49.08	15.2	2999	45.558	92.8
95	115	781.3	46.64	15.2	2849	43.293	92.8
90	115	748.9	44.29	15.2	2699	41.098	92.8
85	115	718.0	41.94	15.3	2549	38.914	92.8
80	115	683.7	39.47	15.3	2399	36.614	92.8
75	115	651.8	37.12	15.3	2249	34.421	92.7
70	115	617.3	34.66	15.3	2099	32.130	92.7
65	115	583.1	32.23	15.3	1949	29.857	92.6
60	115	548.5	29.81	15.3	1799	27.598	92.6
55	115	512.9	27.36	15.3	1649	25.314	92.5
50	115	476.8	24.90	15.4	1500	23.026	92.5
45	115	439.8	22.45	15.4	1350	20.734	92.4
40	115	401.5	19.99	15.4	1200	18.435	92.2
35	115	362.1	17.52	15.4	1050	16.133	92.1
30	115	322.0	15.06	15.4	900	13.824	91.8
25	115	281.0	12.60	15.4	750	11.521	91.4
20	115	238.4	10.15	15.4	600	9.221	90.9
15	115	191.1	7.67	15.3	450	6.903	90.0
10	115	138.5	5.22	15.3	300	4.595	88.1
5	115	74.5	2.74	15.3	150	2.297	84.0

10.7 *Test Data Average Efficiency, 5 V / 6.5 A @ 115 VAC (PCB End)*

Load Settings	Input Measurement			5 V / 6.5 A Measurement Variable			Efficiency (%)
% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	
100	115	629.0	35.61	5.0	6498	32.217	90.5
75	115	501.7	26.69	5.0	4874	24.440	91.6
50	115	368.7	18.00	5.1	3249	16.550	91.9
25	115	217.2	9.04	5.1	1625	8.328	92.1
AVERAGE							91.5

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10.8 *Test Data Average Efficiency, 9 V / 5 A @ 115 VAC (PCB End)*

Load Settings	Input Measurement			9 V / 5 A Measurement Variable			
% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	115	799.1	47.88	8.8	4999	44.050	92.0
75	115	638.3	36.10	8.9	3749	33.507	92.8
50	115	468.1	24.29	9.0	2500	22.555	92.9
25	115	274.7	12.22	9.1	1250	11.317	92.6
AVERAGE							92.6

10.9 *Test Data Average Efficiency, 15 V / 3 A @ 115 VAC (PCB End)*

Load Settings	Input Measurement			15 V / 3 A Measurement Variable			
% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	115	813.7	49.08	15.2	2999	45.558	92.8
75	115	651.8	37.12	15.3	2249	34.421	92.7
50	115	476.8	24.90	15.4	1500	23.026	92.5
25	115	281.0	12.60	15.4	750	11.521	91.4
AVERAGE							92.4

10.10 *Test Data Line Regulation, 5 V / 6.5 A (PCB End)*

Input		5 V / 6.5 A		
VAC (V_{RMS})	Freq (Hz)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)
100	47	4.9	6498	32.123
115	50	5.0	6498	32.217
135	60	5.0	6498	32.301

10.11 *Test Data Line Regulation, 9 V / 5 A (PCB End)*

Input		9 V / 5 A		
VAC (V_{RMS})	Freq (Hz)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)
100	47	8.8	4999	44.026
115	50	8.8	4999	44.050
135	60	8.8	4999	44.006

10.12 *Test Data Line Regulation, 15 V / 3 A (PCB End)*

Input		15 V / 3 A		
VAC (V_{RMS})	Freq (Hz)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)
100	47	15.1	2999	45.262
115	50	15.2	2999	45.558
135	60	15.2	2999	45.496

10.13 *Test Data Load Regulation, 5 V / 6.5 A @ 115 VAC (PCB End)*

Load Settings	5 V / 6.5 A Measurement Variable		
% Load	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)
100	5.0	6498	32.217
95	5.0	6173	30.659
90	5.0	5849	29.101
85	5.0	5524	27.531
80	5.0	5199	25.938
75	5.0	4874	24.440
70	5.0	4549	22.918
65	5.1	4224	21.338
60	5.1	3899	19.748
55	5.1	3574	18.155
50	5.1	3249	16.550
45	5.1	2925	14.930
40	5.1	2600	13.284
35	5.1	2274	11.642
30	5.1	1950	9.990
25	5.1	1625	8.328
20	5.1	1300	6.670
15	5.1	975	4.990
10	5.1	650	3.319
5	5.1	325	1.658
0	5.1	0.13	0.000

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10.14 *Test Data Load Regulation, 9 V / 5 A @ 115 VAC (PCB End)*

Load Settings	9 V / 5 A Measurement Variable		
% Load	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)
100	8.8	4999	44.050
95	8.8	4749	41.811
90	8.9	4499	39.902
85	8.9	4249	37.796
80	8.9	3999	35.644
75	8.9	3749	33.507
70	9.0	3499	31.370
65	9.0	3249	29.141
60	9.0	2999	26.970
55	9.0	2749	24.775
50	9.0	2500	22.555
45	9.0	2250	20.317
40	9.0	2000	18.074
35	9.1	1750	15.831
30	9.1	1500	13.575
25	9.1	1250	11.317
20	9.1	1000	9.052
15	9.0	750	6.784
10	9.0	500	4.514
5	9.0	250	2.254
0	9.1	0.10	0.000

10.15 *Test Data Load Regulation, 15 V / 3 A @ 115 VAC (PCB End)*

Load Settings	15 V / 3 A Measurement Variable		
% Load	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)
100	15.2	2999	45.558
95	15.2	2849	43.293
90	15.2	2699	41.098
85	15.3	2549	38.914
80	15.3	2399	36.614
75	15.3	2249	34.421
70	15.3	2099	32.130
65	15.3	1949	29.857
60	15.3	1799	27.598
55	15.3	1649	25.314
50	15.4	1500	23.026
45	15.4	1359	20.734
40	15.4	1200	18.435
35	15.4	1050	16.133
30	15.4	900	13.824
25	15.4	750	11.521
20	15.4	600	9.221
15	15.3	450	6.903
10	15.3	300	4.595
5	15.3	150	2.297
0	15.4	0.02	0.000

10.16 *Test Data No-Load Consumption, 5 V / 0 A (PCB End)*

Input		Input Measurement		
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (mW)
100	60	100	31.7	7.23
110	60	110	31.3	9.22
115	60	115	31.8	9.04
120	60	120	31.1	9.70
135	60	135	30.5	13.63

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11 Thermal Performance

11.1 *Open Case at 15 V / 3 A (25 ºC Ambient)*

11.1.1 100 VAC @ 25 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge Diode (BR1)
24.3	76.1	72	76.1	69.9

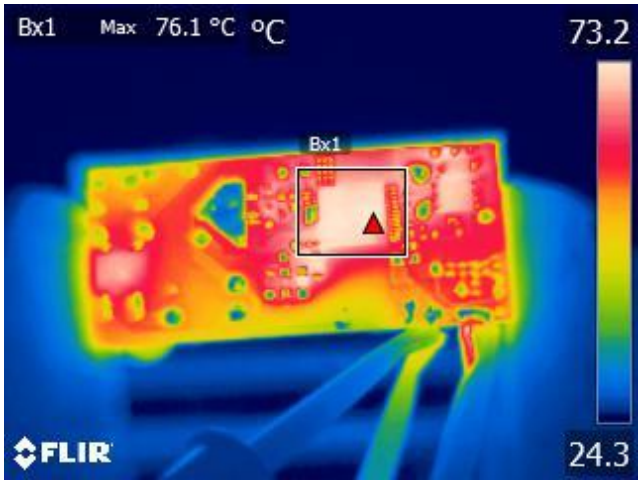

Figure 20 – Ambient = 24.3 ºC.
INN3279C, U1 = 76.1 ºC.

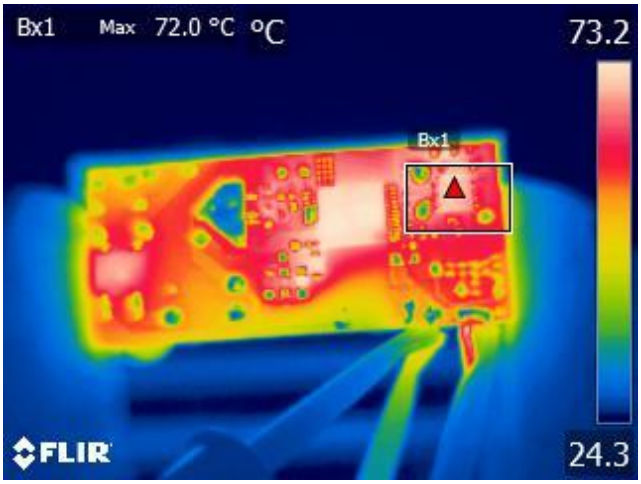

Figure 21 – Ambient = 24.3 ºC.
SR FET, Q3 = 72 ºC.

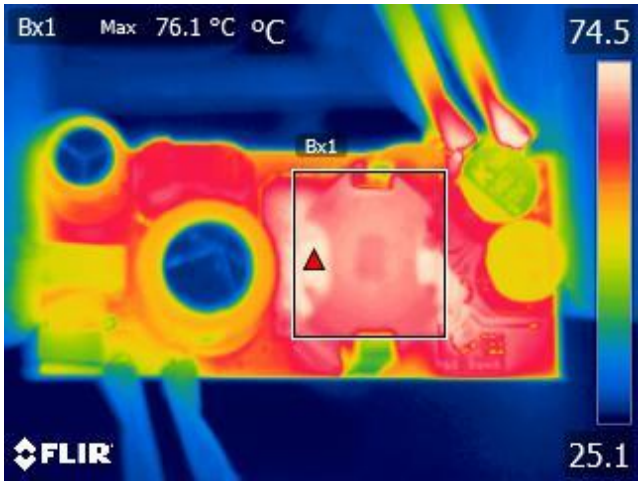

Figure 22 – Ambient = 25.1 ºC.
Transformer, T2 = 76.1 ºC.

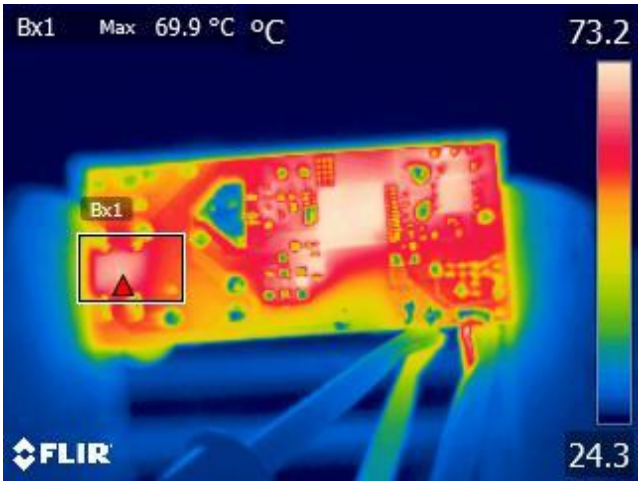

Figure 23 – Ambient = 24.3 ºC.
Bridge Diode, BR1 = 69.9 ºC.

11.1.2 135 VAC @ 25 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge Diode (BR1)
24.7	76	74.4	79	59.8

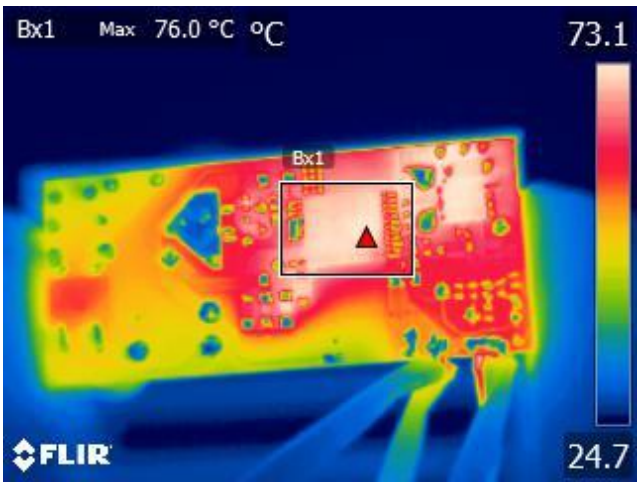

Figure 24 – Ambient = 24.7 ºC.
INN3279C, U1 = 76 ºC.

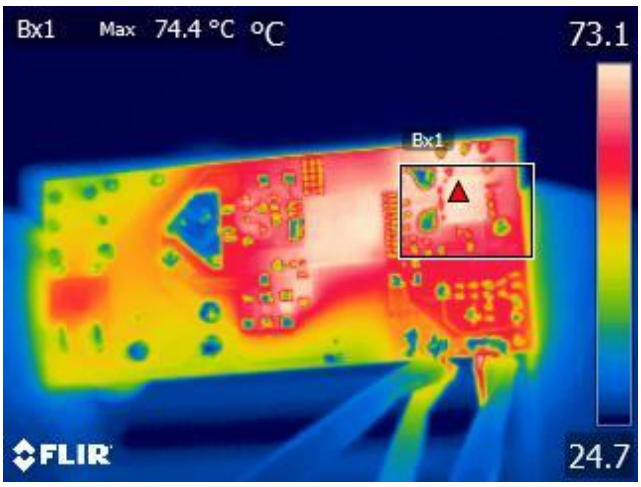

Figure 25 – Ambient = 24.7 ºC.
SR FET, Q3 = 74.4 ºC.

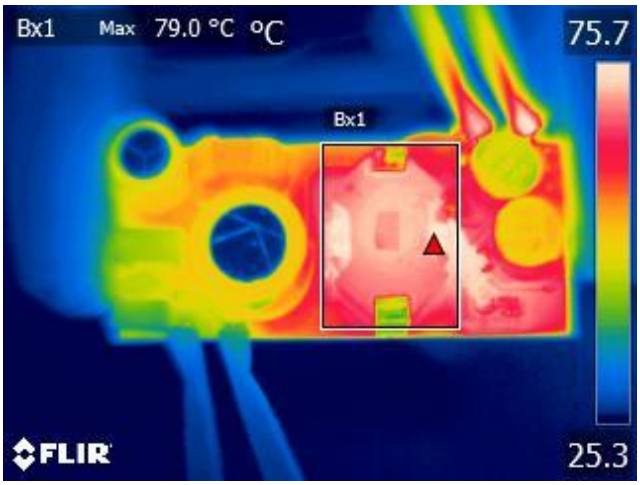

Figure 26 – Ambient = 25.3 ºC.
Transformer, T2 = 79 ºC.

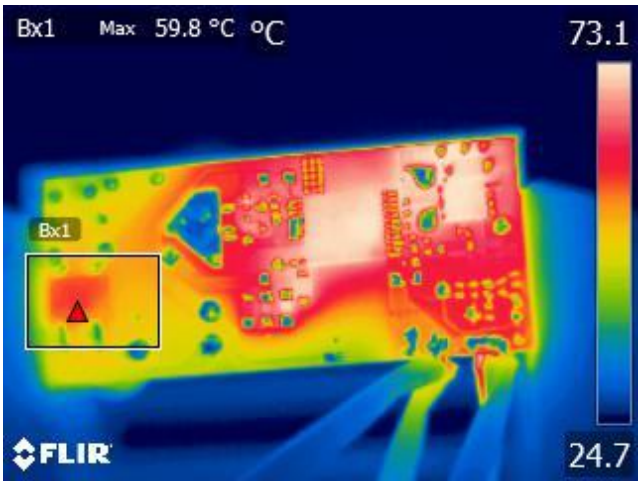

Figure 27 – Ambient = 24.7 ºC.
Bridge Diode, BR1 = 59.8 ºC.

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11.2 *Open Case at 9 V / 5 A (25 ºC Ambient)*

11.2.1 100 VAC @ 25 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge Diode (BR1)
25.7	93.8	90	81.9	73.5

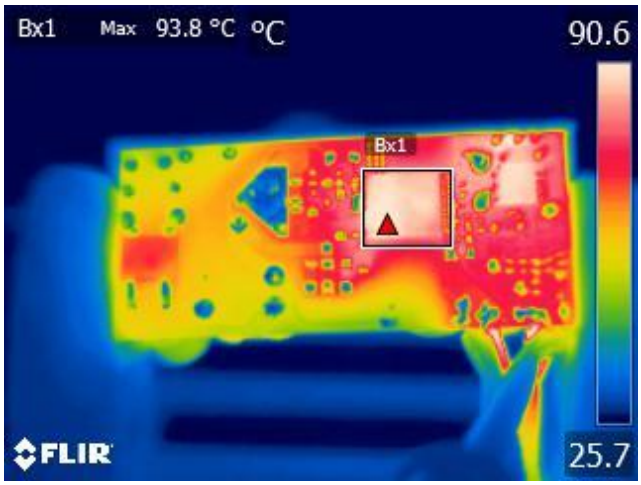

Figure 28 – Ambient = 25.7 ºC.
INN3168C, U1 = 93.8 ºC.

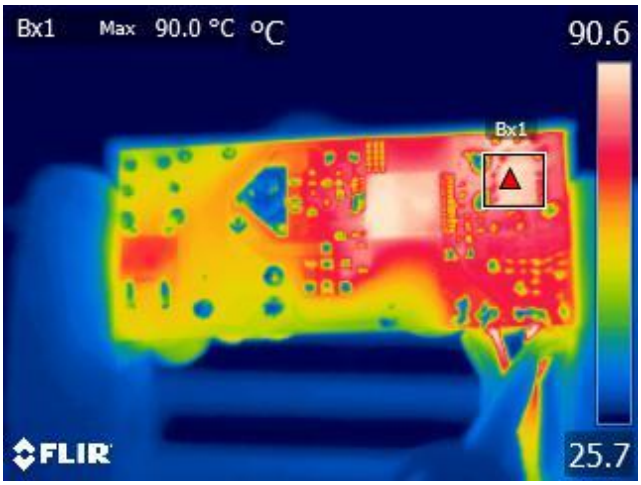

Figure 29 – Ambient = 25.7 ºC.
SR FET, Q3 = 90 ºC.

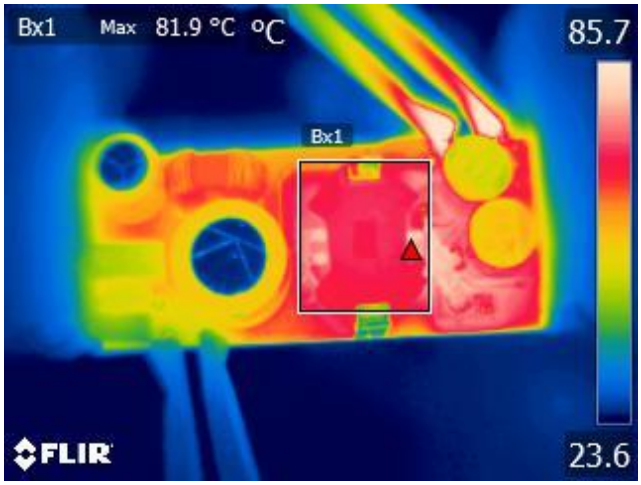

Figure 30 – Ambient = 23.6 ºC.
Transformer, T2 = 81.9 ºC.

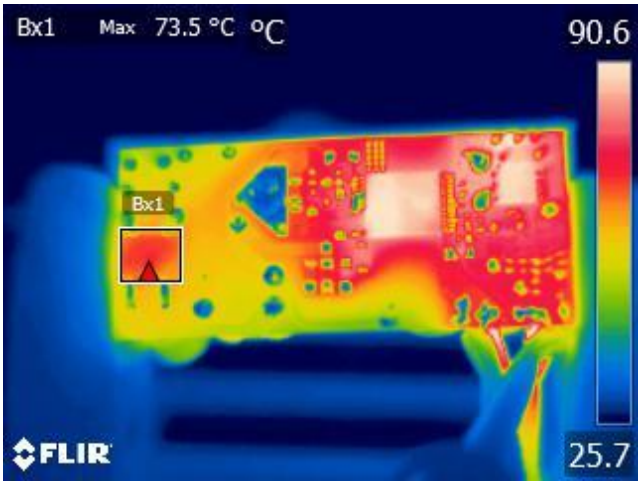

Figure 31 – Ambient = 25.7 ºC.
Bridge Diode, BR1 = 73.5 ºC.

11.2.2 135 VAC @ 25 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge Diode (BR1)
23.7	87.2	87.5	83.4	60.2

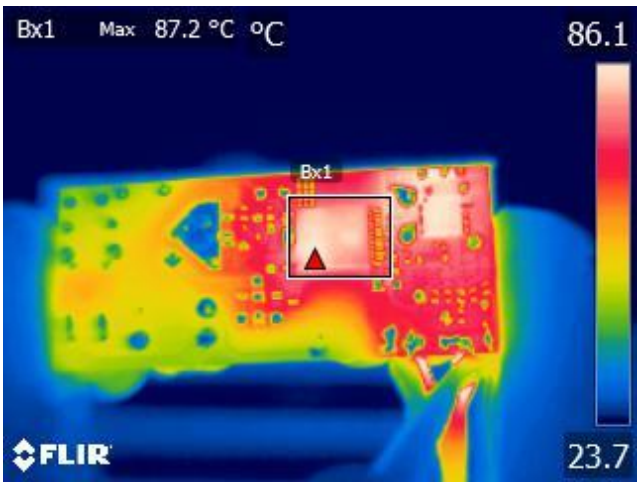

Figure 32 – Ambient = 23.7 ºC.
INN3279C, U1 = 87.2 ºC.

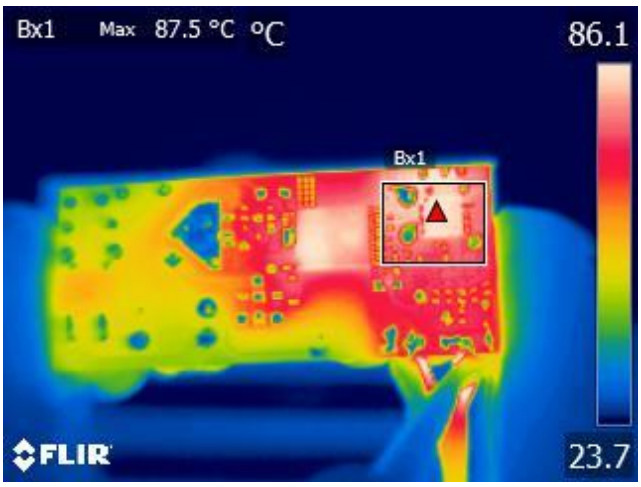

Figure 33 – Ambient = 23.7 ºC.
SR FET, Q3 = 87.5 ºC.

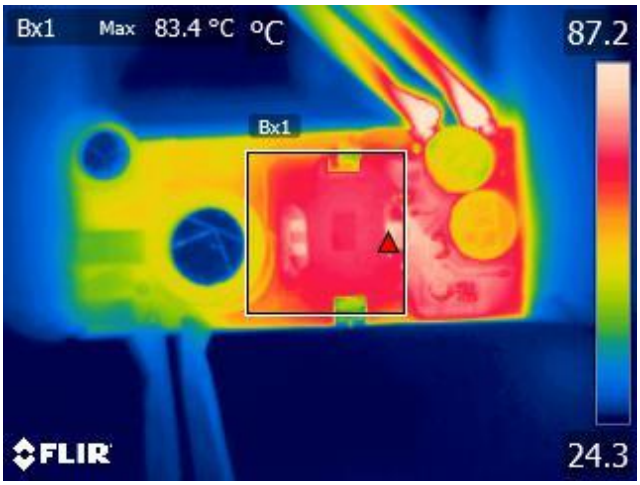

Figure 34 – Ambient = 24.3 ºC.
Transformer, T2 = 83.4 ºC.

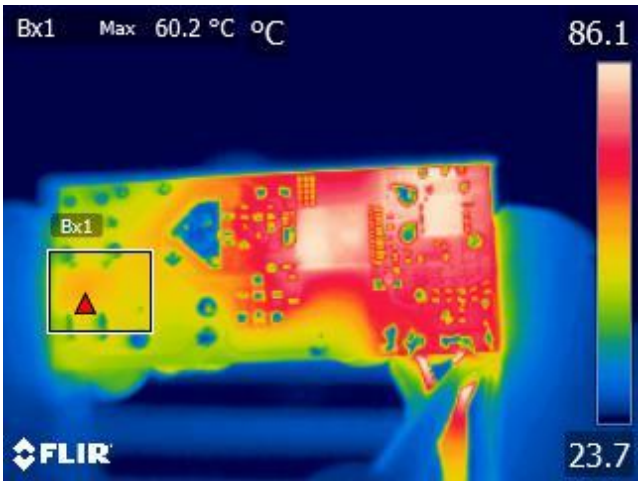

Figure 35 – Ambient = 23.7 ºC.
Bridge Diode, BR1 = 60.2 ºC.

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11.3 *Open Case at 5 V / 6.5 A (25 ºC Ambient)*

11.3.1 100 VAC @ 25 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge Diode (BR1)
22.5	78.1	85.4	79.5	57.8

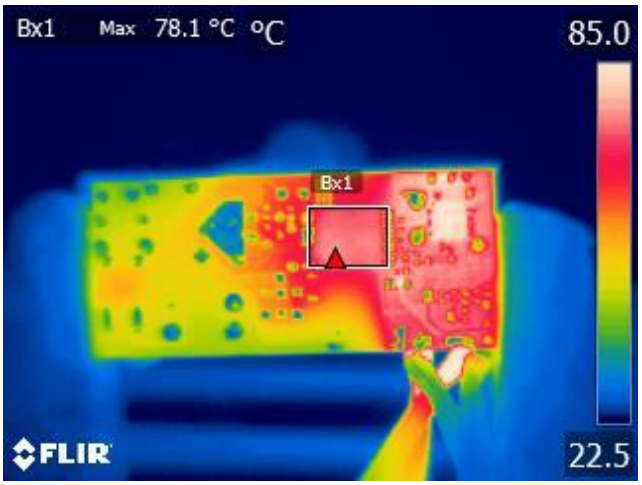

Figure 36 – Ambient = 22.5 ºC.
INN3279C, U1 = 78.1 ºC.

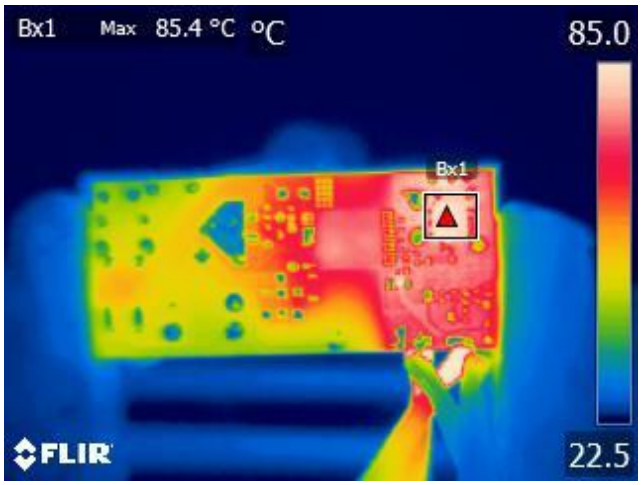

Figure 37 – Ambient = 22.5 ºC.
SR FET, Q3 = 85.4 ºC.

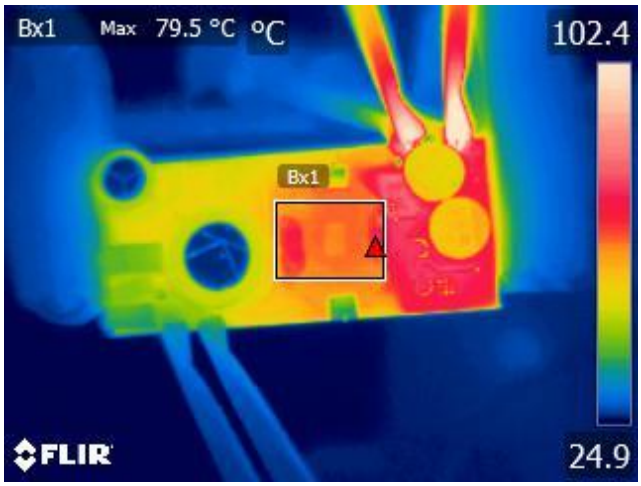

Figure 38 – Ambient = 24.9 ºC.
Transformer, T2 = 79.5 ºC.

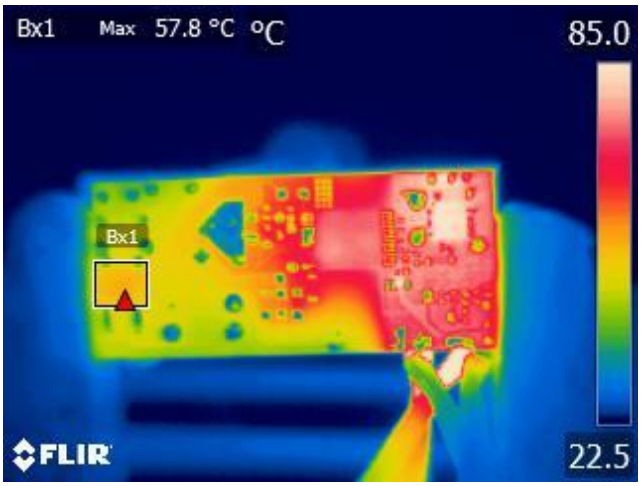

Figure 39 – Ambient = 22.5 ºC.
Bridge Diode, BR1 = 57.8 ºC.

11.3.2 135 VAC @ 25 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR MOSFET (Q3)	Transformer (T2)	Bridge Diode (BR1)
24.6	82	88.1	81	53.3

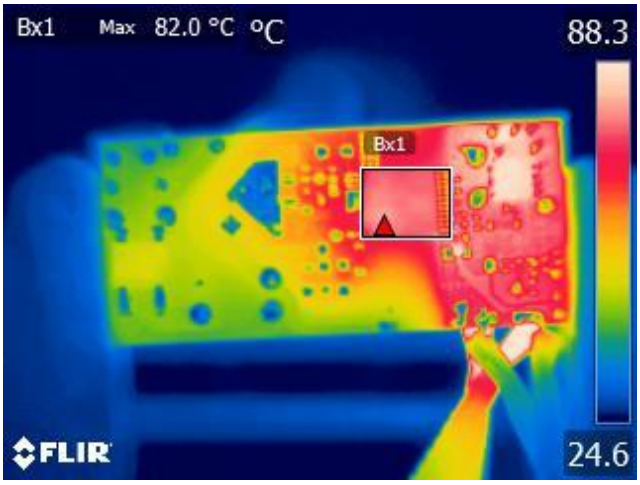

Figure 40 – Ambient = 24.6 ºC.
INN3279C, U1 = 82 ºC.

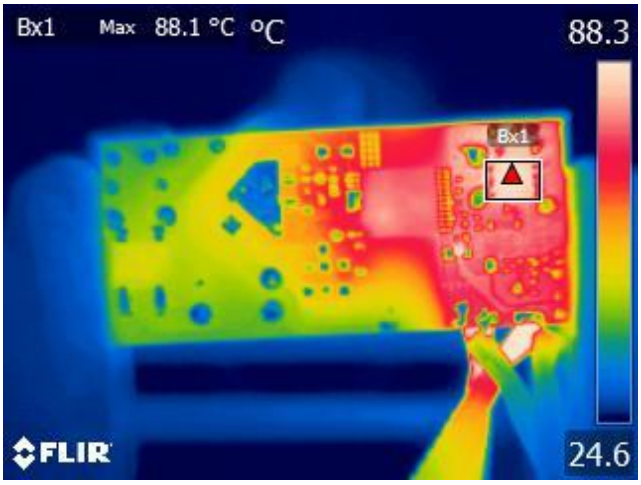

Figure 41 – Ambient = 24.6 ºC.
SR FET, Q3 = 88.1 ºC.

Figure 42 – Ambient = 25 ºC.
Transformer, T2 = 81 ºC.

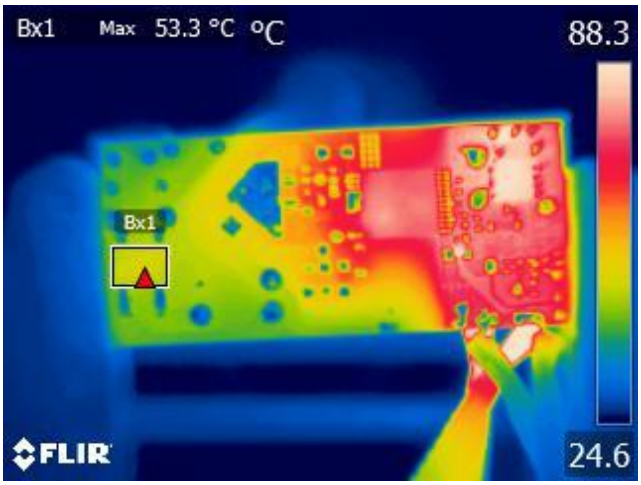

Figure 43 – Ambient = 24.6 ºC.
Bridge Diode, BR1 = 53.3 ºC.

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11.4 *Open Case at 5 V / 6.5 A (50 ºC Ambient)*

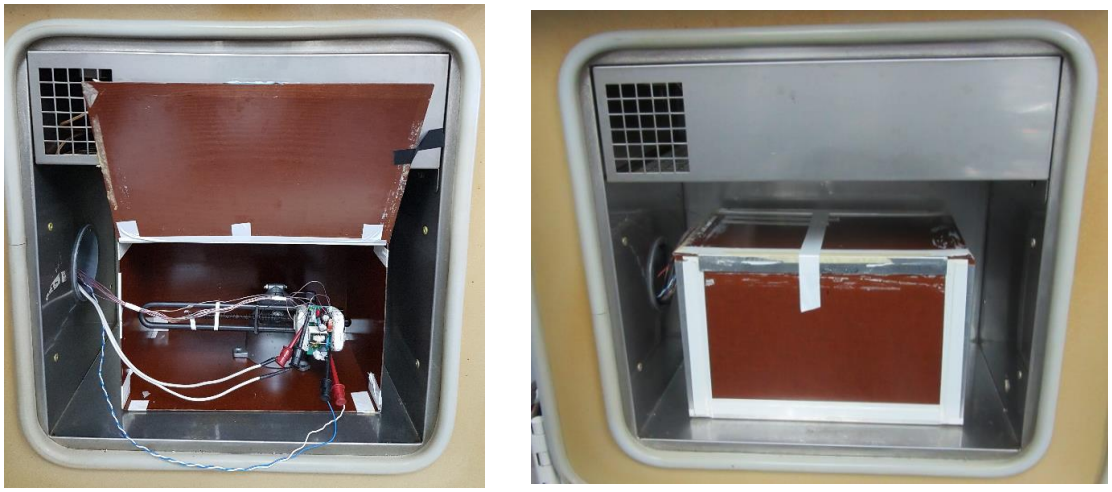
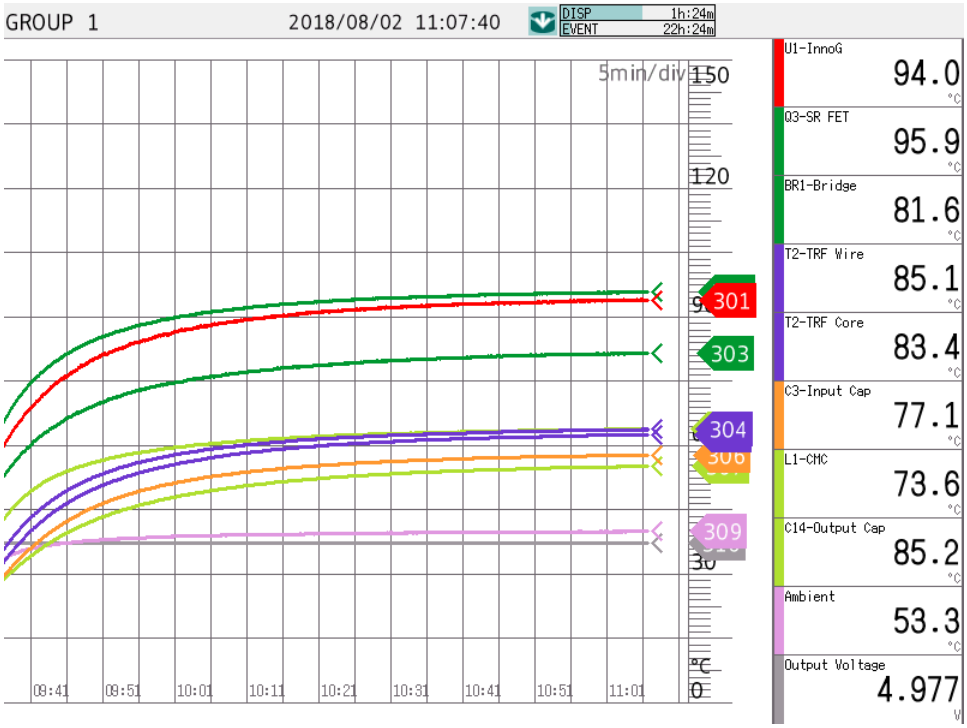


Figure 44 – Test Set-up Picture.

Unit was placed inside a box enclosure to prevent airflow that might affect the thermal measurements. Ambient temperature was set to 50 ºC. Temperature was measured using type T thermocouple.

11.4.1 100 VAC @ 50 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
53.3	94.0	95.9	85.1	81.6	73.6	77.1	85.2



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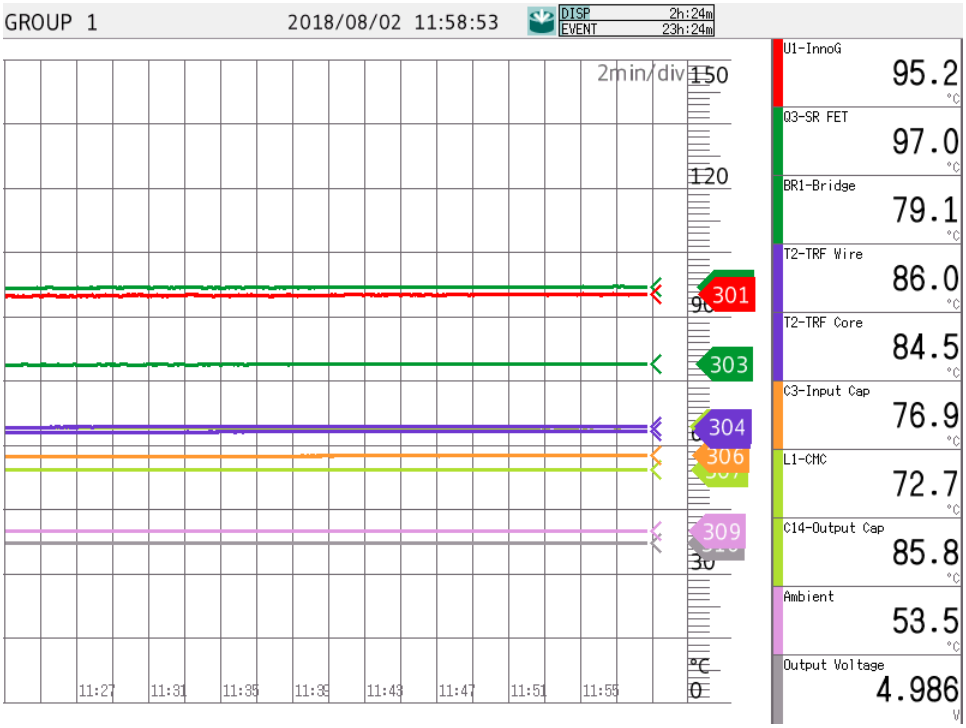
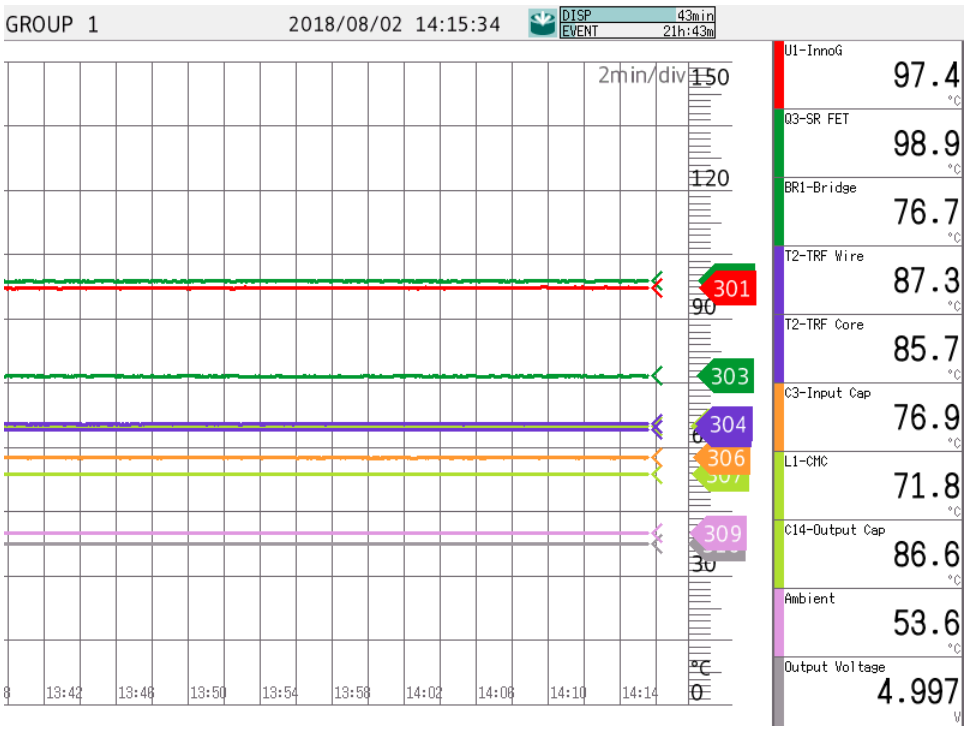
11.4.2 115 VAC @ 50 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
53.5	95.2	97.0	86.0	79.1	72.7	76.9	85.8



11.4.3 135 VAC @ 50 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
53.6	97.4	98.9	87.3	76.7	71.8	76.9	86.6



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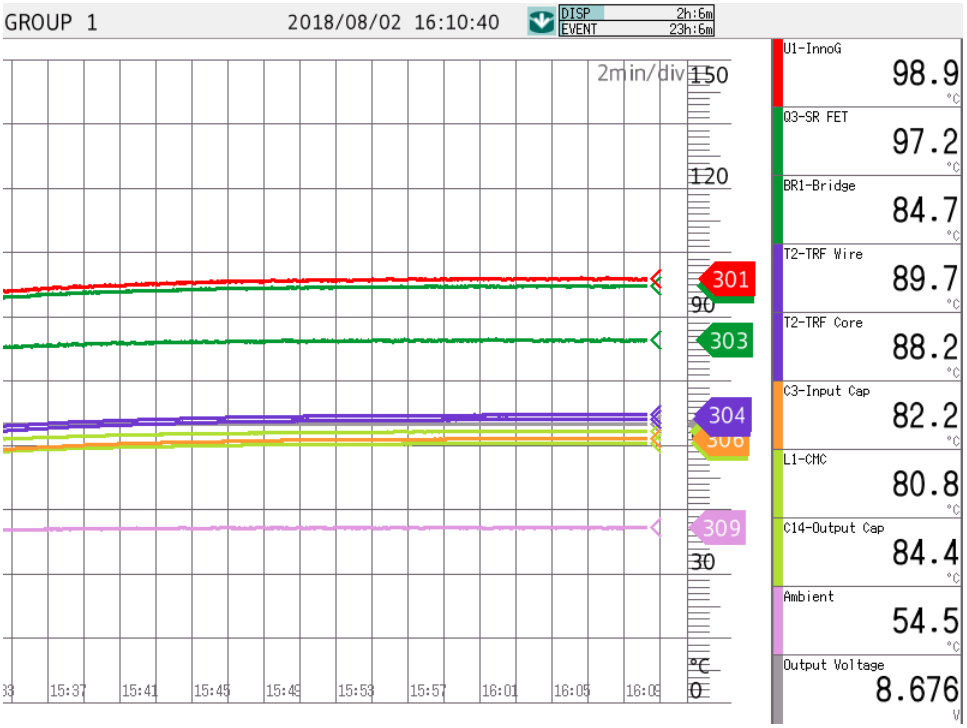
11.5 *Open Case at 9 V / 5 A (50 ºC Ambient)*

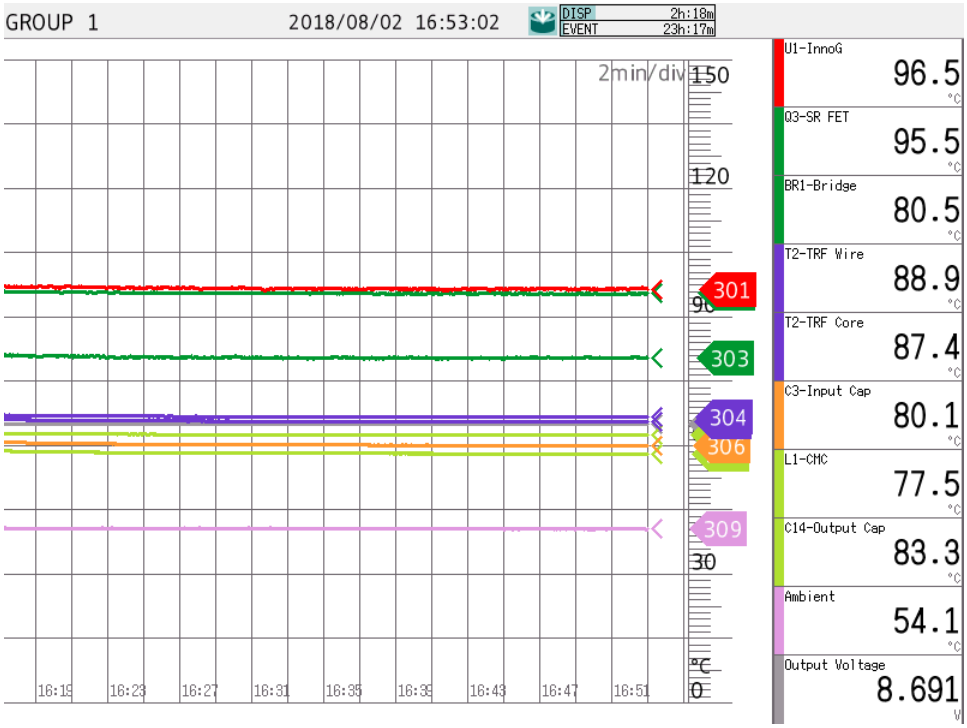
11.5.1 100 VAC @ 50 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
54.5	98.9	97.2	89.7	84.7	80.8	82.2	84.4



11.5.2 115 VAC @ 50 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
54.1	96.5	95.5	88.9	80.5	77.5	80.1	83.3



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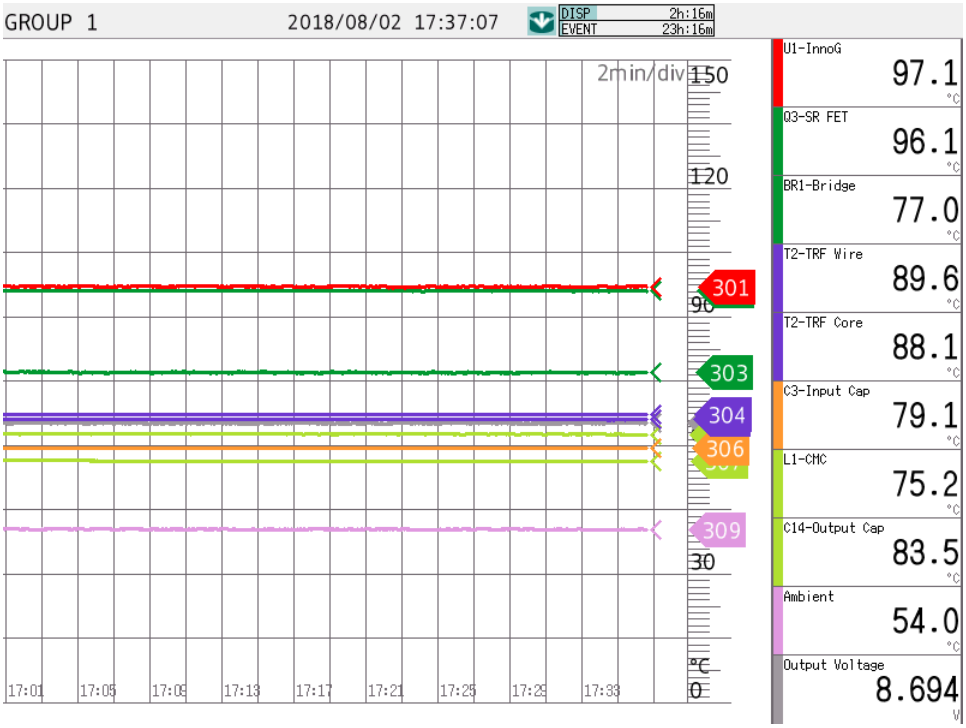
11.5.3 135 VAC @ 50 ºC Ambient

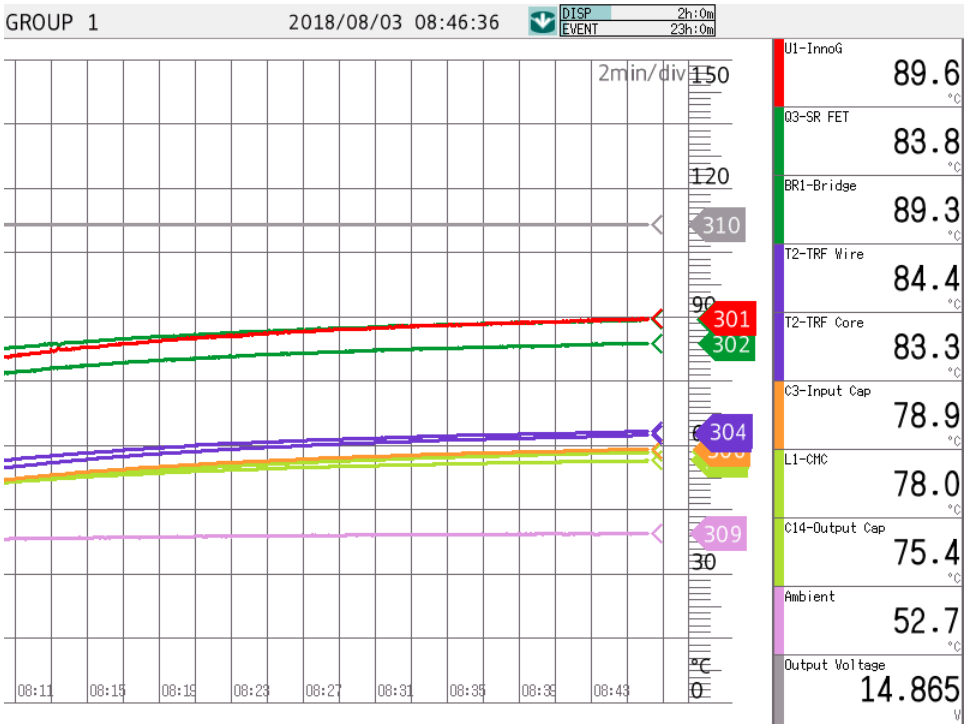
Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
54.0	97.1	96.1	89.6	77.0	75.2	79.1	83.5



11.6 *Open Case at 15 V / 3 A (50°C Ambient)*

11.6.1 100 VAC @ 50 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
52.7	89.6	83.8	84.4	89.3	78.0	78.9	75.4



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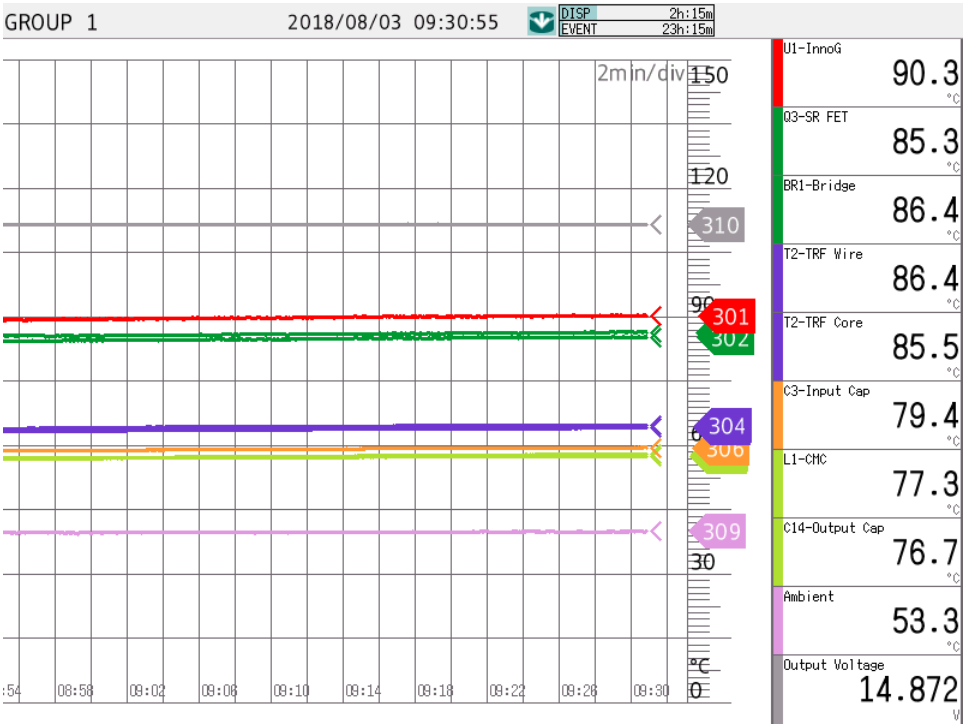
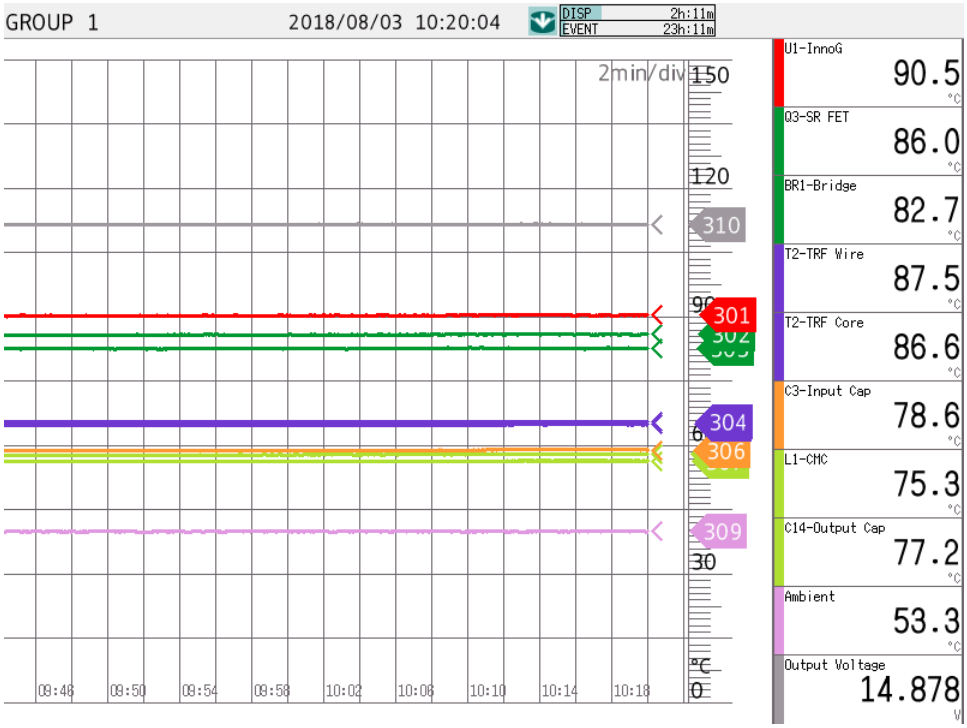
11.6.2 115 VAC @ 50 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
53.3	90.3	85.3	86.4	86.4	77.3	79.4	76.7



11.6.3 135 VAC @ 50 ºC Ambient

Ambient (ºC)	INN3279C (U1)	SR MOSFET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
53.3	90.5	86.0	87.5	82.1	75.3	78.6	77.2



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12 Waveforms

12.1 *Load Transient Response (PCB End)*

12.1.1 5 V Output

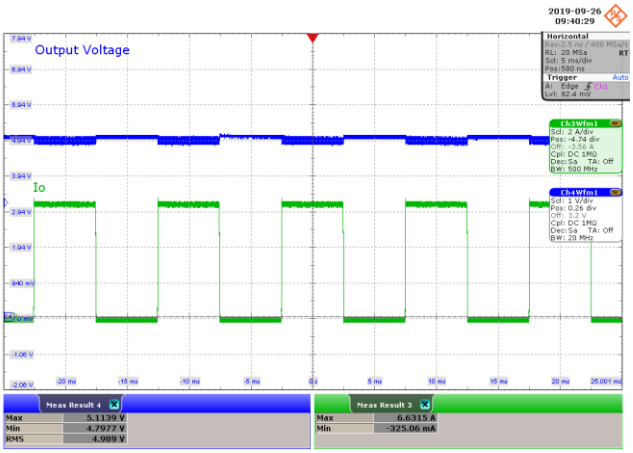

Figure 45 – Transient Response.
100 VAC, 5 V, 0 – 6.5 A Load Step.
V_{MIN}: 4.797 V, V_{MAX}: 5.113 V.
Upper: V_{OUT}, 1 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

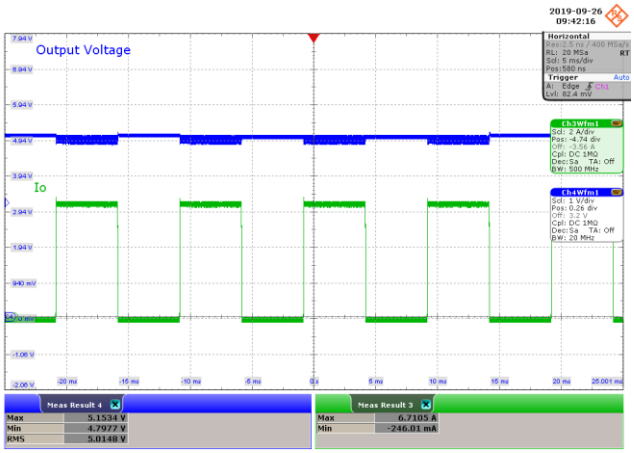

Figure 46 – Transient Response.
135 VAC, 5 V, 0 – 6.5 A Load Step.
V_{MIN}: 4.797 V, V_{MAX}: 5.153 V.
Upper: V_{OUT}, 1 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

12.1.2 9 V Output

Figure 47 – Transient Response.
100 VAC, 9 V, 0 – 5 A Load Step.
V_{MIN}: 8.605 V, V_{MAX}: 9.000 V.
Upper: V_{OUT}, 1 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

Figure 48 – Transient Response.
135 VAC, 9 V, 0 – 5 A Load Step.
V_{MIN}: 8.605 V, V_{MAX}: 9.000 V.
Upper: V_{OUT}, 1 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

12.1.3 15 V Output

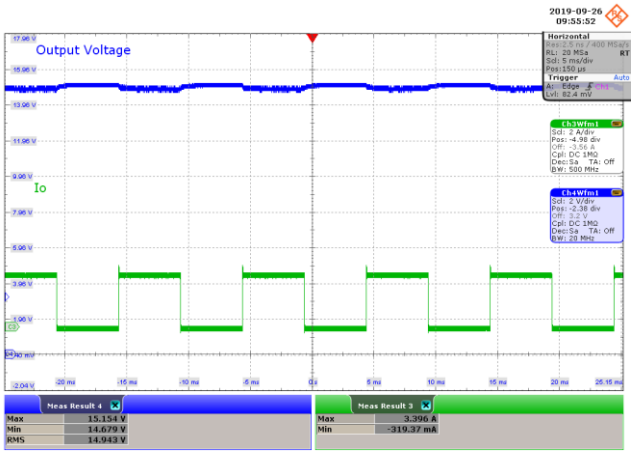

Figure 49 – Transcient Response.
100 VAC, 15 V, 0 – 3 A Load Step.
V_{MIN}: 14.679 V, V_{MAX}: 15.154 V.
Upper: V_{OUT}, 2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

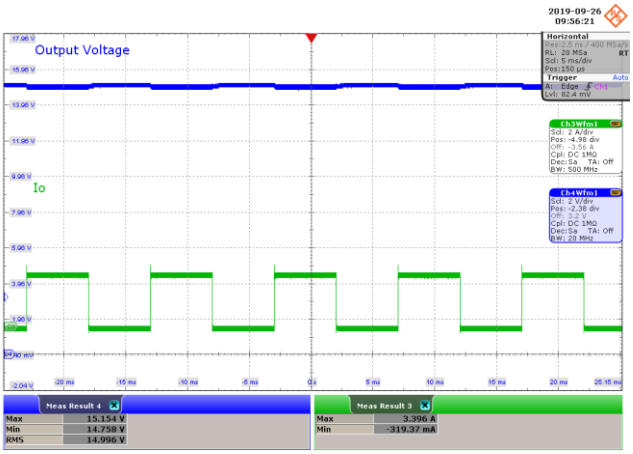

Figure 50 – Transient Response.
135 VAC, 15 V, 0 – 3 A Load Step.
V_{MIN}: 14.758 V, V_{MAX}: 15.154 V.
Upper: V_{OUT}, 2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

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12.2 *Switching Waveforms*

12.2.1 Drain Voltage and Current (Normal Operation)

12.2.1.1 5 V Output

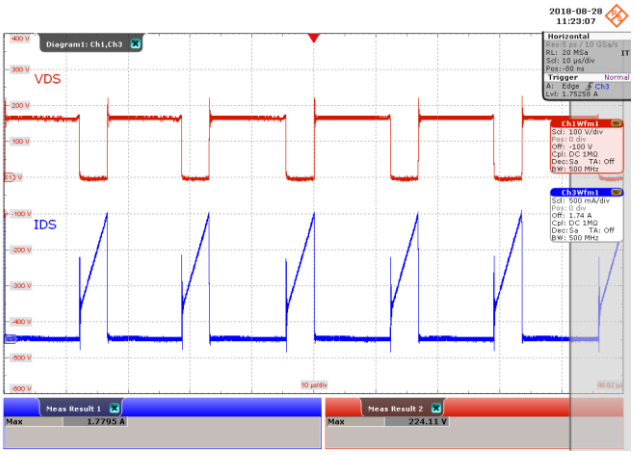

Figure 51 – Drain Voltage and Current Waveforms.
100 VAC, 5 V, 6.5 A Load, (224 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

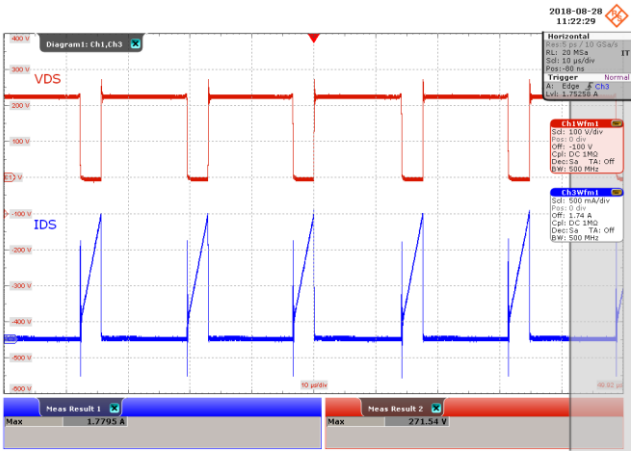

Figure 52 – Drain Voltage and Current Waveforms.
135 VAC, 5 V, 6.5 A Load, (271 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

12.2.1.2 9 V Output

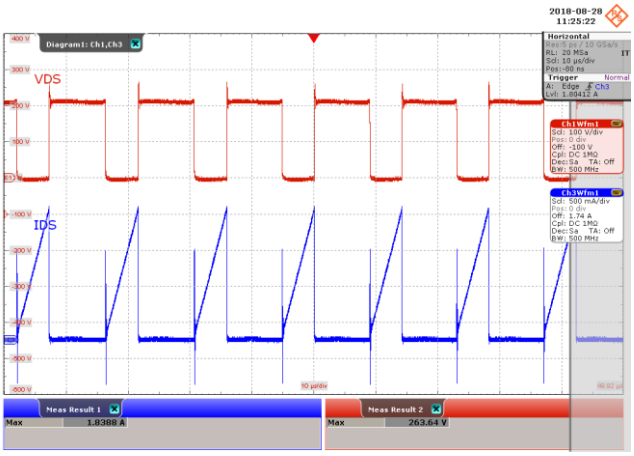

Figure 53 – Drain Voltage and Current Waveforms.
100 VAC, 9.0 V, 5.0 A Load, (264 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

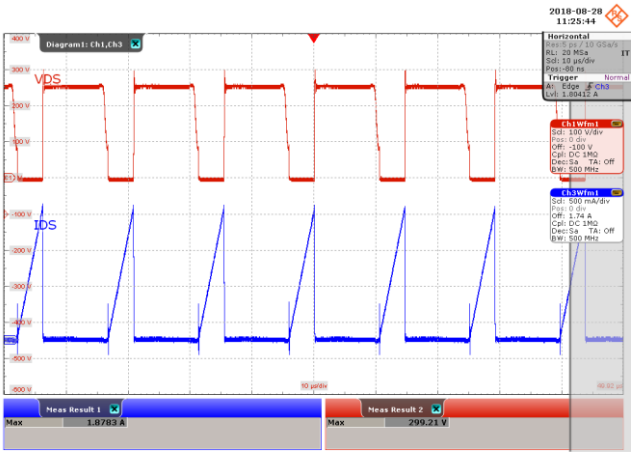

Figure 54 – Drain Voltage and Current Waveforms.
135 VAC, 9.0 V, 5.0 A Load, (299 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

12.2.1.3 15 V Output

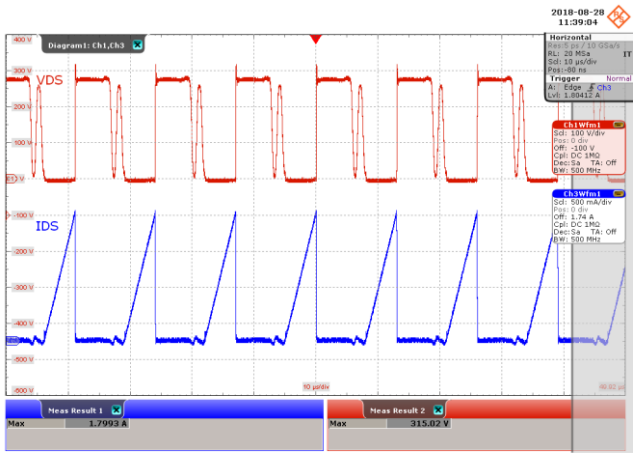

Figure 55 – Drain Voltage and Current Waveforms.
100 VAC, 15.0 V, 3.0 A Load, (315 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

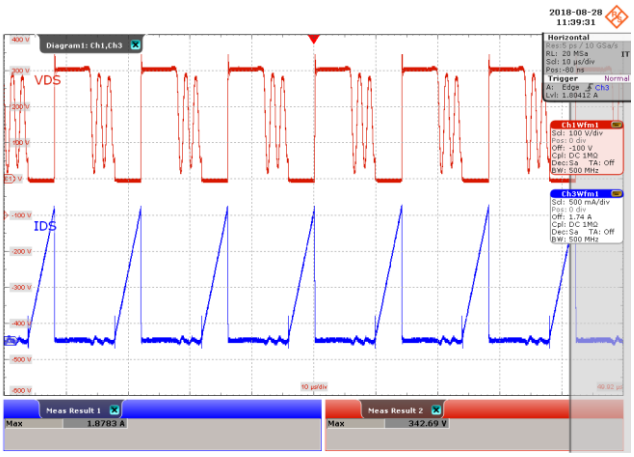

Figure 56 – Drain Voltage and Current Waveforms.
135 VAC, 15.0 V, 3.0 A Load, (343 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

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12.2.2 Drain Voltage and Current (Start-up)

12.2.2.1 5 V Output

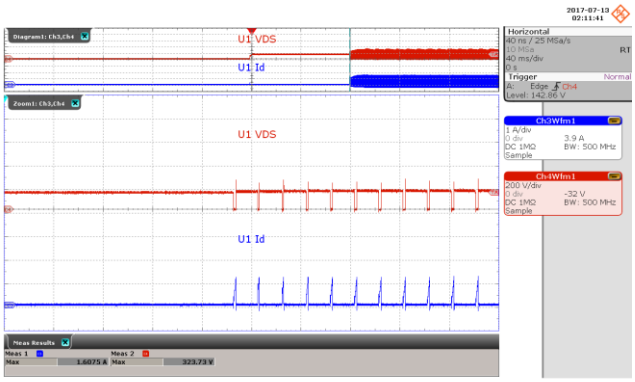

Figure 57 – Drain Voltage and Current Waveforms.
100 VAC, 5 V, 6.5 A Load, (324 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 1 A / div.

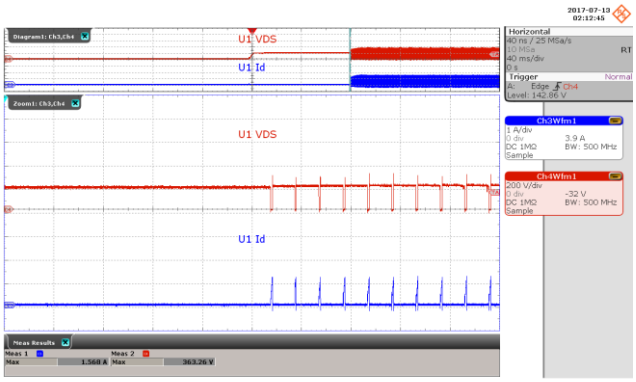

Figure 58 – Drain Voltage and Current Waveforms.
135 VAC, 5 V, 6.5 A Load, (363 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 1 A / div.

12.2.2.2 9 V Output

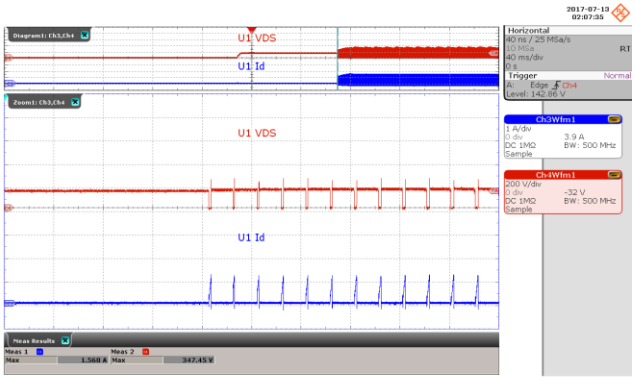

Figure 59 – Drain Voltage and Current Waveforms.
100 VAC, 9.0 V, 5.0 A Load, (347 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 1 A / div.

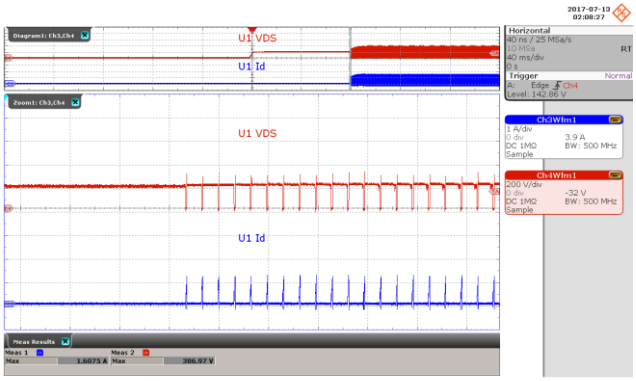

Figure 60 – Drain Voltage and Current Waveforms.
135 VAC, 9.0 V, 5.0 A Load, (387 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 1 A / div.

12.2.2.3 15 V Output

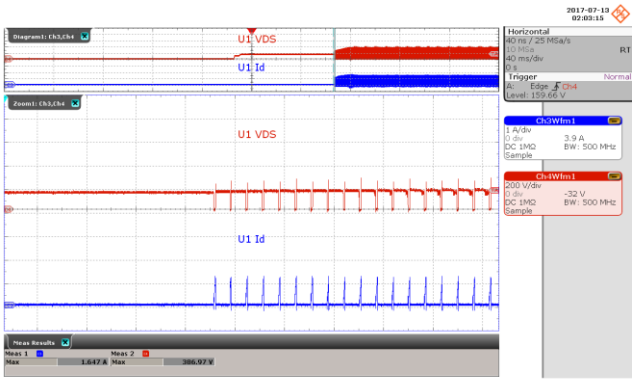

Figure 61 – Drain Voltage and Current Waveforms.
100 VAC, 15.0 V, 3.0 A Load, (387 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 1 A / div.

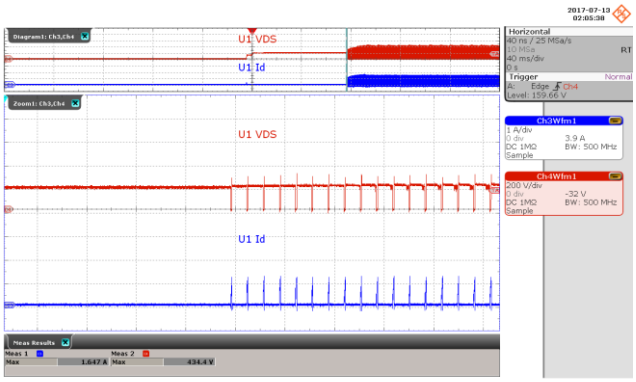

Figure 62 – Drain Voltage and Current Waveforms.
135 VAC, 15.0 V, 3.0 A Load, (434 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 1 A / div.

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12.2.3 SR MOSFET Voltage

12.2.3.1 5 V Output

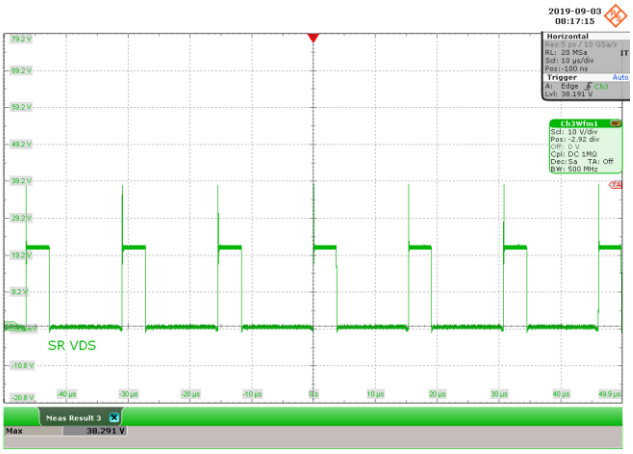

Figure 63 – SR FET Voltage Waveform.
100 VAC, 5 V, 6.5 A Load, (38.291 V_{MAX}).
V_{DRAIN}, 10 V, 10 µs / div.

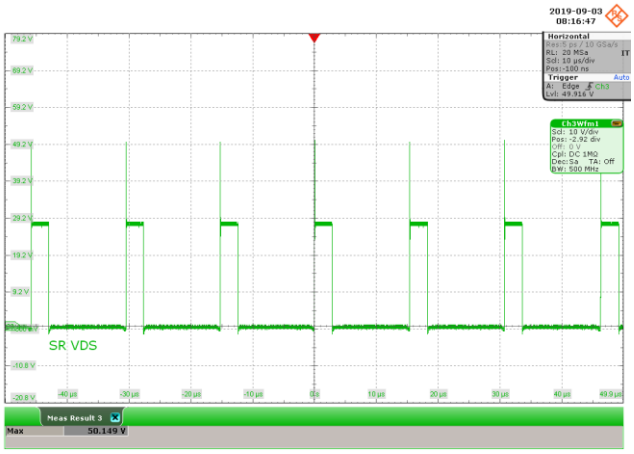

Figure 64 – SR FET Voltage Waveform.
135 VAC, 5 V, 6.5 A Load, (50.149 V_{MAX}).
V_{DRAIN}, 10 V, 10 µs / div.

12.2.3.2 9 V Output

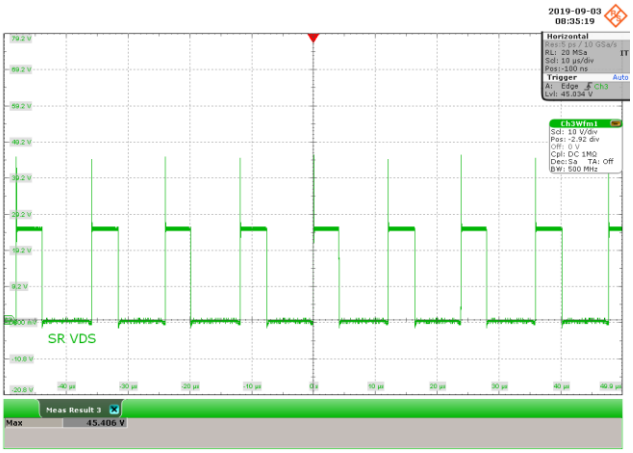

Figure 65 – SR1 FET Voltage Waveform.
100 VAC, 9 V, 5.0 A Load, (45.406 V_{MAX}).
V_{DRAIN}, 10 V, 10 µs / div.

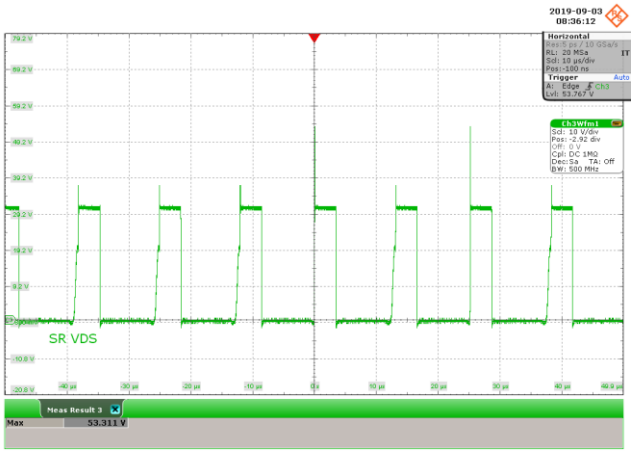

Figure 66 – SR1 FET Voltage Waveform.
135 VAC, 9 V, 5.0 A Load, (53.311 V_{MAX}).
V_{DRAIN}, 10 V, 10 µs / div.

12.2.3.3 15 V Output

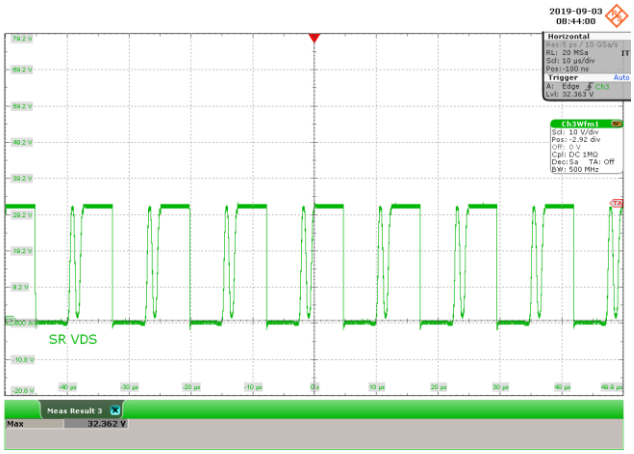

Figure 67 – SR FET Voltage Waveform.
100 VAC, 15 V, 3 A Load, (32.362 V_{MAX}).
V_{DRAIN}, 10 V, 10 µs / div.

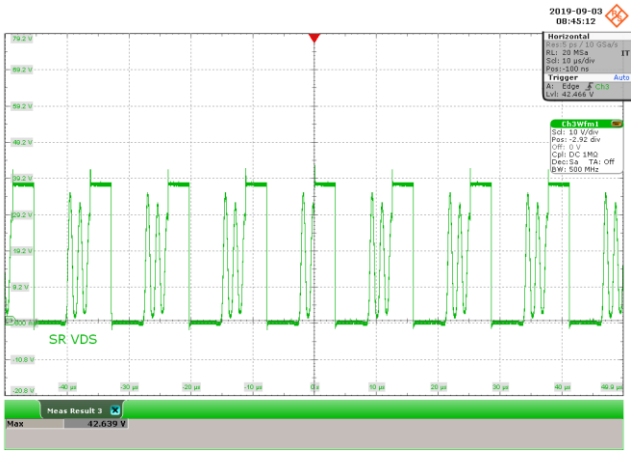

Figure 68 – SR FET Voltage Waveform.
135 VAC, 15 V, 3 A Load, (42.639 V_{MAX}).
V_{DRAIN}, 10 V, 10 µs / div.

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12.2.4 Output Voltage and Current Start-up (End of 100 mΩ Cable)

12.2.4.1 5 V Output

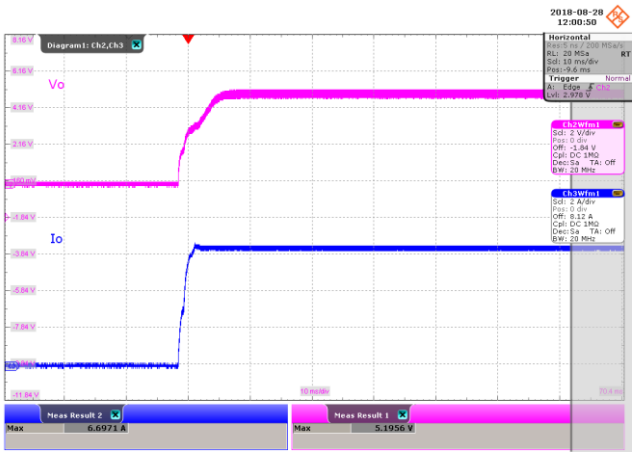

Figure 69 – Output Voltage and Current Waveforms.
100 VAC Input, 5 V, 0.77 Ω Load .
Upper: V_{OUT}, 2 V / div
Lower: I_{OUT}, 2 A, 10 ms / div.

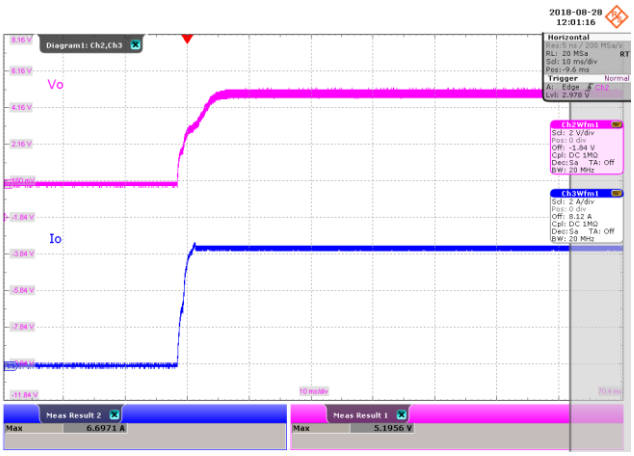

Figure 70 – Output Voltage and Current Waveforms.
135 VAC Input, 5 V, 0.77 Ω Load.
Upper: V_{OUT}, 2 V / div
Lower: I_{OUT}, 2 A, 10 ms / div..

12.2.4.2 9 V Output

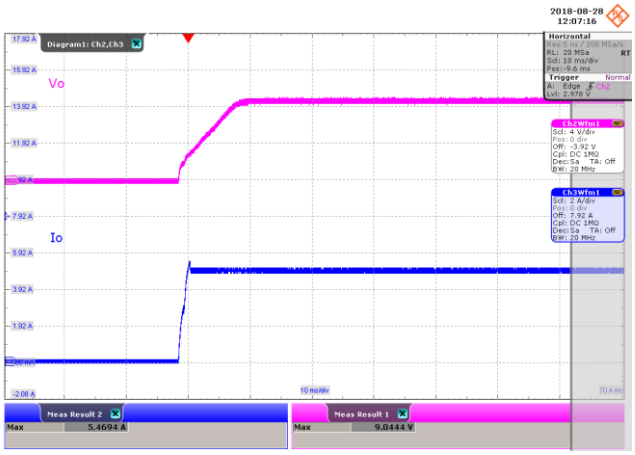

Figure 71 – Output Voltage and Current Waveforms.
100 VAC Input, 9 V, 1.8 Ω Load .
Upper: V_{OUT}, 4 V / div
Lower: I_{OUT}, 2 A, 10 ms / div.

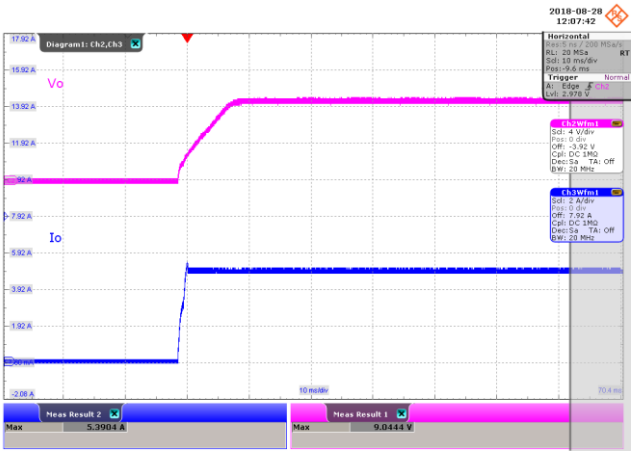

Figure 72 – Output Voltage and Current Waveforms.
135 VAC Input, 9 V, 1.8 Ω Load.
Upper: V_{OUT}, 4 V / div
Lower: I_{OUT}, 2 A, 10 ms / div.

12.2.4.3 15 V Output

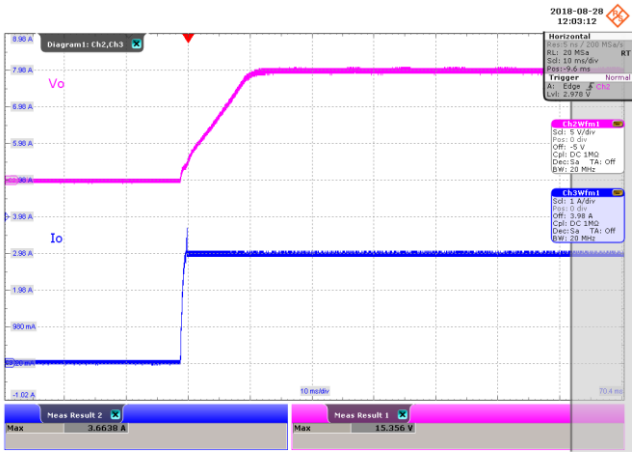

Figure 73 – Output Voltage and Current Waveforms.
100 VAC Input, 15 V, 5 Ω Load .
Upper: V_{OUT}, 5 V / div
Lower: I_{OUT}, 1 A, 10 ms / div.

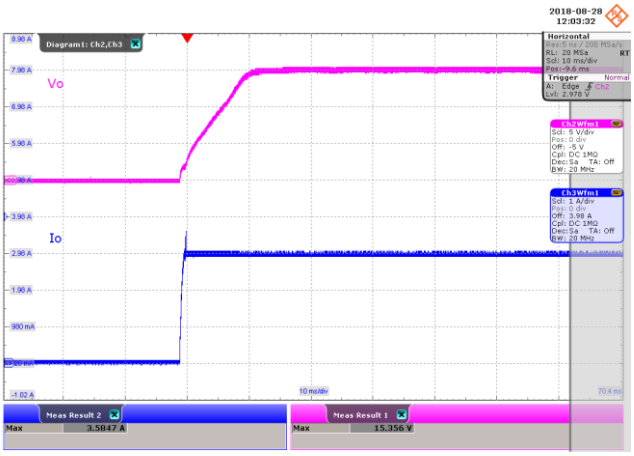

Figure 74 – Output Voltage and Current Waveforms.
135 VAC Input, 15 V, 5 Ω Load.
Upper: V_{OUT}, 5 V / div
Lower: I_{OUT}, 1 A, 10 ms / div.

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12.3 *Output Ripple Measurements*

12.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below). Ripple measurement done at the end of a 100mΩ cable.

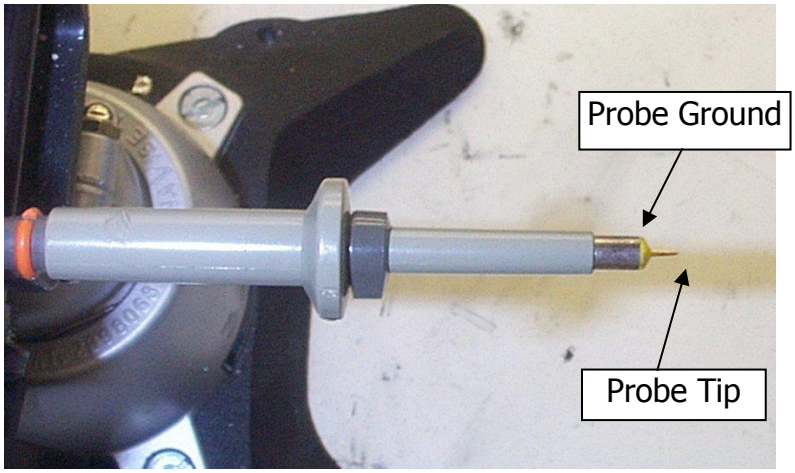

Figure 75 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

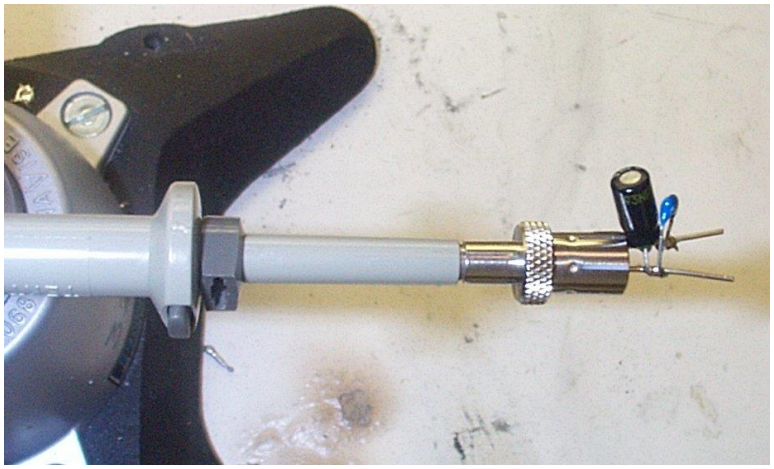

Figure 76 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

12.3.1.1 5 V Output

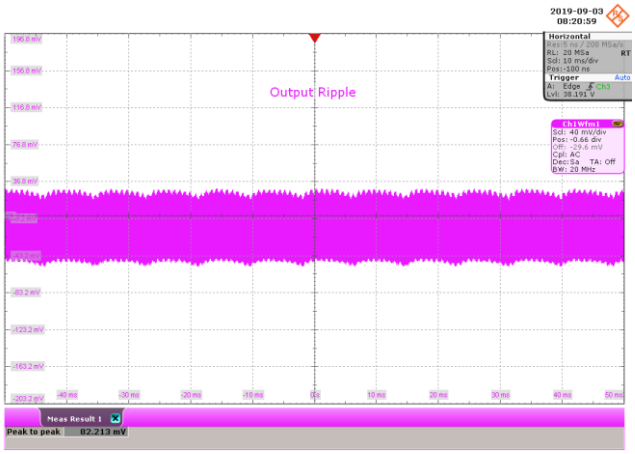

Figure 77 – Output Ripple.
100 VAC Input 5 V, 6.5 A Load.
V_{OUT}, 40 mV / div., 10 ms / div.

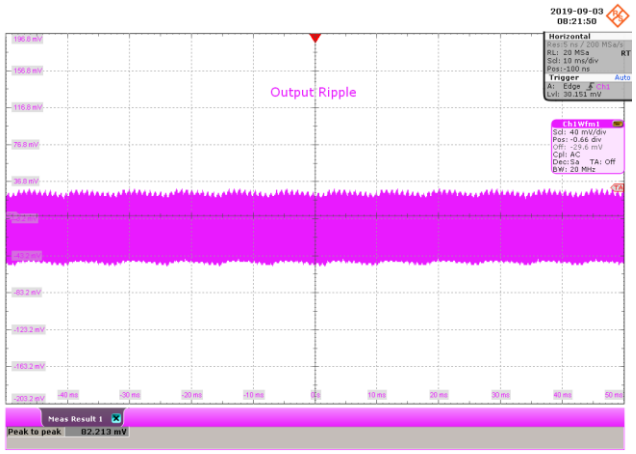

Figure 78 – Output Ripple.
135 VAC Input 5 V, 6.5 A Load.
V_{OUT}, 40 mV / div., 10 ms / div.

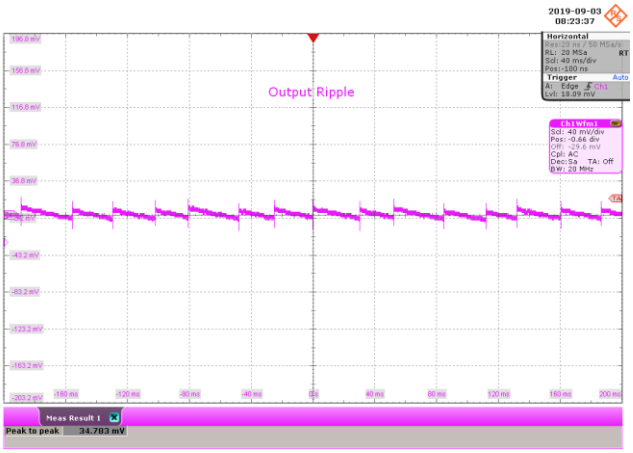

Figure 79 – Output Ripple.
100 VAC Input 5 V, 0 A Load.
V_{OUT}, 40 mV / div., 40 ms / div.

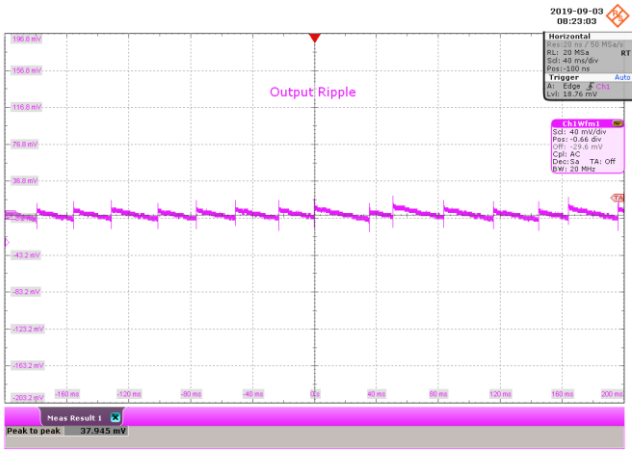

Figure 80 – Output Ripple.
135 VAC Input 5 V, 0 A Load.
V_{OUT}, 40 mV / div., 40 ms / div.

Input (VAC)	Full Load (mV)	No-Load (mV)
100	82.21	34.78
132	82.21	37.95

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12.3.1.2 9 V Output

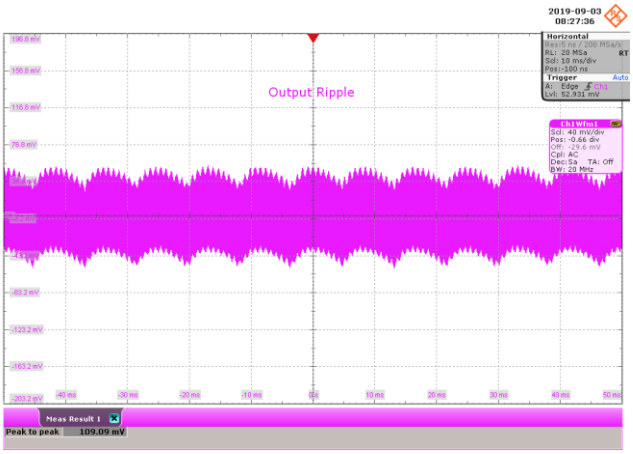

Figure 81 – Output Ripple.
100 VAC Input, 9.0 V, 5.0 A Load.
V_{OUT}, 40 mV / div., 10 ms / div.

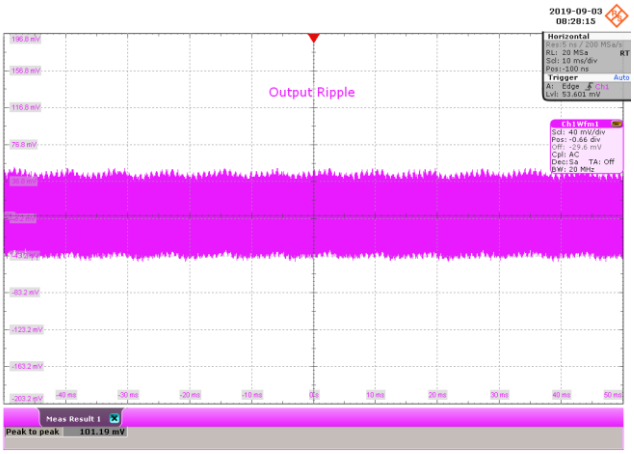

Figure 82 – Output Ripple.
135 VAC Input 9.0 V, 5.0 A Load.
V_{OUT}, 40 mV / div., 10 ms / div.

12.3.1.3 15 V Output

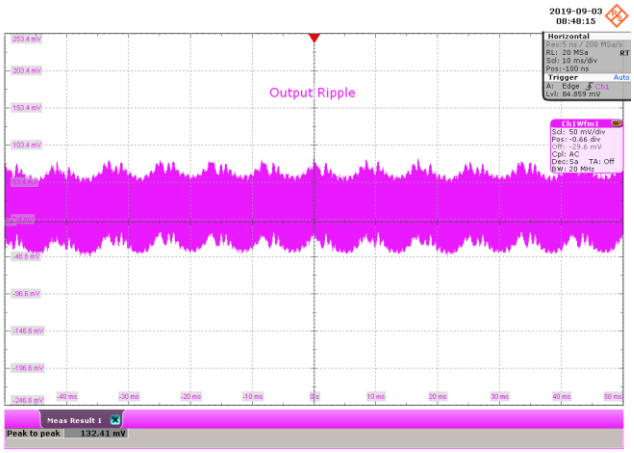

Figure 83 – Output Ripple.
100 VAC Input, 15.0 V, 3.0 A Load.
V_{OUT}, 50 mV / div., 10 ms / div.

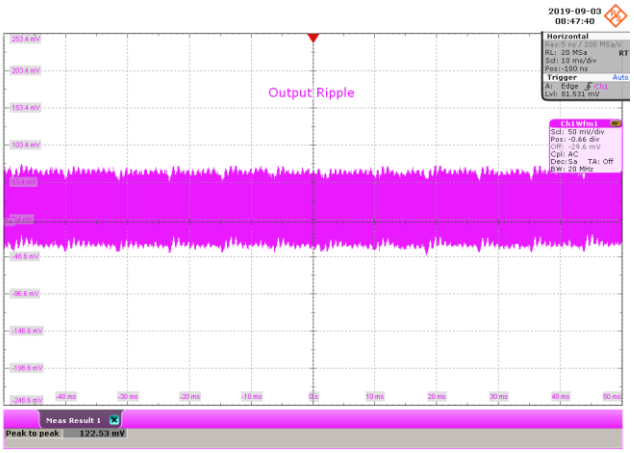

Figure 84 – Output Ripple.
135 VAC Input 15.0 V, 3.0 A Load.
V_{OUT}, 50 mV / div., 10 ms / div.

Input (VAC)	9 V (mV)	15 V (mV)
100	109.09	132.41
135	101.19	122.53

13 Conducted EMI

13.1 *Test Set-up*

13.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture, model A662003.
5. Resistor load with input voltage set at 115 VAC.

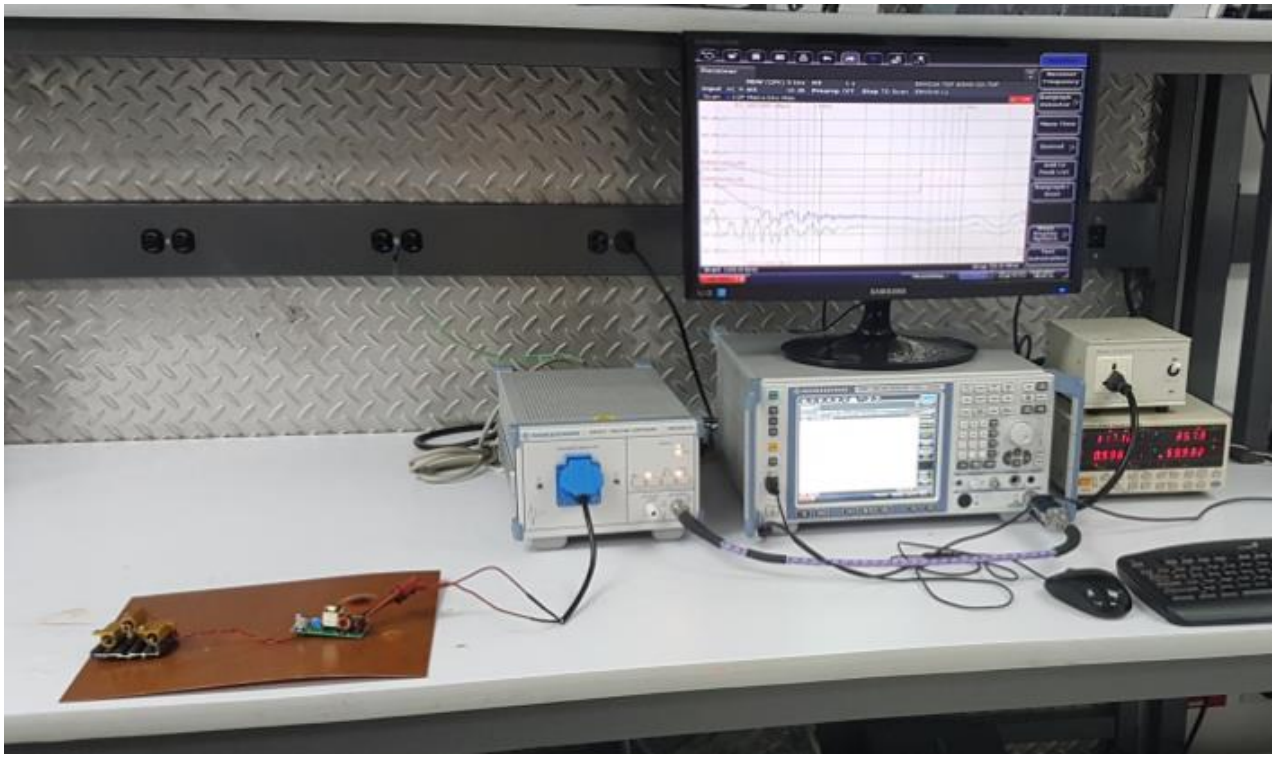

Figure 85 – Conducted EMI Test Set-up.

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13.2 *EMI Test Result*

13.2.1 Floating Output

13.2.1.1 Output 5 V / 6.5 A

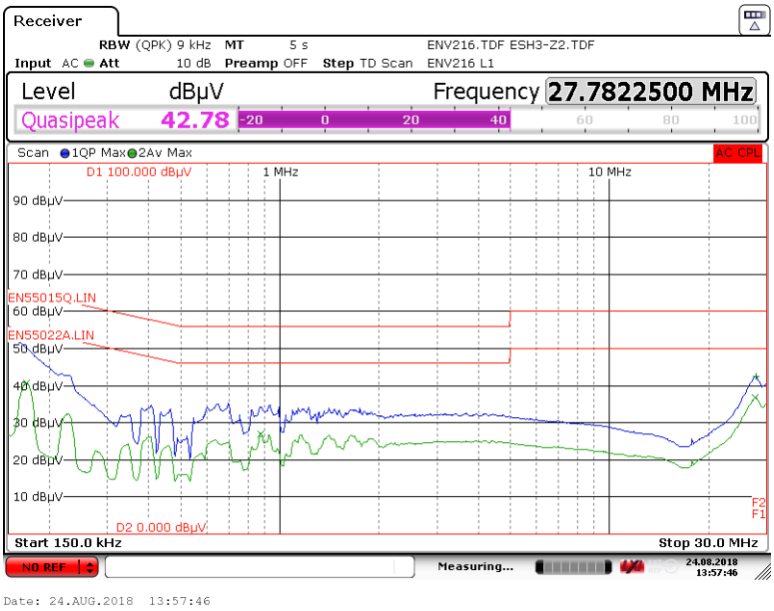

Figure 86 – Conducted EMI, 5 V / 6.5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

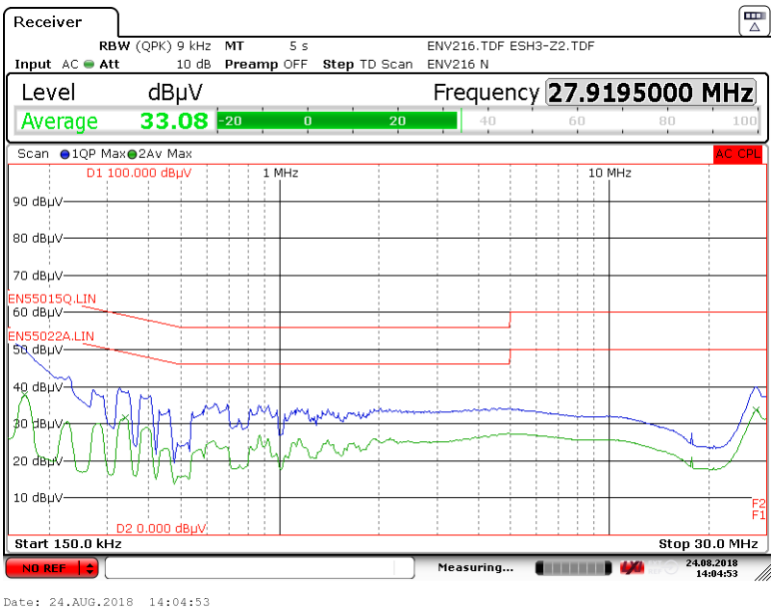

Figure 87 – Conducted EMI, 5 V / 6.5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

13.2.1.2 Output 9 V / 5 A

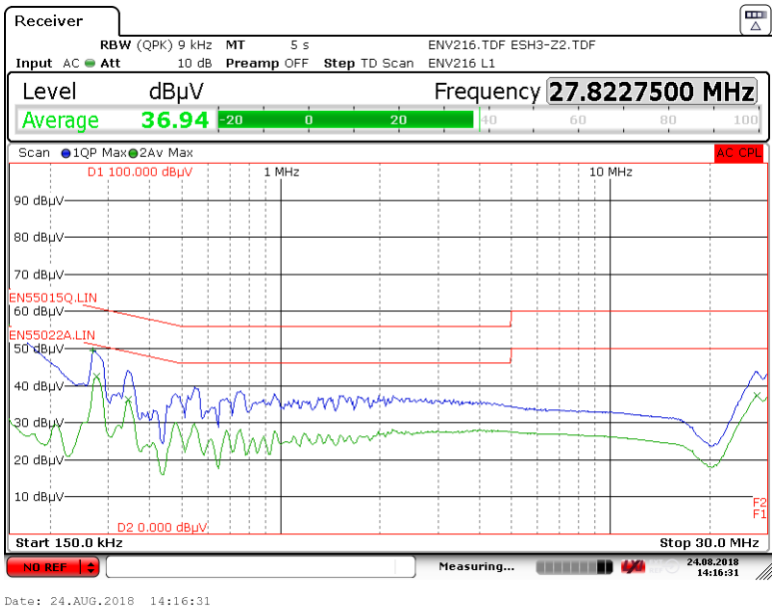

Figure 88 – Conducted EMI, 9 V / 5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

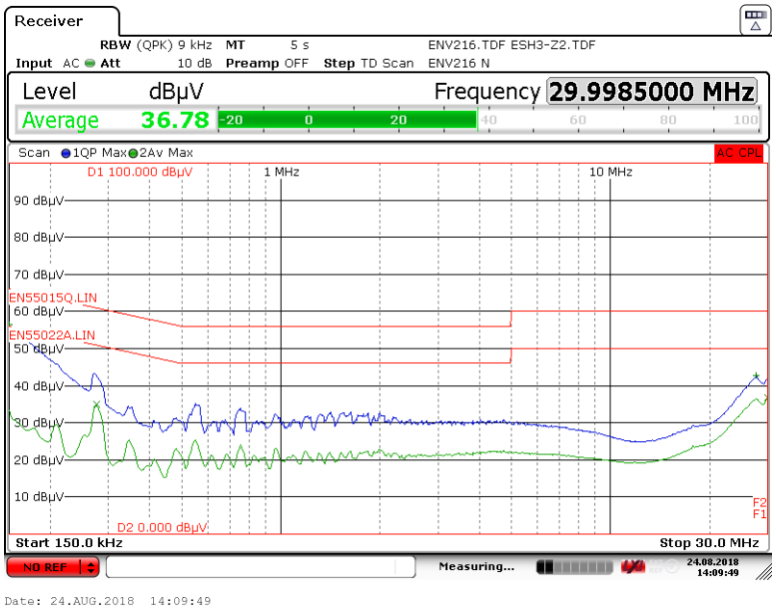

Figure 89 – Conducted EMI, 9 V / 5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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13.2.1.3 Output 15 V / 3 A

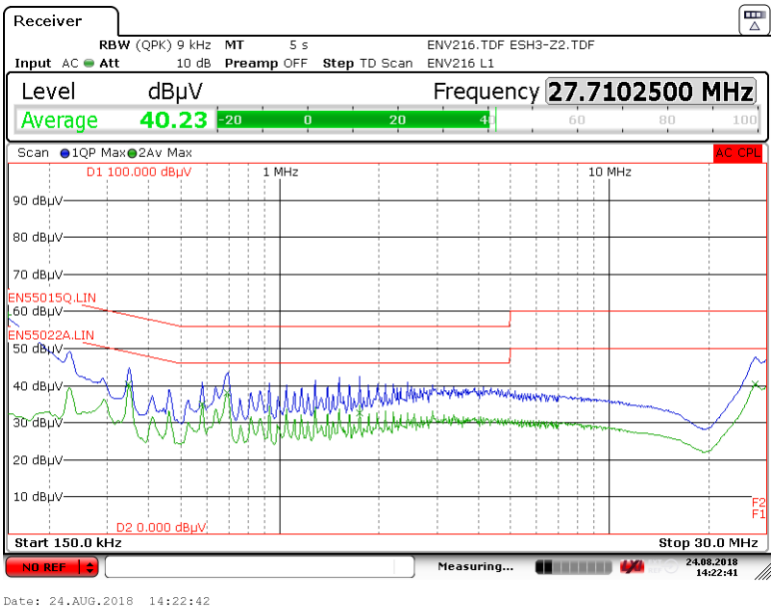

Figure 90 – Conducted EMI, 15 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

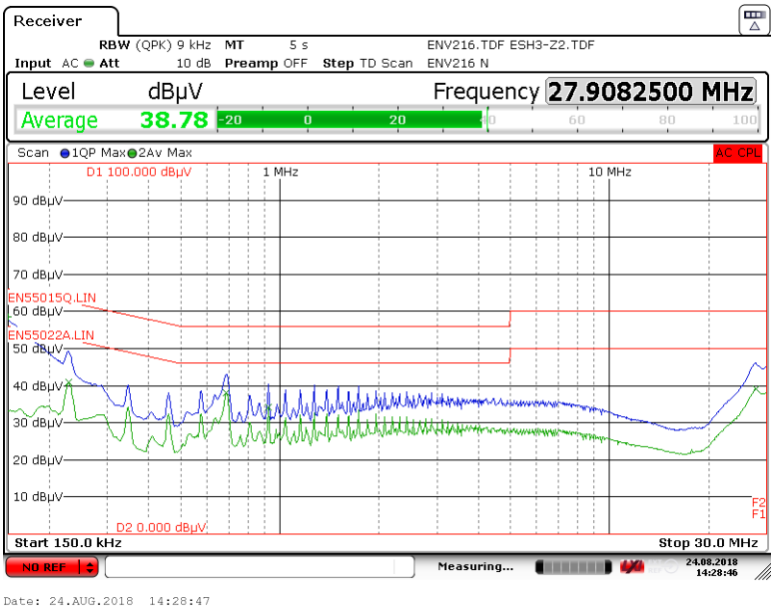

Figure 91 – Conducted EMI, 15 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

13.2.2 Artificial Hand

13.2.2.1 Output 5 V / 6.5 A

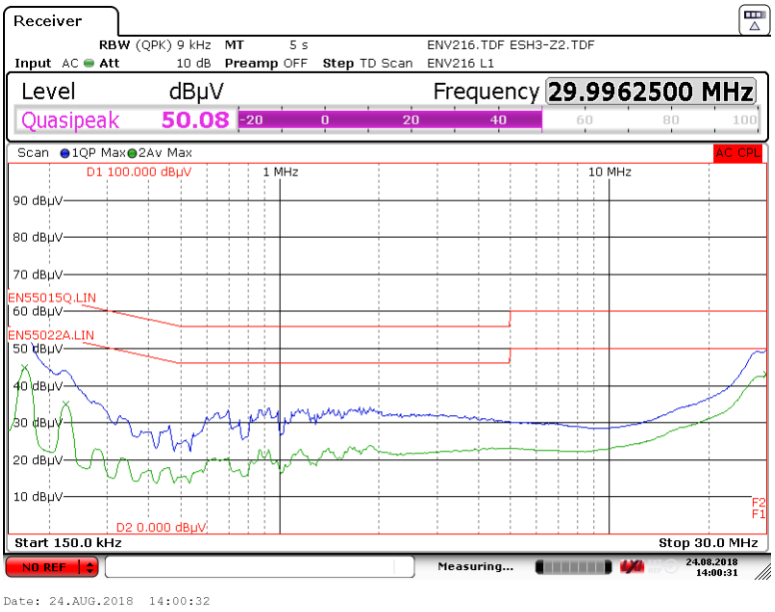

Figure 92 – Conducted EMI, 5 V / 6.5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

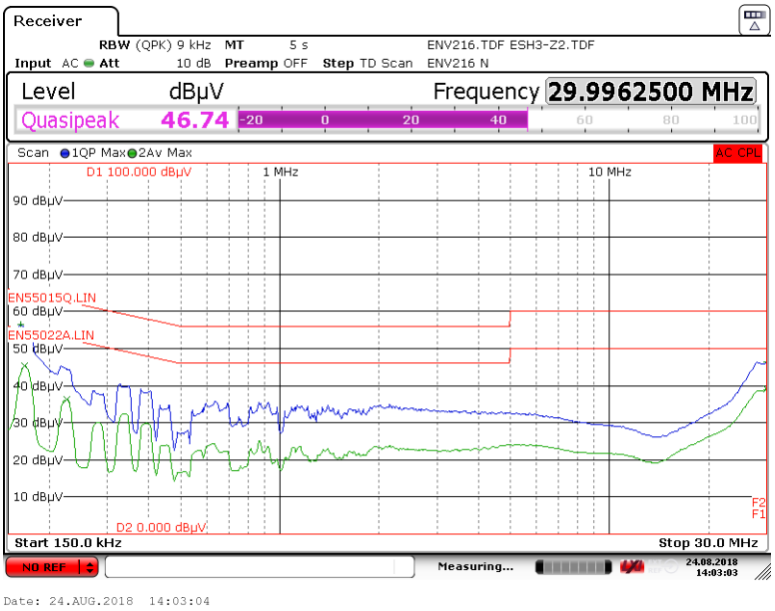

Figure 93 – Conducted EMI, 5 V / 6.5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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13.2.2.2 Output 9 V / 5 A

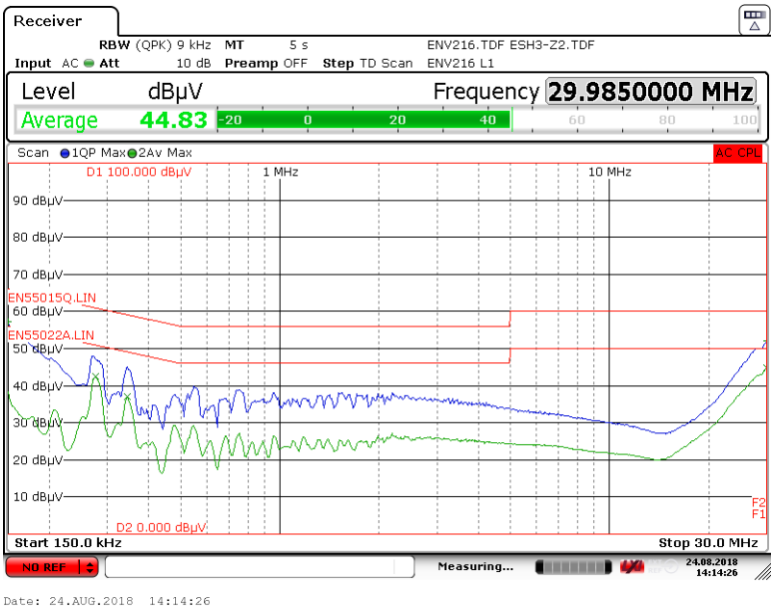

Figure 94 – Conducted EMI, 9 V / 5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

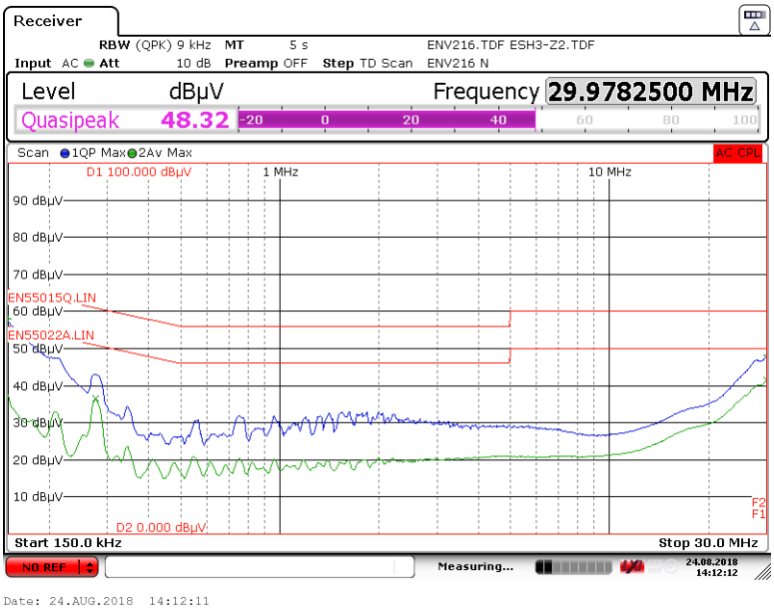

Figure 95 – Conducted EMI, 9 V / 5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

13.2.2.3 Output 15 V / 3 A

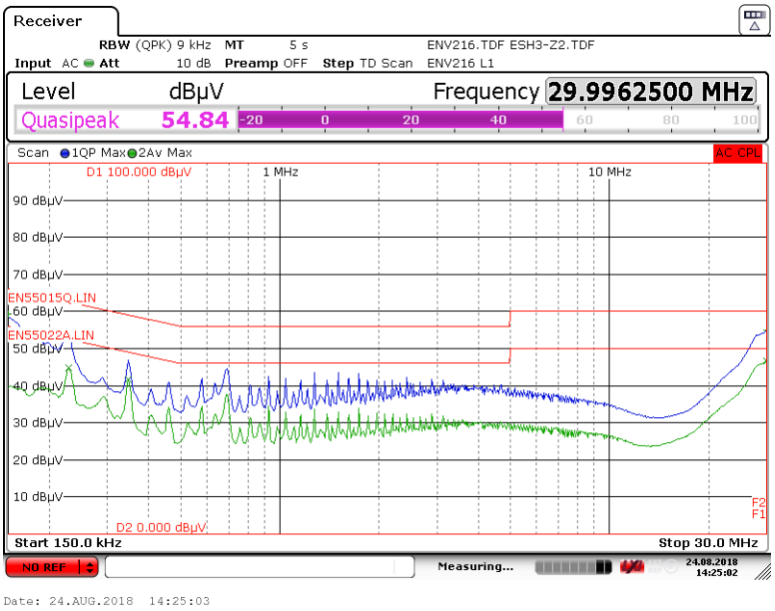

Figure 96 – Conducted EMI, 15 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

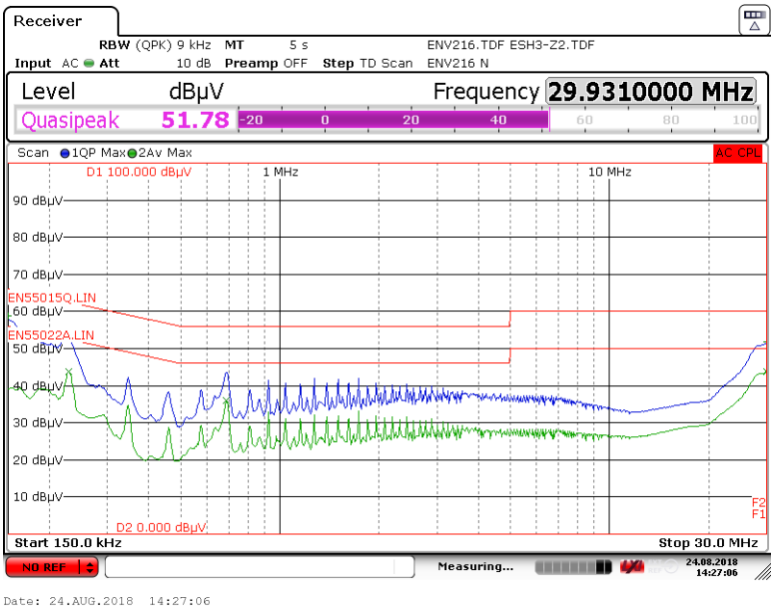

Figure 97 – Conducted EMI, 15 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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14 Line Surge

The unit was subjected to ±2000 V, common mode surge and ±1000 V differential surge using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	115	L to N	0	Pass
-1000	115	L to N	0	Pass
+1000	115	L to N	90	Pass
-1000	115	L to N	90	Pass
+2000	115	L to PE	0	Pass
-2000	115	L to PE	0	Pass
+2000	115	L to PE	90	Pass
-2000	115	L to PE	90	Pass

Note: Output ground of output connected to PE.

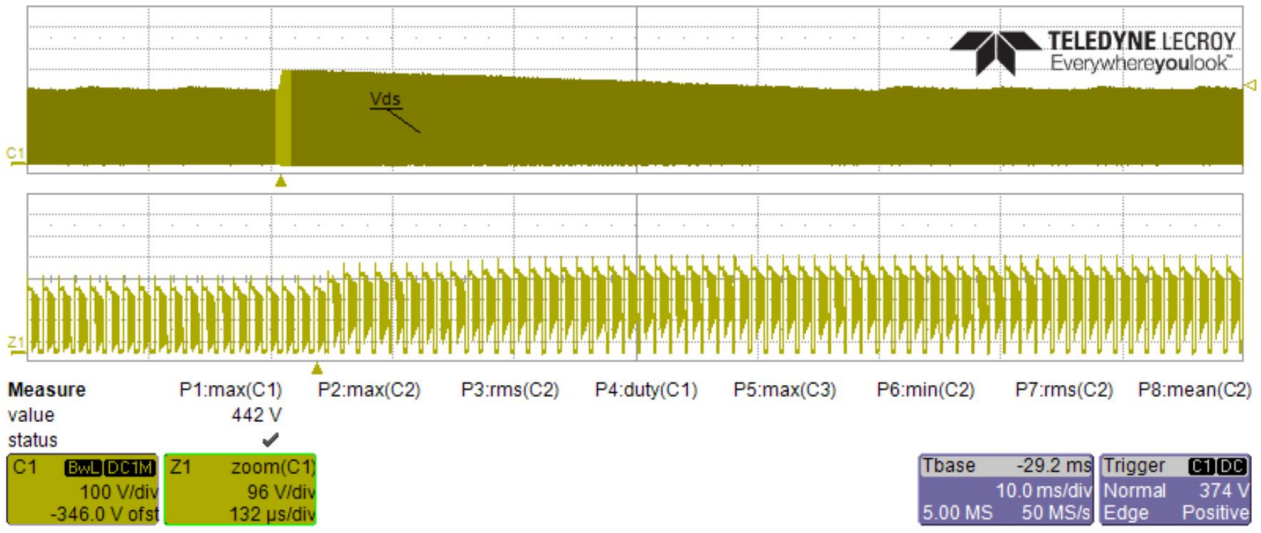

Figure 98 – U1 Drain to Source Voltage, 15 V / 3 A Load 115 VAC, 60 Hz, and Line Input Surge Test.

15 ESD Test

Passed ±8 kV contact test.

Contact Voltage (kV)	Applied to	Number of Strikes	Test Result
8	5 V	10	PASS
-8	5 V	10	PASS
8	9 V	10	PASS
-8	9 V	10	PASS
8	15 V	10	PASS
-8	15 V	10	PASS

Passed ±15 kV air test.

Differential Voltage (kV)	Applied to	Number of Strikes	Test Result
15	5 V	10	PASS
-15	5 V	10	PASS
15	9 V	10	PASS
-15	9 V	10	PASS
15	15 V	10	PASS
-15	15 V	10	PASS

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16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
11-Nov-19	IB / RPA	1.0	Initial Release	Apps & Mktg

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WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

GERMANY (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

GERMANY (Gate Driver Sales)
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@
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INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

JAPAN
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com