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U\_B12  
B12.SchDoc

U\_B13  
B13.SchDoc

U\_B14  
B14.SchDoc

U\_B15  
B15.SchDoc

U\_B16  
B16.SchDoc

U\_B34  
B34.SchDoc

U\_FPGA-MGT  
FPGA-MGT.SchDoc

U\_FPGA-CFG  
FPGA-CFG.SchDoc

U\_FPGA-MISC  
FPGA-MISC.SchDoc

U\_FPGA-PWR  
FPGA-PWR.SchDoc

U\_PWR1  
PWR1.SchDoc

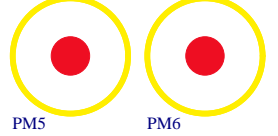
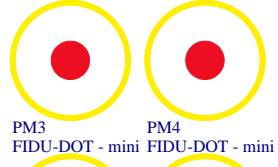
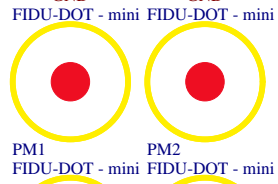
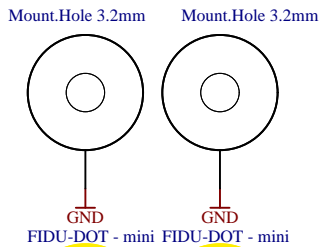
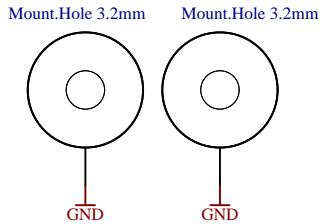
U\_PWR2  
PWR2.SchDoc

U\_Clock  
Clock.SchDoc

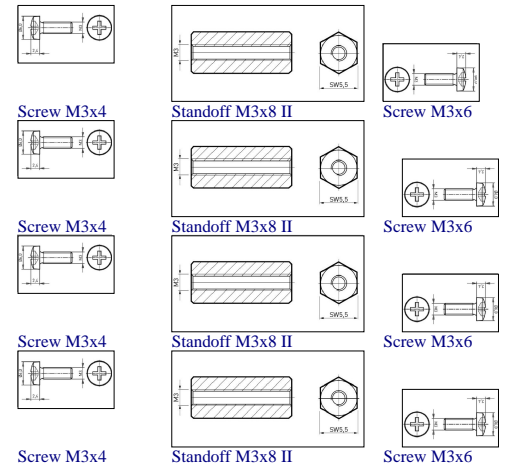
U\_B2B-Connectors  
B2B-Connectors.SchDoc

U\_B33  
B33.SchDoc

Serial  
Serialnumber 6,3 x 6.3mm



Top of Board



Assembly variant	D21-1-A
Created by	VT
Modified by	VT
Modified at	2017-01-23
SVN Revision	12616



Title: TE0741		
A4	Number: TE0741 D21-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page1 of 17
Filename: TE0741.SchDoc		

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2

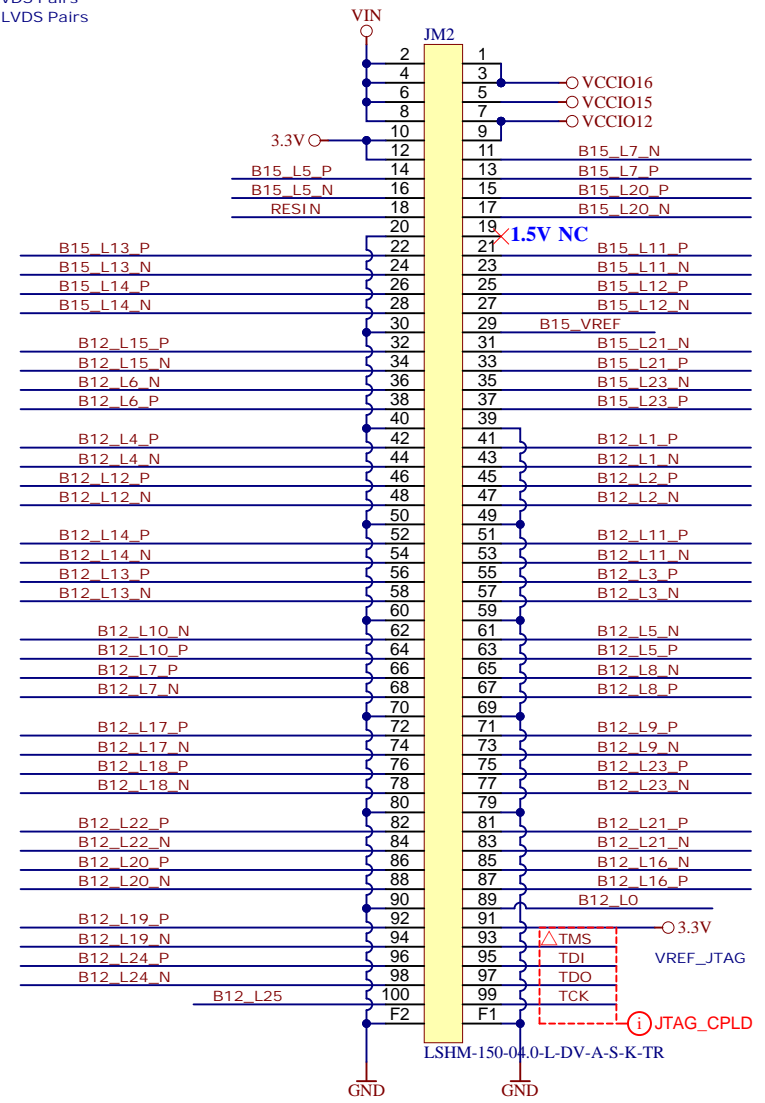
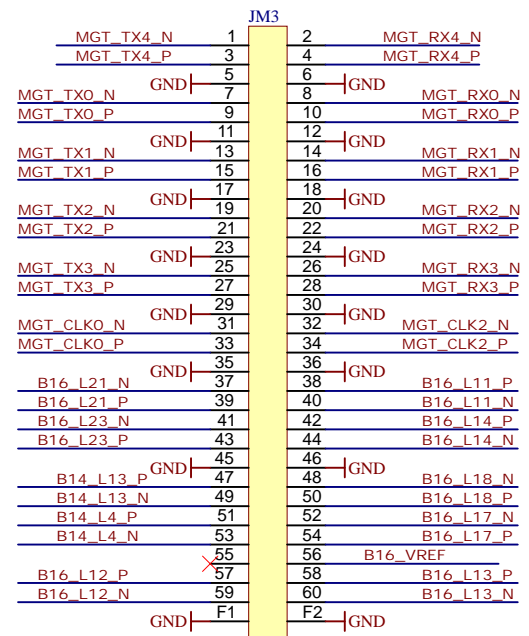
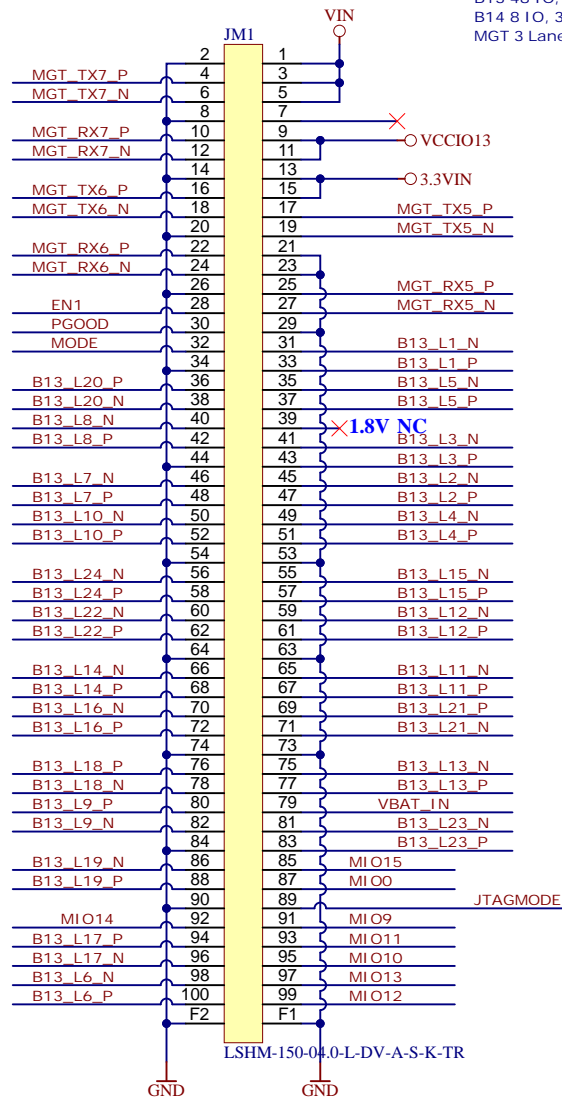
3

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B13 48 IO, 24 LVDS Pairs  
 B14 8 IO, 3.3V  
 MGT 3 Lanes

B16 16 IO, 8 LVDS Pairs  
 MGT 4 + 1 Lanes  
 B14 4 IO, 3.3V

B15 18 IO, 9 LVDS Pairs  
 B12 48 IO, 24 LVDS Pairs  
 B12 2 IO



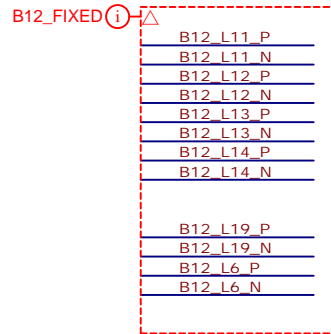
TE0720 Compatibility

MIO0 8 pins => 8 IO B14  
 USB D+,D-, vbusen,otg\_id => 4 IO B14  
 SGMII => MGT  
 MIO1(SDCARD) => MGT  
 ETH MDI => MGT  
 B34 => B16, MGT  
 B35 => B13  
 B13 => B12  
 B33 => B15

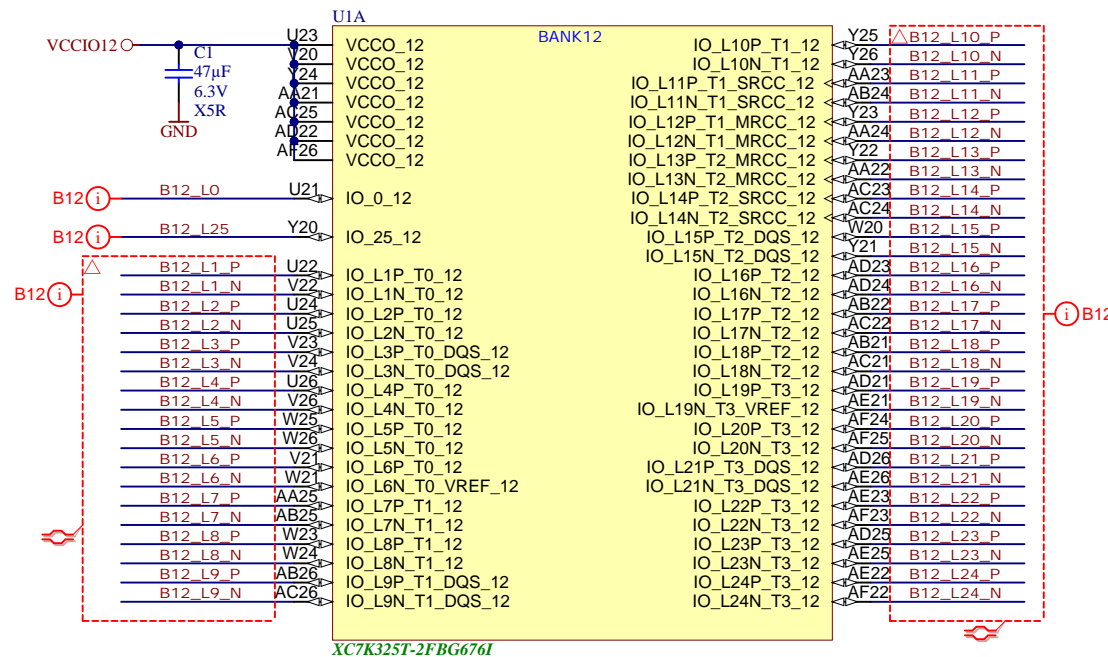
Clock Capable I/O  
 All pins named  
 Bxx\_11\_X  
 Bxx\_12\_X  
 Bxx\_13\_X  
 Bxx\_14\_X  
 Are Clock Capable I/O's



Title: TE0741		
A4	Number: TE0741 D2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page2 of 17
Filename: B2B-Connectors.SchDoc		

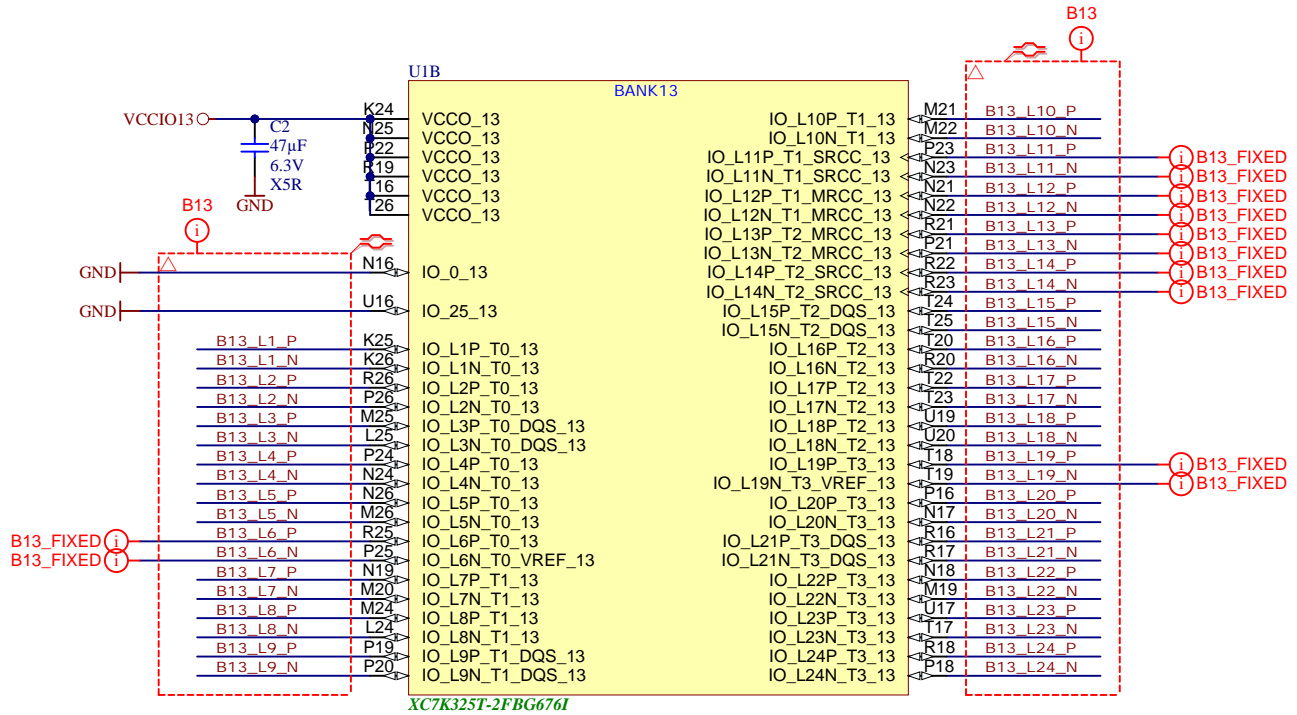


**K70T version does not have this bank!**



XC7K325T-2FBG676I

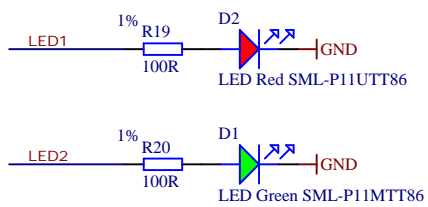
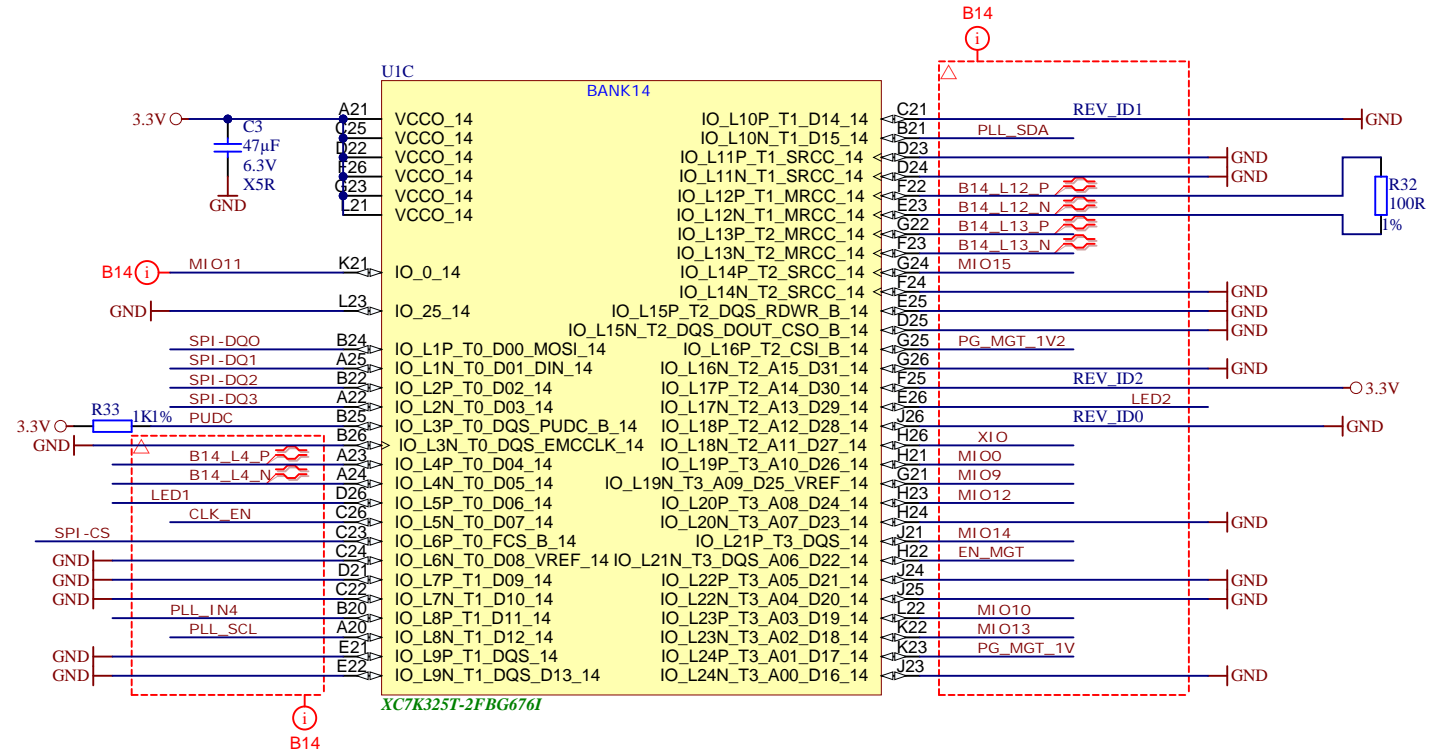
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	A4	Number: <b>TE0741 D2I-1-A</b>	Rev. <b>04</b>
	Date: <b>2016-10-25</b>	Copyright: <b>2013 Trenz Electronic GmbH</b>	Page <b>3</b> of <b>17</b>
	Filename: <b>B12.SchDoc</b>		



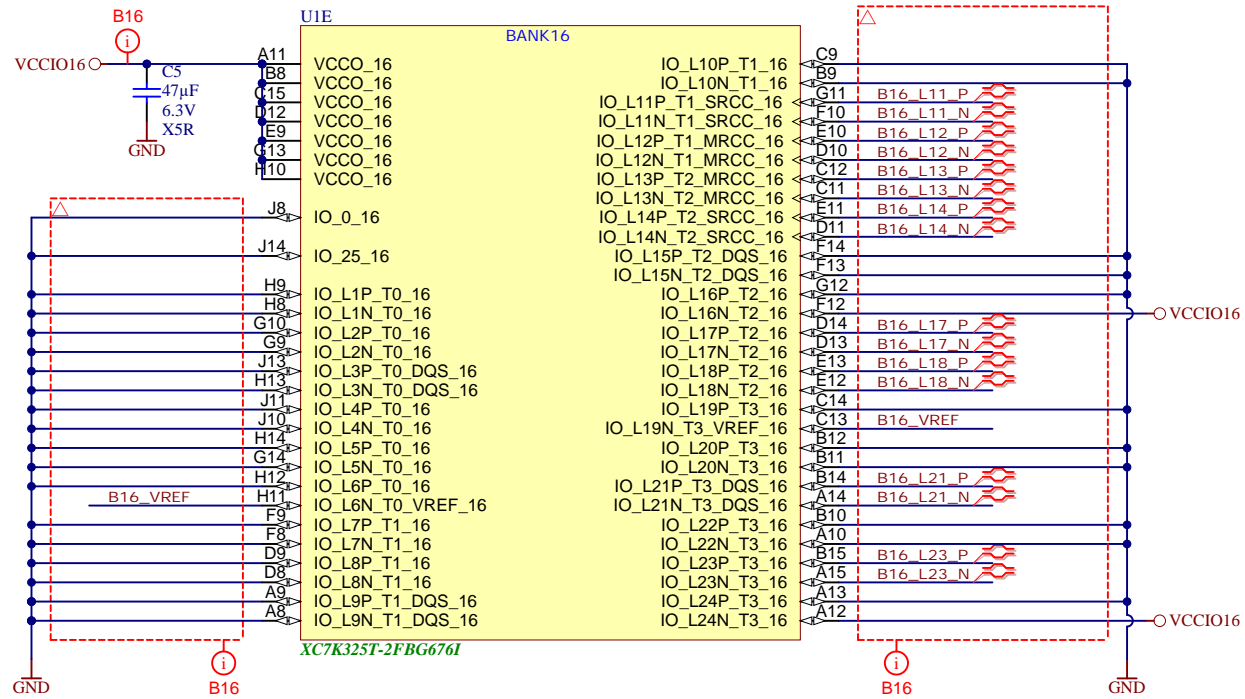
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	A4	Number: <b>TE0741 D2I-1-A</b>	Rev. <b>04</b>
	Date: <b>2016-10-25</b>	Copyright: <b>2013 Trenz Electronic GmbH</b>	Page <b>4</b> of <b>17</b>
	Filename: <b>B13.SchDoc</b>		

Revision PCB Board:

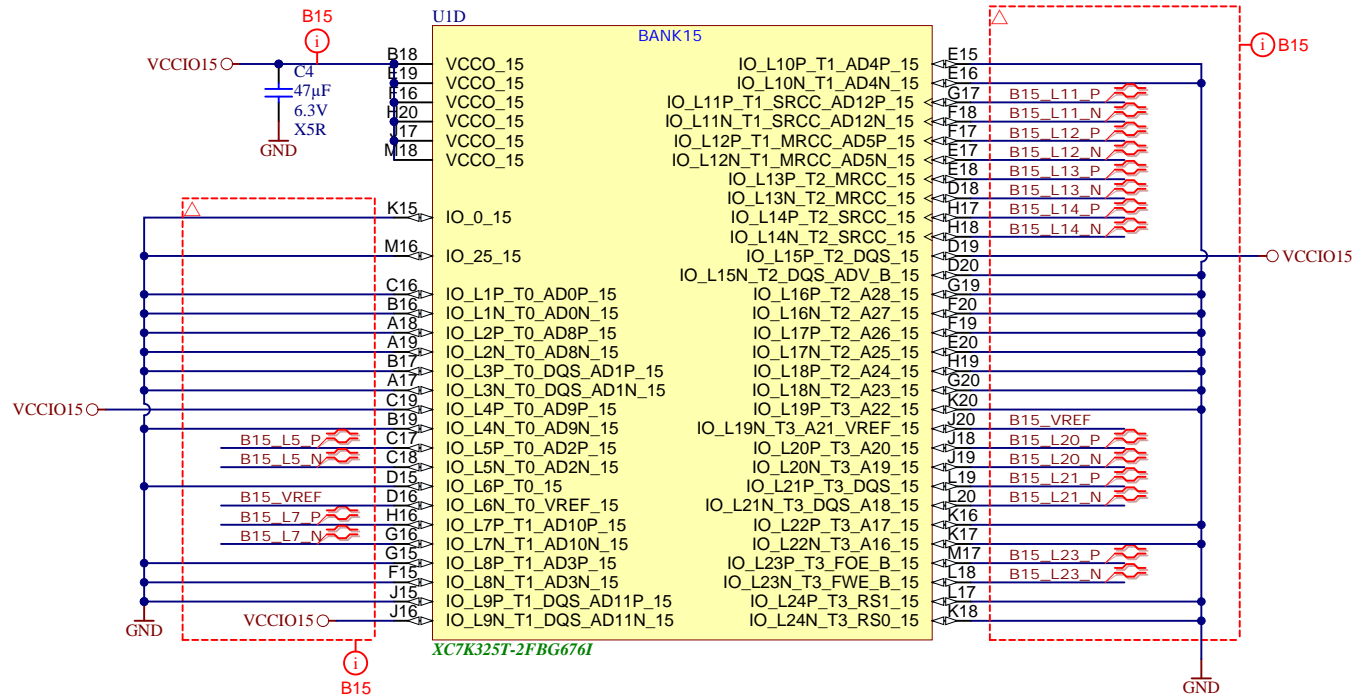
	"0"	"1"	"2"	"3"	"4"
REV_ID0	0	1	0	1	0
REV_ID1	0	0	1	1	0
REV_ID2	0	0	0	0	1




Title: TE0741		
A4	Number: TE0741 D2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 5 of 17
Filename: B14.SchDoc		



Title: TE0741		
A4	Number: TE0741 D2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 6 of 17
Filename: B16.SchDoc		



		Title: TE0741	
		A4	Number: TE0741 D2I-1-A
Date: 2016-10-25		Copyright: 2013 Trenz Electronic GmbH	
Page 7 of 17		Page 7 of 17	
Filename: B15.SchDoc			

1

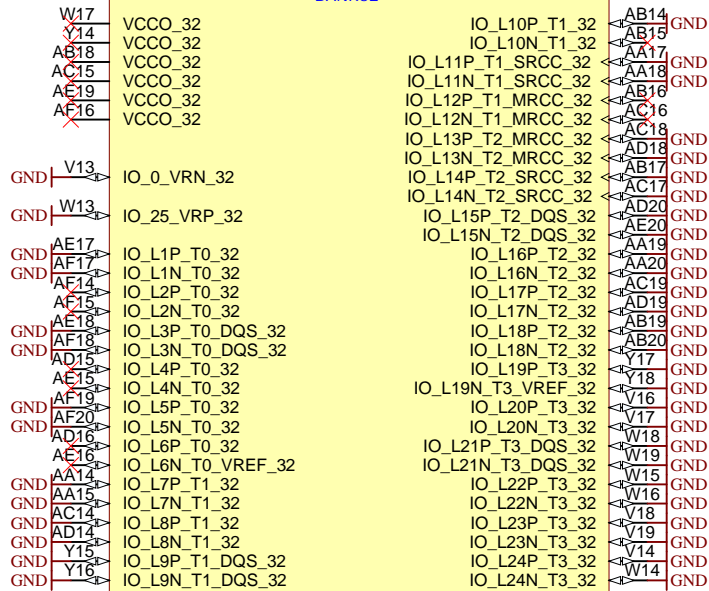
2

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UIF

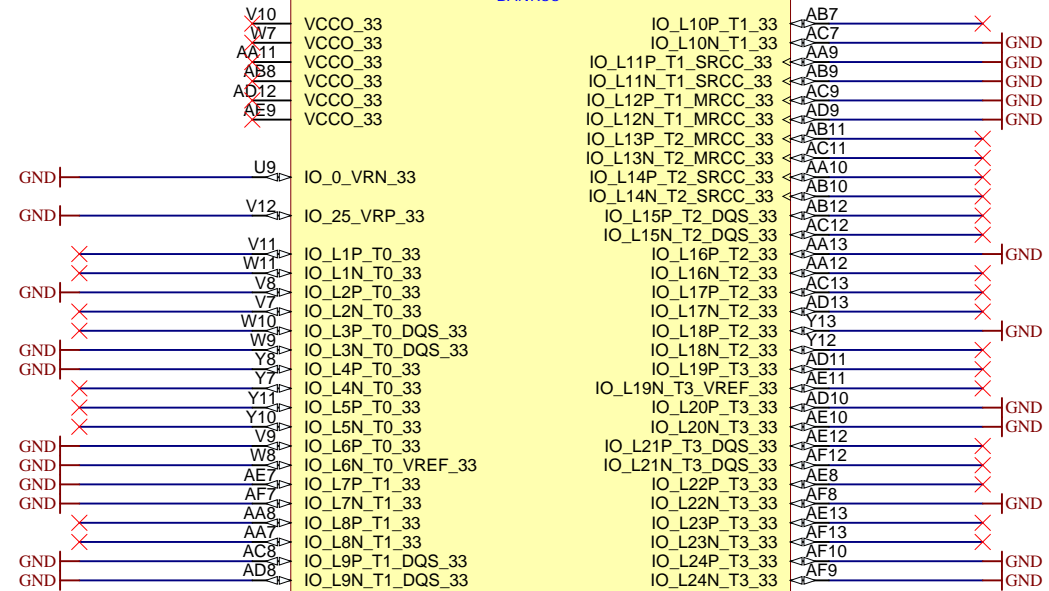
BANK32



XC7K325T-2FBG676I

UIG

BANK33



XC7K325T-2FBG676I



Title: TE0741		
A4	Number: TE0741 D2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page8 of 17
Filename: B33.SchDoc		

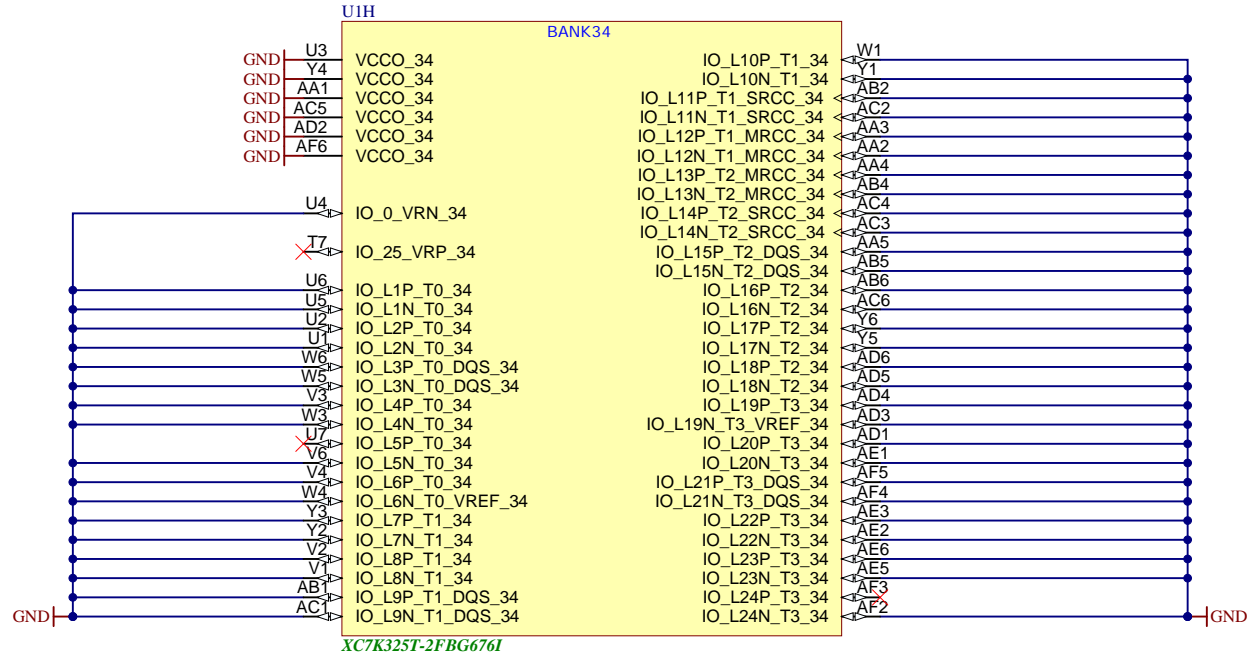

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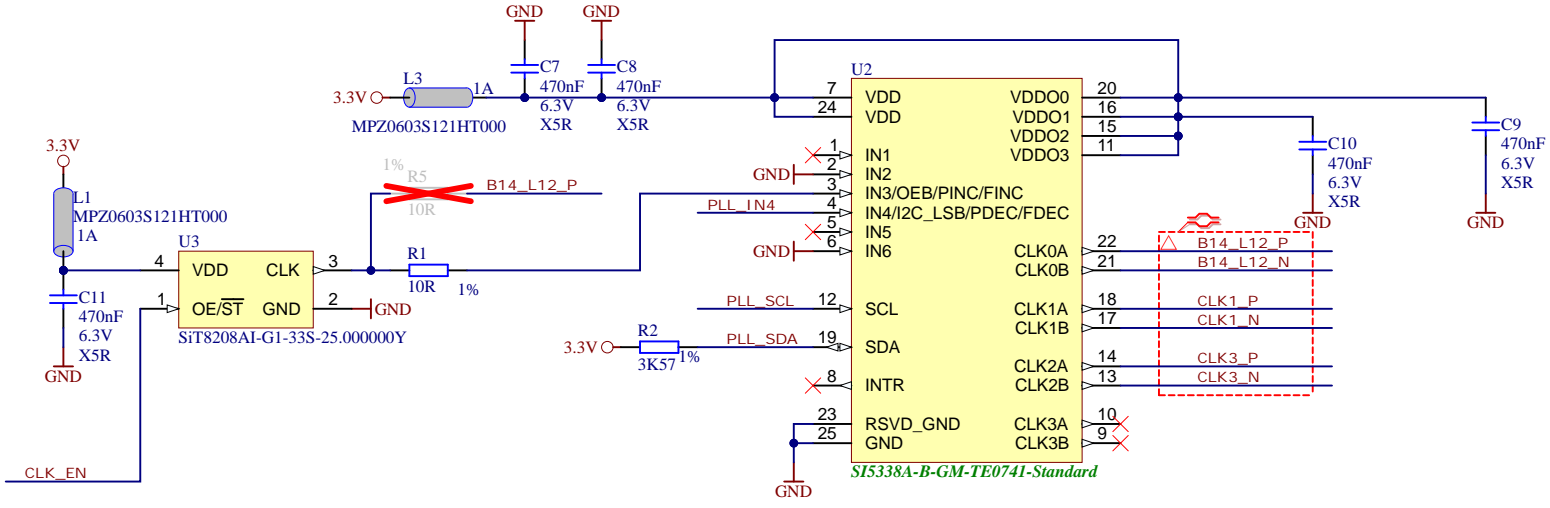
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4

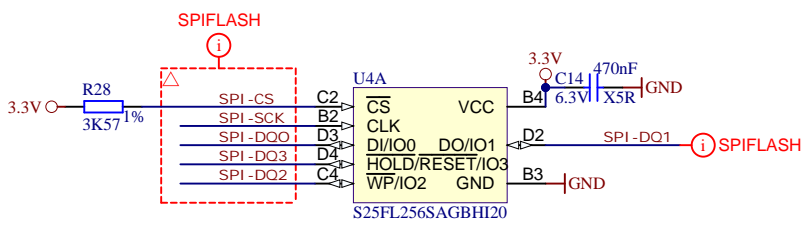
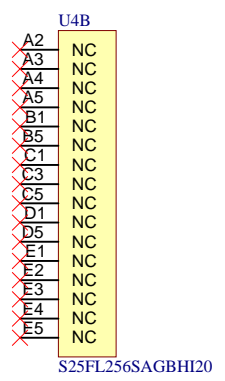
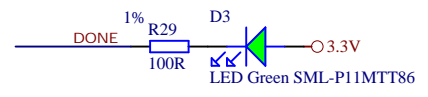
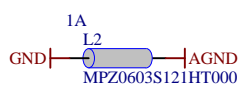
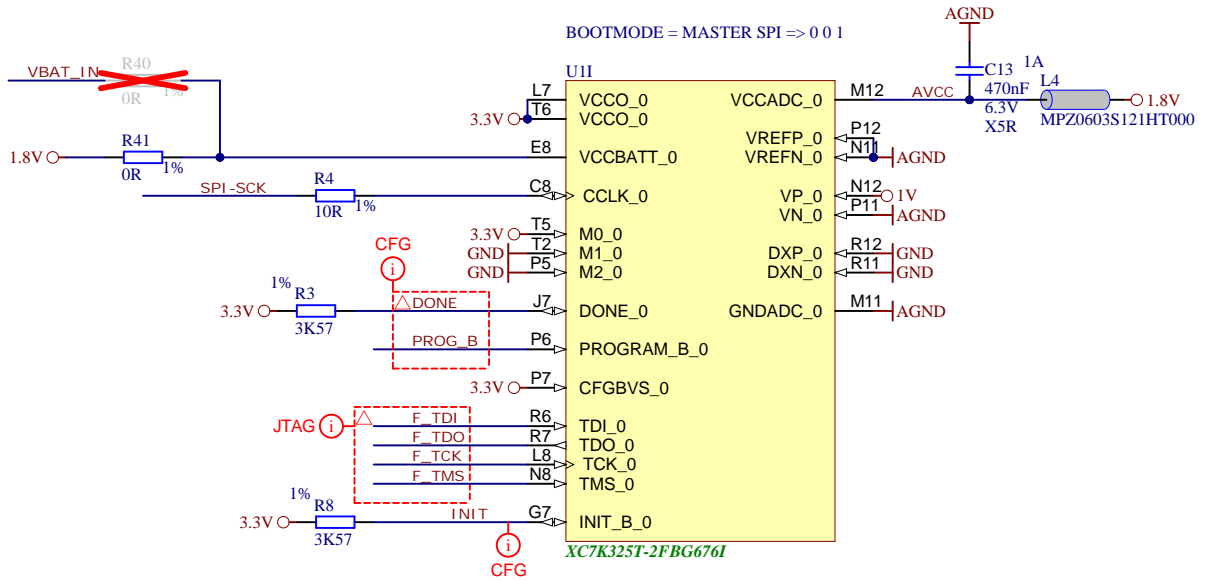


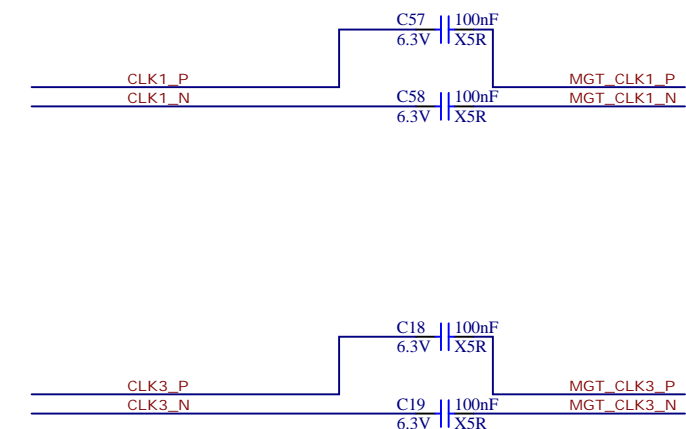
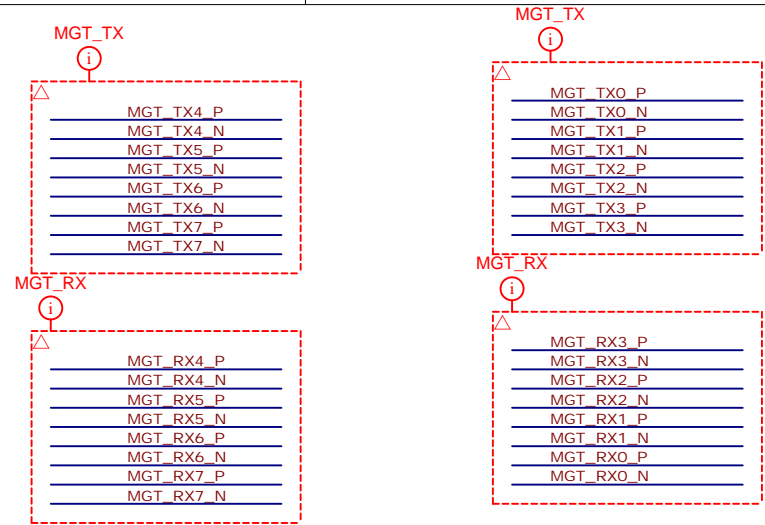
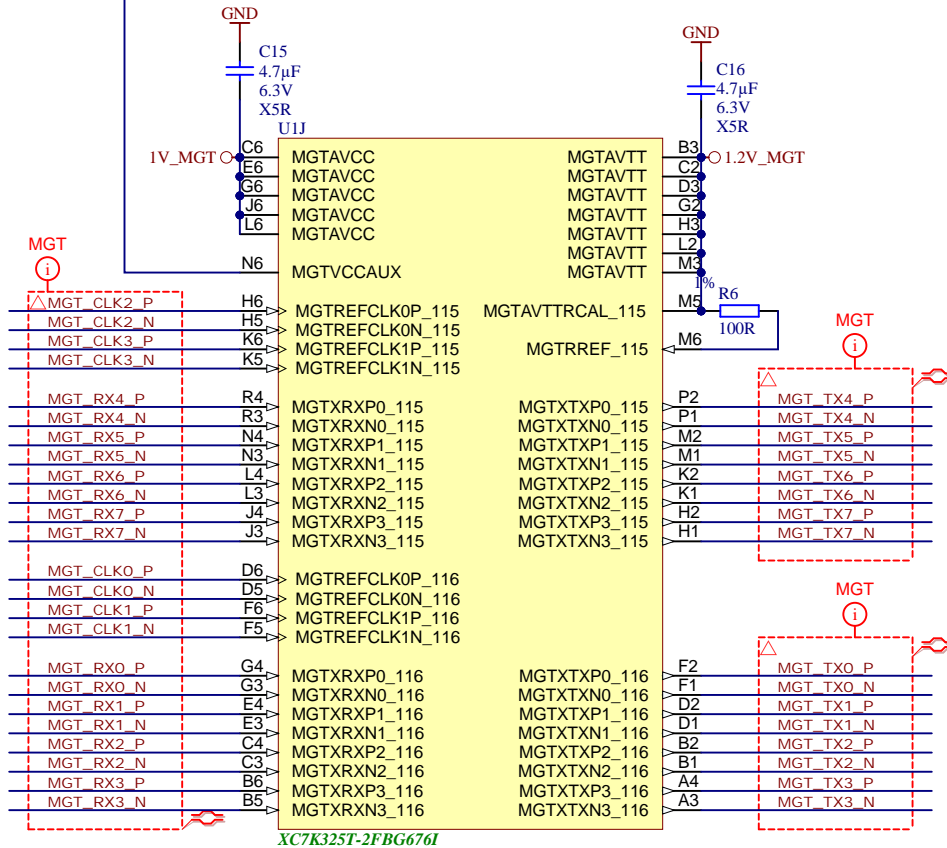
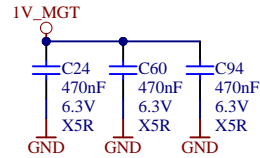
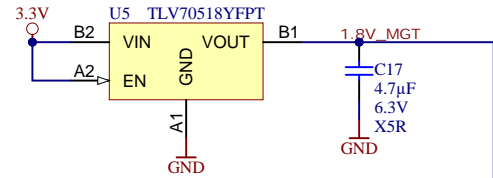

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A4	Number: <b>TE0741 D2I-1-A</b>	Rev. <b>04</b>
Date: <b>2016-10-25</b>	Copyright: <b>2013 Trenz Electronic GmbH</b>	Page <b>9</b> of <b>17</b>
Filename: <b>B34.SchDoc</b>		



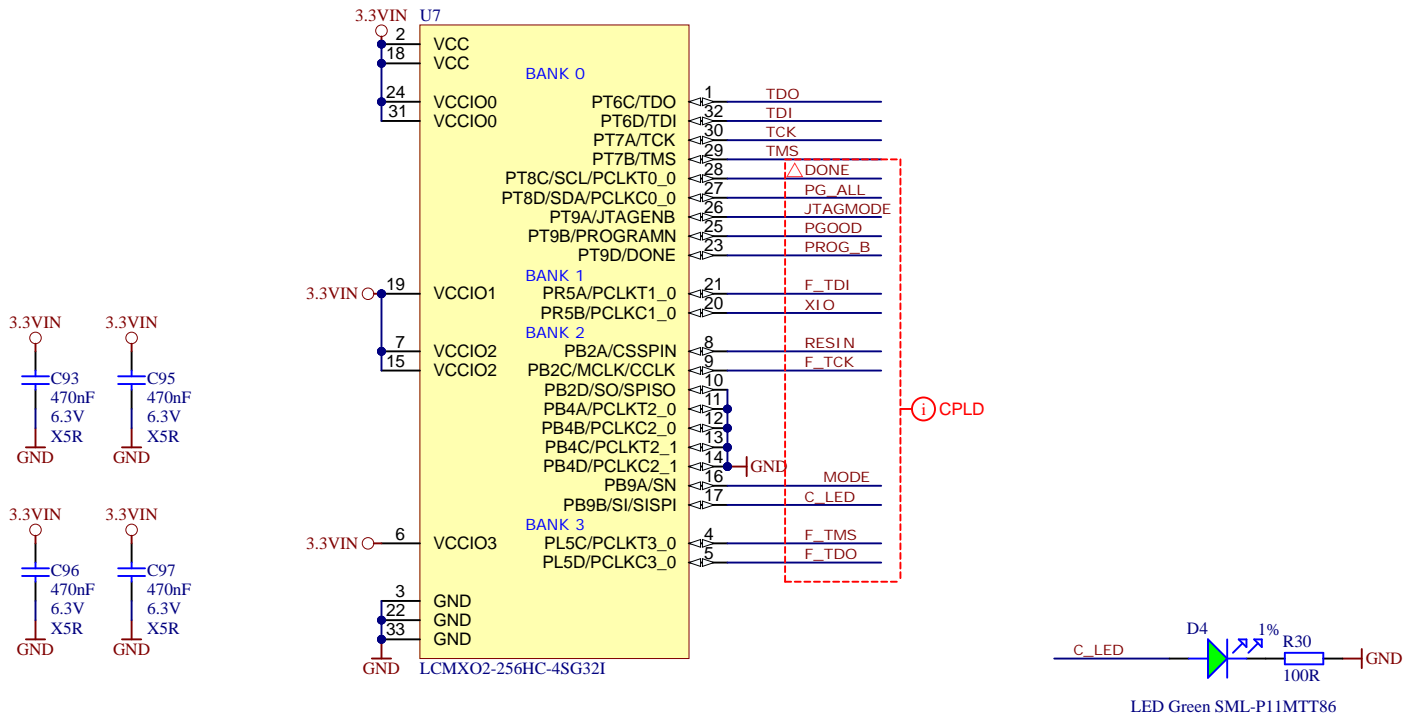
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		A4	Number: TE0741 D2I-1-A
Date: 2016-10-25		Copyright: 2013 Trenz Electronic GmbH	
Filename: Clock.SchDoc		Page 10 of 17	



Title: TE0741		
A4	Number: TE0741 D2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 11 of 17
Filename: FPGA-CFG.SchDoc		

Title: TE0741		
A4	Number: TE0741 D2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 12 of 17
Filename: FPGA-MGT.SchDoc		



Title: TE0741		
A4	Number: TE0741 D2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page13 of 17
Filename: FPGA-MISC.SchDoc		

1

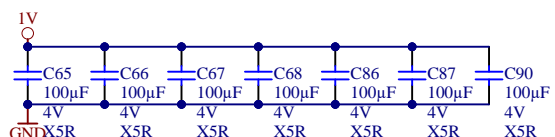
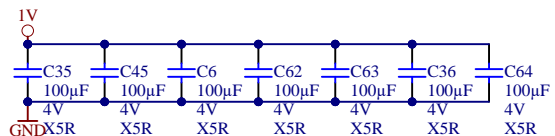
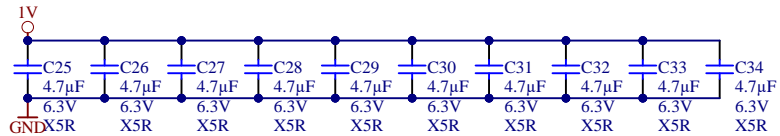
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A

A



B

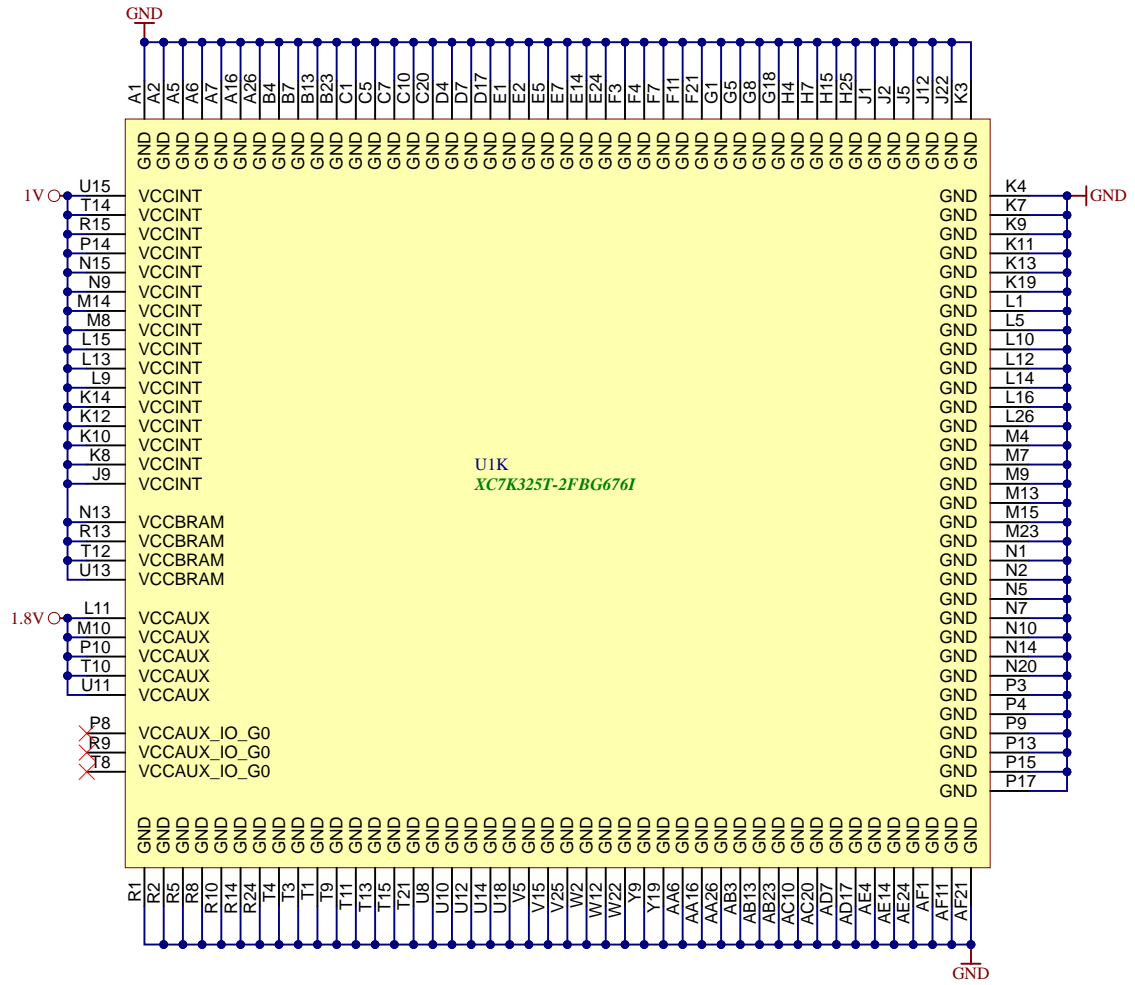
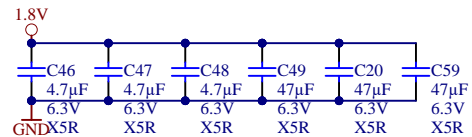
B

C

C

D

D



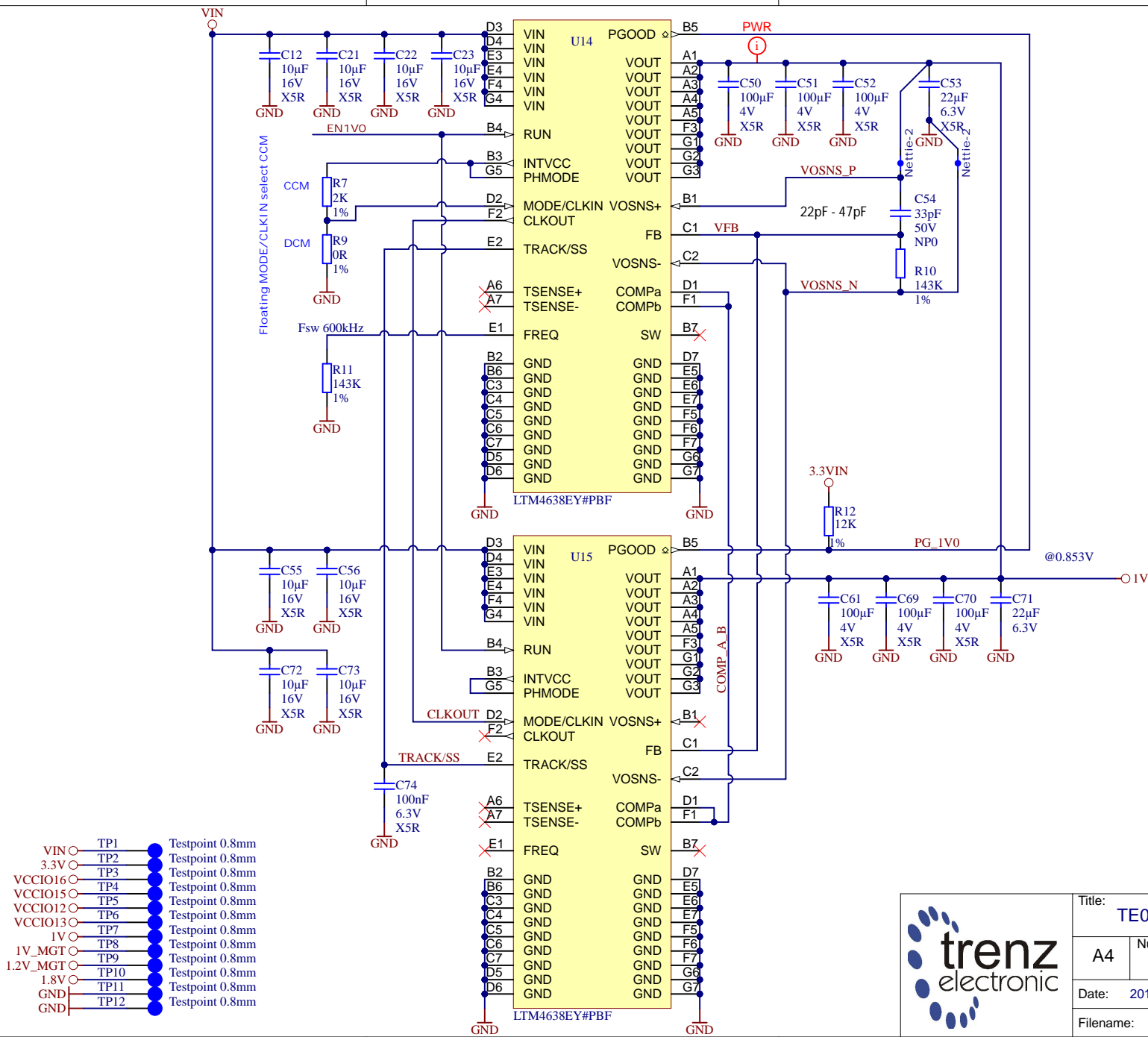
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A4	Number: TE0741 D2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 14 of 17
Filename: FPGA-PWR.SchDoc		

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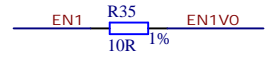
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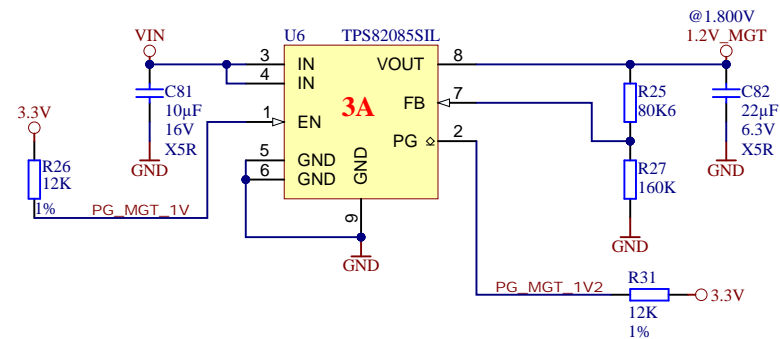
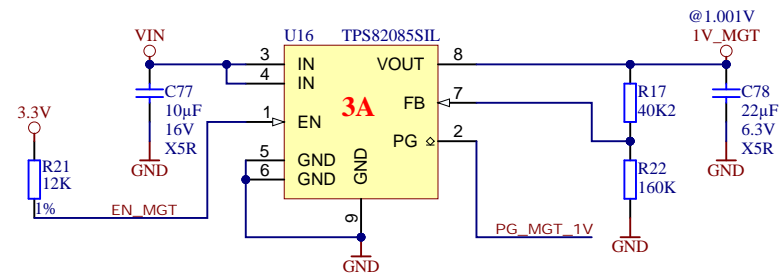
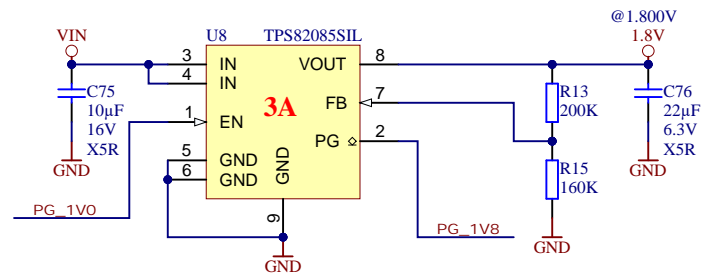
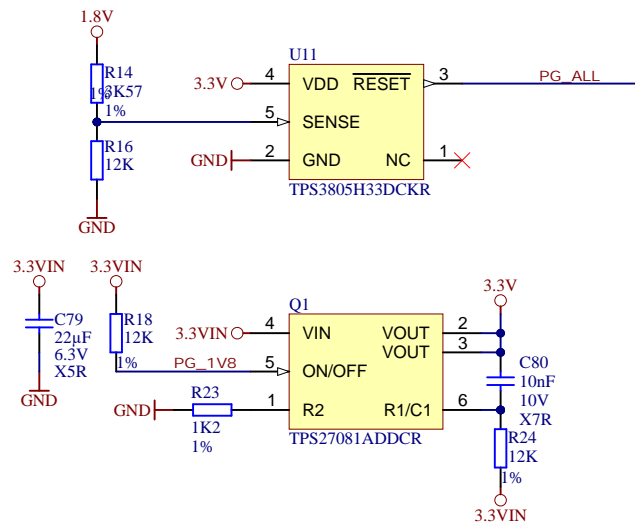
4




- VIN ○ TP1 ● Testpoint 0.8mm
- 3.3V ○ TP2 ● Testpoint 0.8mm
- VCCIO16 ○ TP3 ● Testpoint 0.8mm
- VCCIO15 ○ TP4 ● Testpoint 0.8mm
- VCCIO12 ○ TP5 ● Testpoint 0.8mm
- VCCIO13 ○ TP6 ● Testpoint 0.8mm
- 1V ○ TP7 ● Testpoint 0.8mm
- 1V\_MGT ○ TP8 ● Testpoint 0.8mm
- 1.2V\_MGT ○ TP9 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- GND ○ TP11 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm



Title: TE0741		
A4	Number: TE0741 D2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 15 of 17
Filename: PWR1.SchDoc		



		Title: TE0741	
		A4	Number: TE0741 D2I-1-A
Date: 2016-10-25		Copyright: 2013 Trenz Electronic GmbH	
Page 16		of 17	
Filename: PWR2.SchDoc			



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CHANGES REV02 to REV03

- 1) fixed connection DCDC for parallel operations
- 2) update Razorbeam Connectors, full update lib
- 3) added serial number (traceability pad)
- 4) changed ferrite beads L1..L4 size 0402 on BKP0603HS121-T
- 5) added thermal vias to mounting holes

Changes REV03 to REV04 (VT:10.2021):

- 1) replaced all DCDC (reason: not recommended use Enpirion DCDC)
- 2) remove Traceability Pad (reason: EOL)
- 3) added additional resistor for VBAT (reason: possibility using external VBAT from Carrier Board)
- 4) full upd LIB components
- 5) optimization PCB routing

A

A

B


B

C

C

D

D

		Title: TE0741 - Changes list	
		A4	Number: TE0741 D2I-1-A
Date: 2016-10-25		Copyright: Trenz Electronic GmbH	
Filename: Revision_Changes.SchDoc		Page 17 of 17	

1

2

3

4