

# NSP8814, NSP8818

## ESD and Surge Protection Device

### Low Capacitance Surge Protection for High Speed Data

The NSP8814 and NSP8818 surge protectors are designed specifically to protect 10/100 and GbE Ethernet signals from high levels of surge current. Low clamping voltage under high surge conditions make this device an ideal solution for protecting voltage sensitive lines leading to Ethernet transceiver chips. Low capacitance combined with flow-through style packaging allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high-speed differential lines.

#### Features

- Protection for the Following IEC Standards:
  - IEC 61000-4-2 (ESD)  $\pm 30$  kV (Contact)
  - IEC 61000-4-5 (Lightning) 35 A (8/20  $\mu$ s)
- Flow-Thru Routing Scheme
- Low Capacitance: 2 pF Max (I/O to I/O)
- UL Flammability Rating of 94 V-0
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- 10/100 and GbE Ethernet
- MagJacks® / Integrated Magnetics
- Notebooks/Desktops/Servers

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	$T_J$	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature – Maximum (10 Seconds)	$T_L$	260	$^\circ\text{C}$
IEC 61000-4-2 Contact (ESD) IEC 61000-4-2 Air (ESD)	ESD	$\pm 30$ $\pm 30$	kV
Maximum Peak Pulse Current 8/20 $\mu$ s @ $T_A = 25^\circ\text{C}$ 10/700 $\mu$ s @ $T_A = 25^\circ\text{C}$	$I_{pp}$	35 20	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

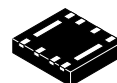
See Application Note AND8308/D for further description of survivability specs.



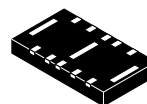
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

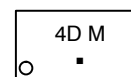
#### MARKING DIAGRAMS



UDFN8  
CASES 506CV



UDFN10  
CASE 506CU



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

#### ORDERING INFORMATION

Device	Package	Shipping
NSP8814MUTAG	UDFN8 (Pb-Free)	3000 / Tape & Reel
NSP8818MUTAG	UDFN10 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NSP8814, NSP8818

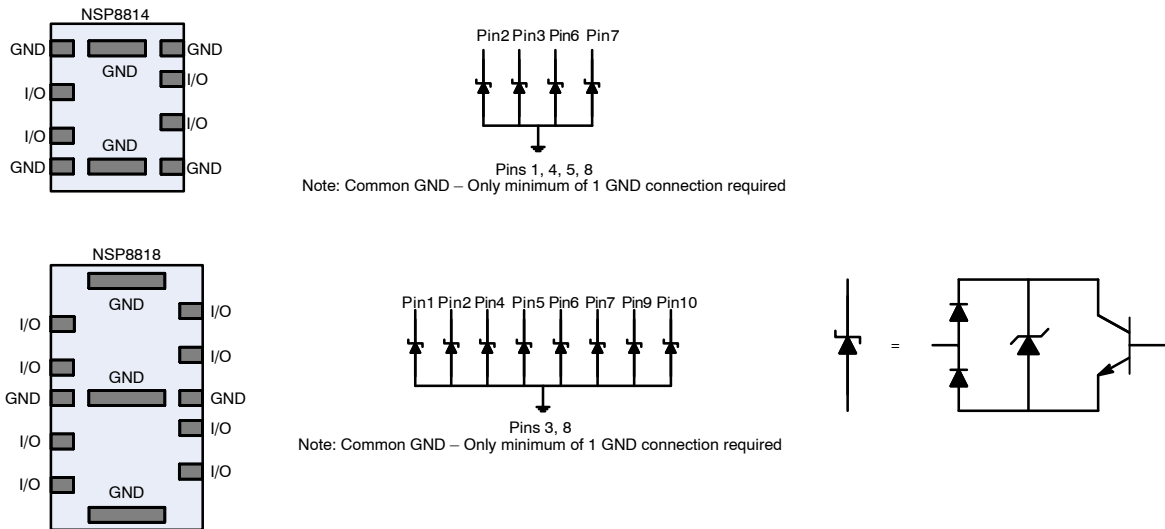
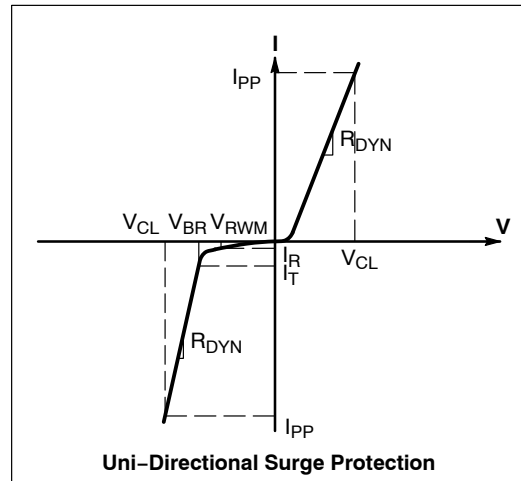


Figure 1. Pin Schematic

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$V_{RWM}$	Working Peak Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$V_{HOLD}$	Holding Reverse Voltage
$I_{HOLD}$	Holding Reverse Current
$R_{DYN}$	Dynamic Resistance
$I_{PP}$	Maximum Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$ $V_C = V_{HOLD} + (I_{PP} * R_{DYN})$



## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	Any I/O to GND (Note 1)			3.0	V
Forward Voltage	$V_F$	$I_F = 10 \text{ mA}$ , GND to All IO Pins	0.5	0.85	1.1	V
Breakdown Voltage	$V_{BR}$	$I_T = 1 \text{ mA}$ , I/O to GND	3.2	3.5	5.0	V
Reverse Leakage Current	$I_R$	$V_{RWM} = 3.0 \text{ V}$ , I/O to GND			0.5	$\mu\text{A}$
Clamping Voltage (Note 2)	$V_C$	$I_{PP} = 1 \text{ A}$ $I_{PP} = 10 \text{ A}$ $I_{PP} = 25 \text{ A}$ $I_{PP} = 35 \text{ A}$		4.0 6.0 8.0 10	5.0 6.5 10 15	V
Clamping Voltage	$V_C$	IEC61000-4-2, $\pm 8 \text{ kV}$ Contact	See Figures 7 and 14			V
Junction Capacitance	$C_J$	$V_R = 0 \text{ V}$ , $f = 1 \text{ MHz}$ between I/O Pins		1.5	2.0	pF
		$V_R = 0 \text{ V}$ , $f = 1 \text{ MHz}$ between I/O Pins and GND			5.0	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Surge protection devices are normally selected according to the working peak reverse voltage ( $V_{RWM}$ ), which should be equal or greater than the DC or continuous peak operating voltage level.
- Any I/O to GND (8/20  $\mu\text{s}$  pulse).

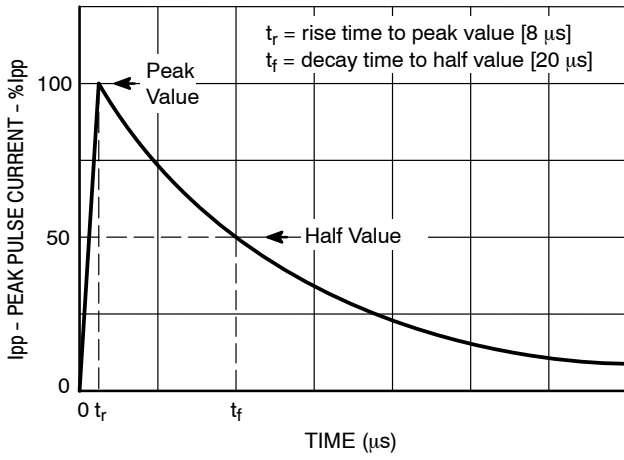


Figure 2. IEC61000-4-5 8/20  $\mu$ s Pulse Waveform

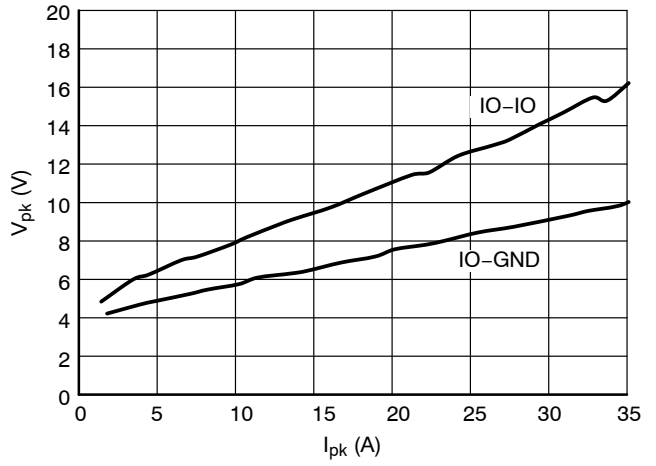


Figure 3. Clamping Voltage vs. Peak Pulse Current ( $t_p = 8/20 \mu$ s per Figure 2)

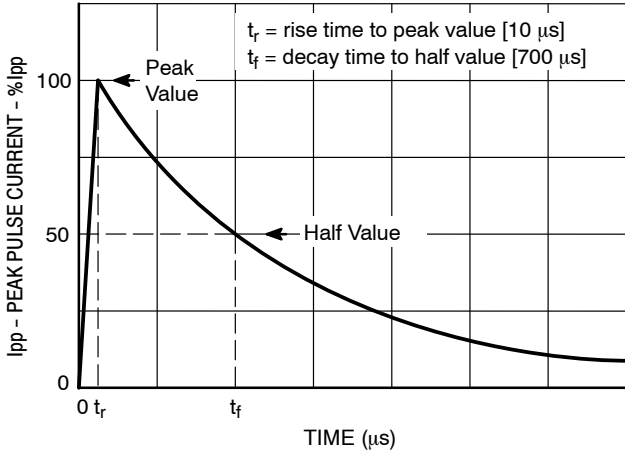


Figure 4. IEC61000-4-5 10/700  $\mu$ s Pulse Waveform

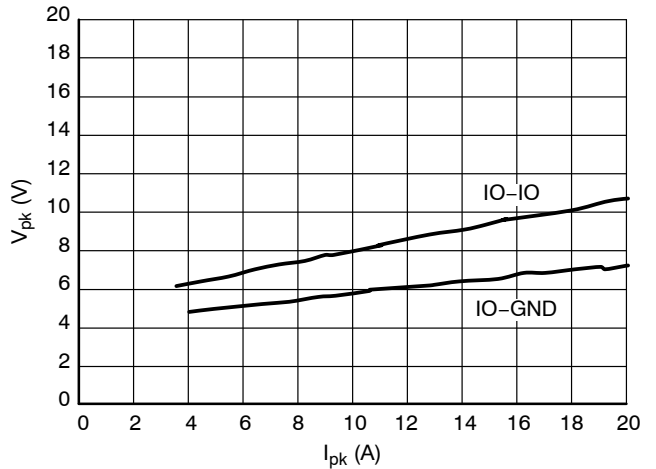


Figure 5. Clamping Voltage vs. Peak Pulse Current ( $t_p = 10/700 \mu$ s per Figure 4)

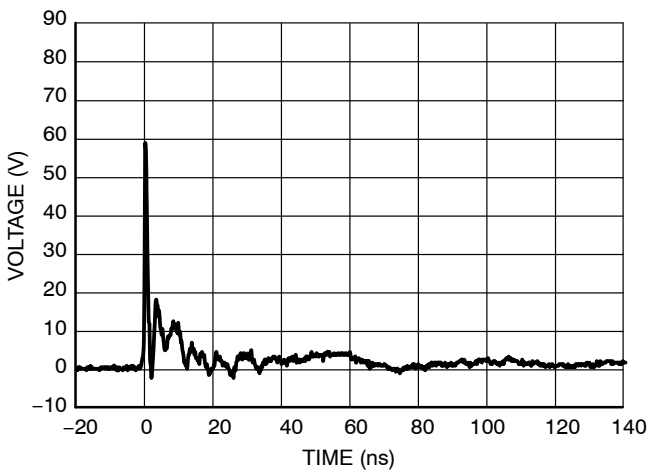


Figure 6. IEC61000-2-4 +8 kV Contact Clamping Voltage

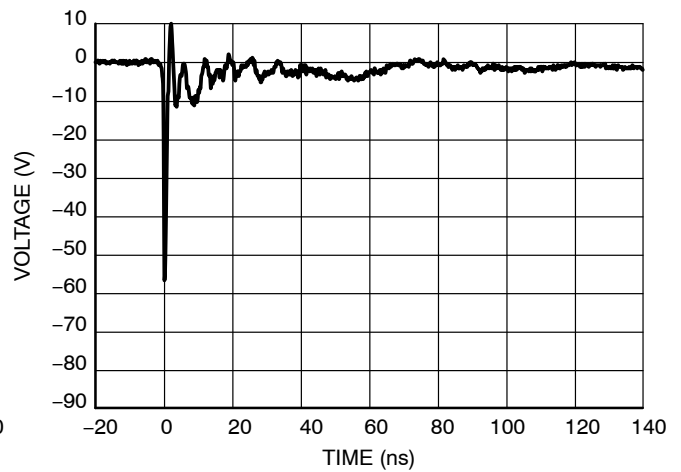


Figure 7. IEC61000-2-4 -8 kV Contact Clamping Voltage

# NSP8814, NSP8818

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 8. IEC61000-4-2 Spec

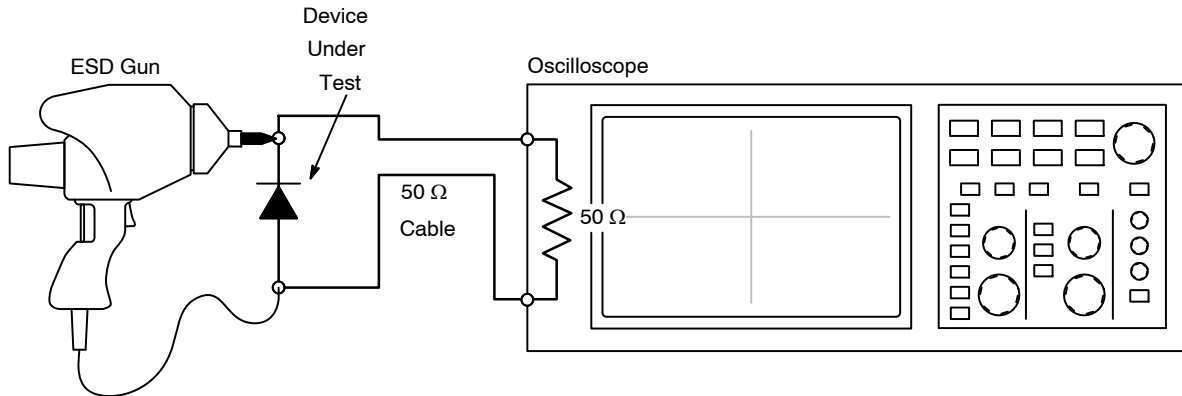


Figure 9. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

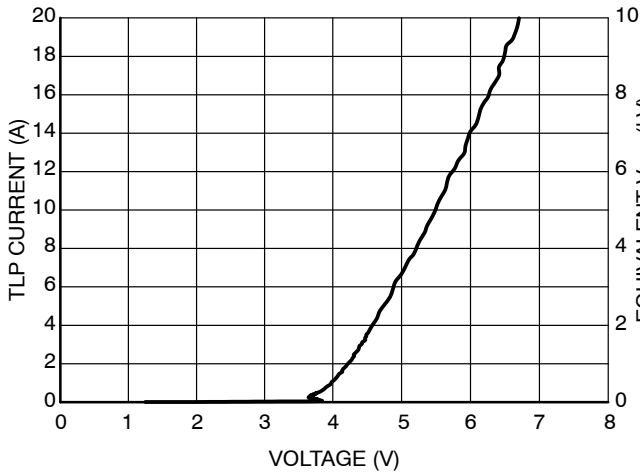


Figure 10. Positive TLP IV Curve

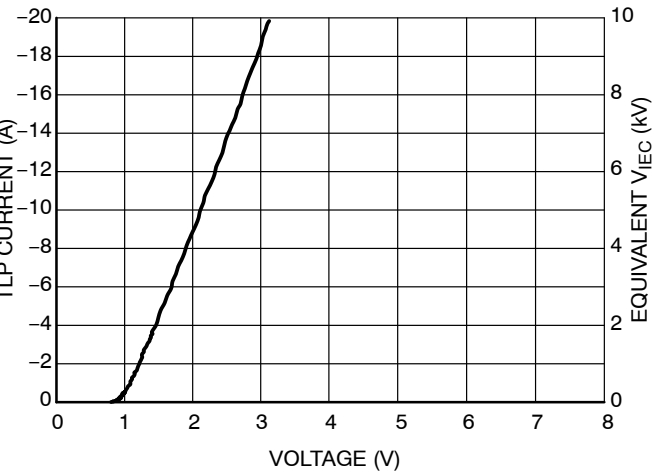


Figure 11. Negative TLP IV Curve

NOTE: TLP parameter:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 300 \text{ ps}$ , averaging window:  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ .

**Transmission Line Pulse (TLP) Measurement**

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 12. TLP I-V curves of ESD protection devices accurately demonstrate the product’s ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 13 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

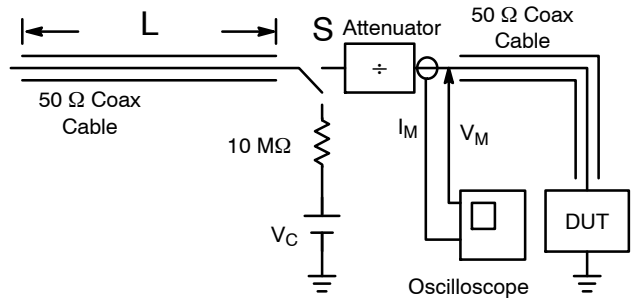


Figure 12. Simplified Schematic of a Typical TLP System

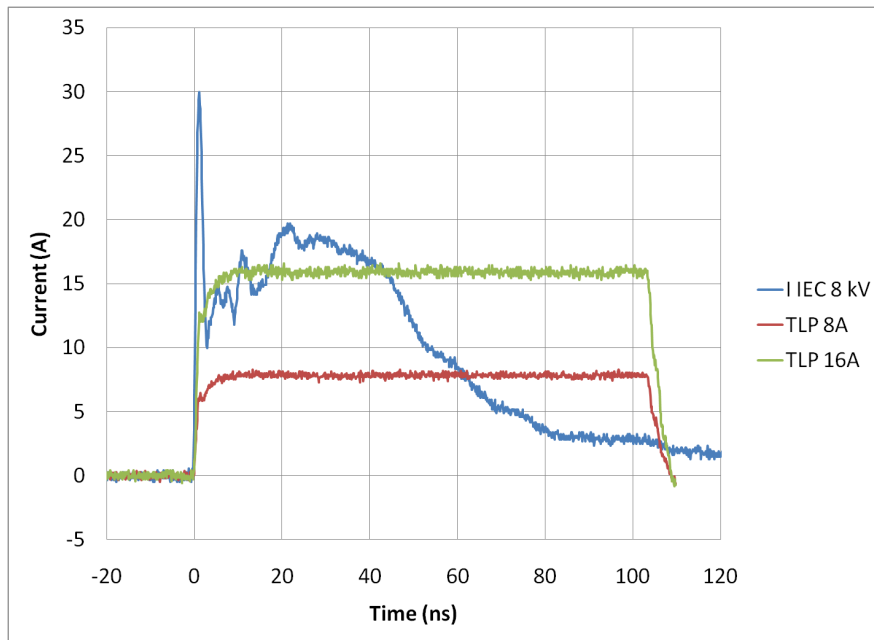


Figure 13. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

# NSP8814, NSP8818

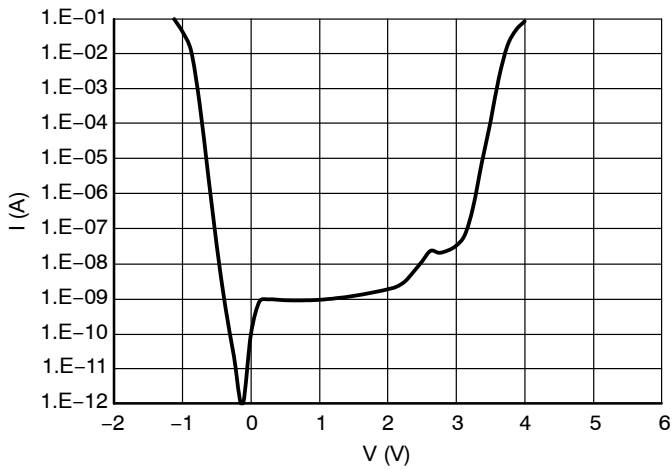


Figure 14. IV Characteristics

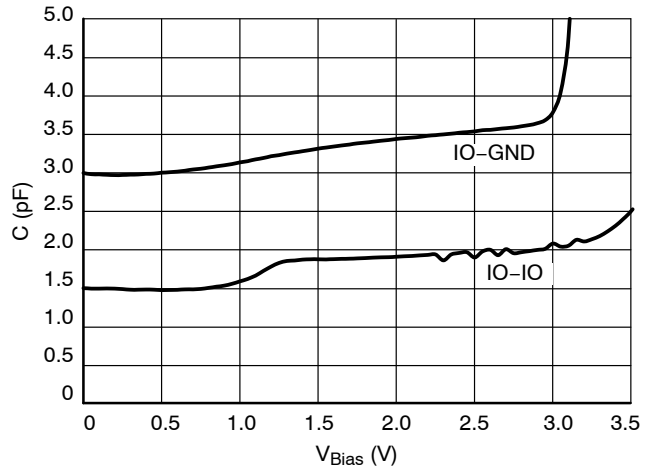


Figure 15. CV Characteristics

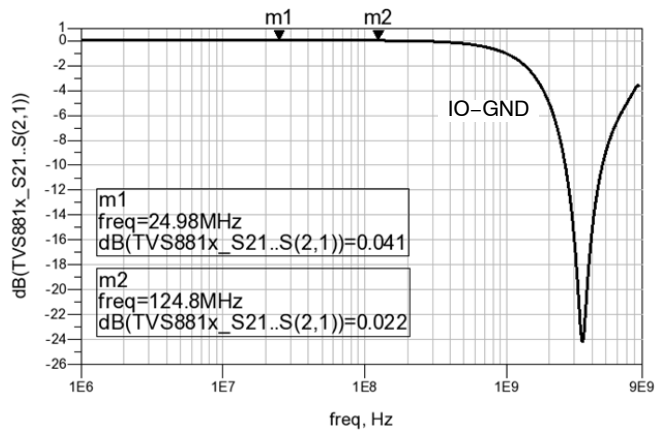


Figure 16. RF Insertion Loss

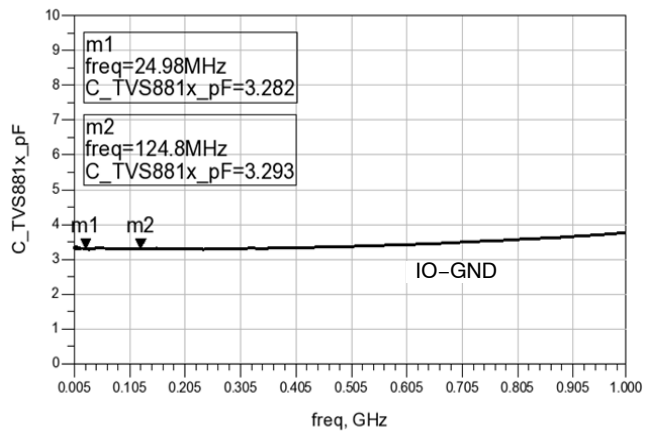


Figure 17. Capacitance Over Frequency

# NSP8814, NSP8818

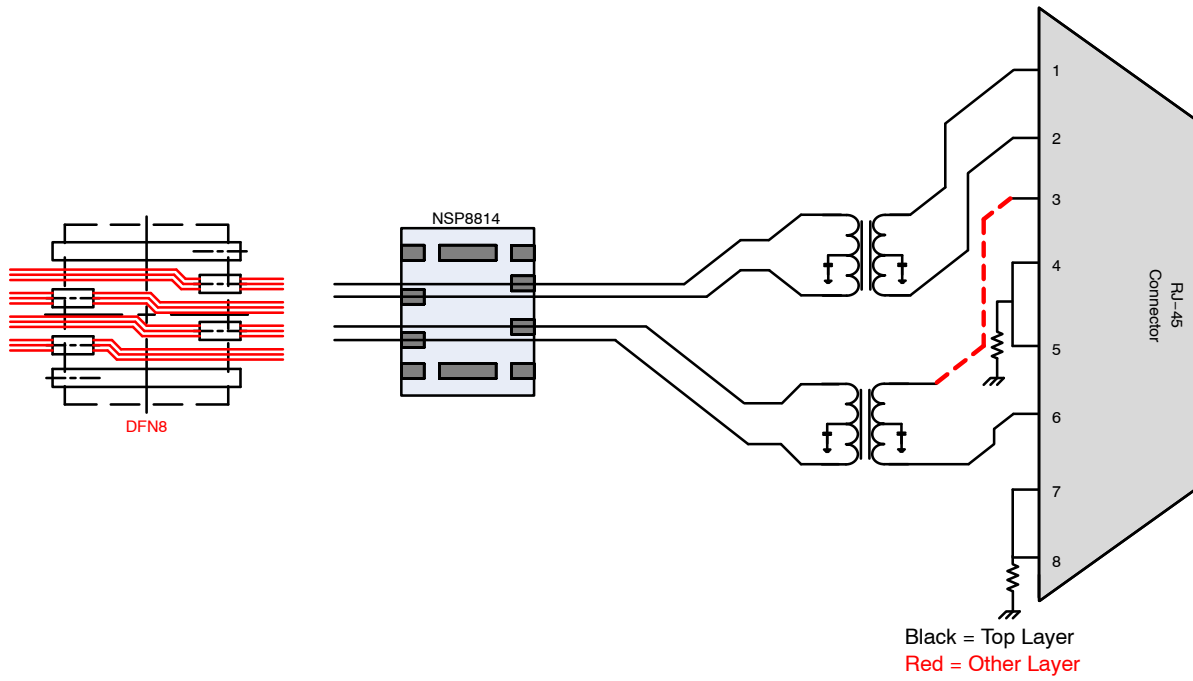


Figure 18. 10/100 Ethernet Layout Diagram and Flow-thru Routing Scheme

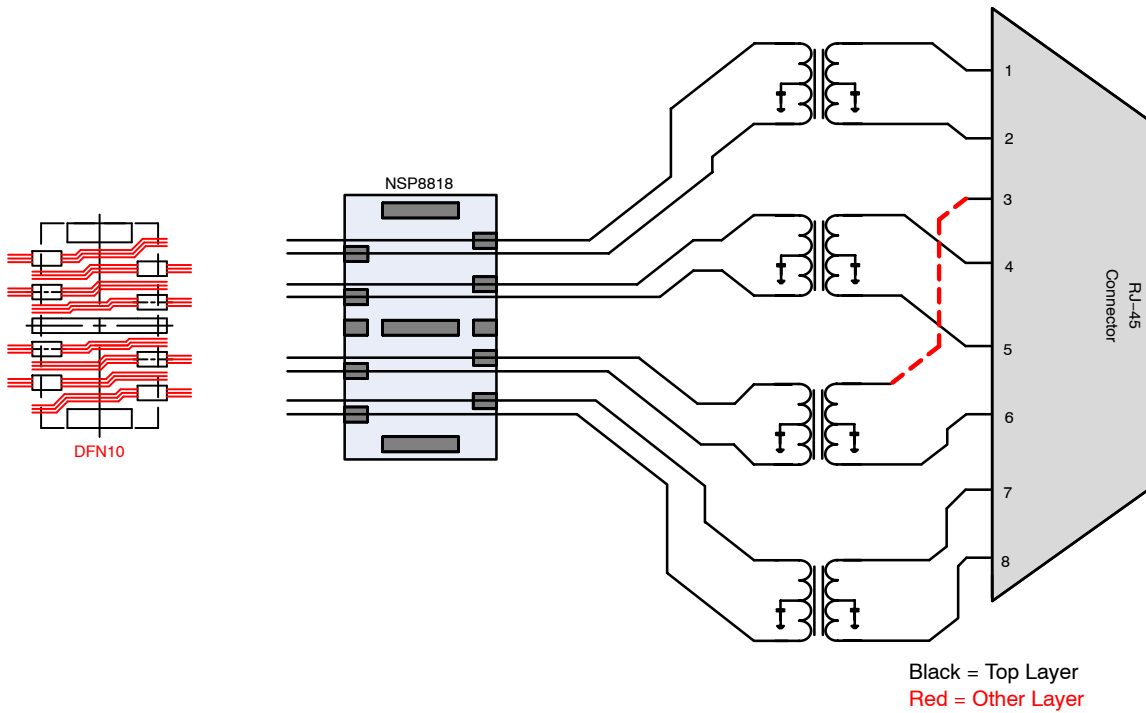
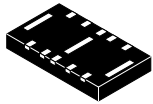


Figure 19. GbE Ethernet Layout Diagram and Flow-thru Routing Scheme

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

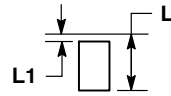
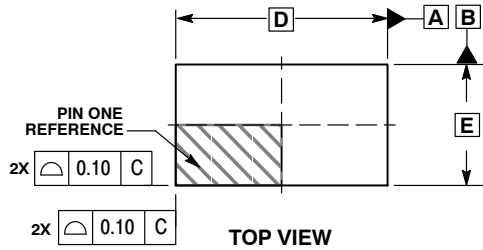
ON Semiconductor®



SCALE 4:1

UDFN10 3.5x2, 0.575P  
CASE 506CU  
ISSUE O

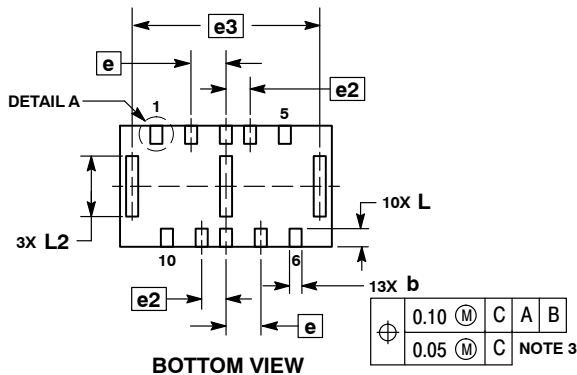
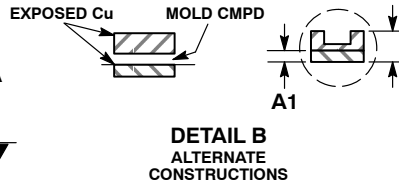
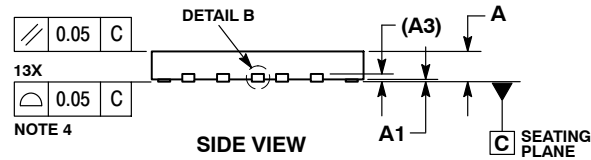
DATE 05 NOV 2013



NOTES:

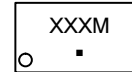
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
D	3.50 BSC	
E	2.00 BSC	
e	0.575 BSC	
e2	0.40 BSC	
e3	3.10 BSC	
L	0.25	0.35
L1	0.05	0.15
L2	0.95	1.05



⊕	0.10	(M)	C	A	B
	0.05	(M)	C	NOTE 3	

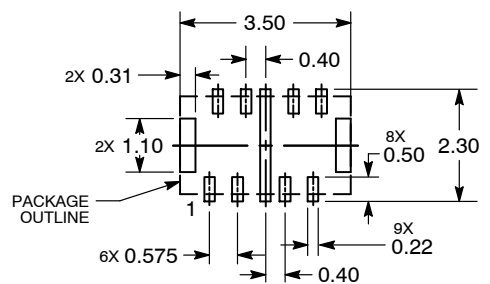
### GENERIC MARKING DIAGRAM\*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

<b>DOCUMENT NUMBER:</b>	<b>98AON79787F</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>UDFN10 3.5X2, 0.575P</b>	<b>PAGE 1 OF 1</b>

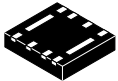
ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.



# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

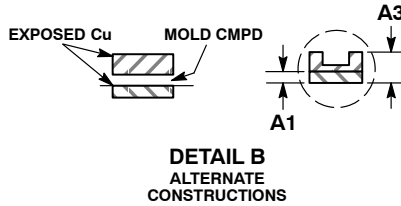
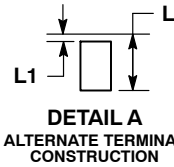
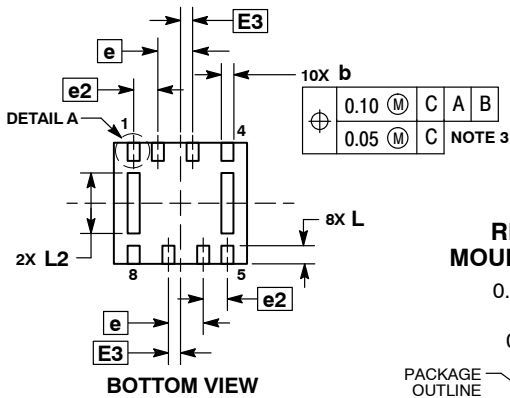
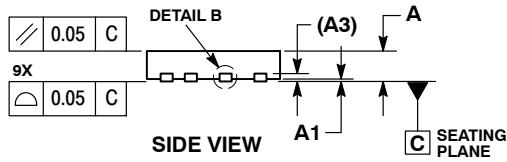
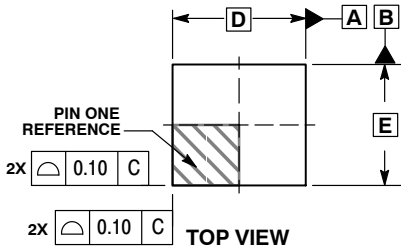
ON Semiconductor®



SCALE 4:1

### UDFN8 2.2x2, 0.575P CASE 506CV ISSUE A

DATE 21 JUL 2015



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
D	2.20	BSC
E	2.00	BSC
E3	0.20	BSC
e	0.575	BSC
e2	0.40	BSC
L	0.25	0.35
L1	0.05	0.15
L2	0.95	1.05

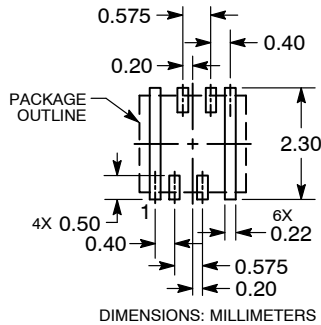
### GENERIC MARKING DIAGRAM\*



XX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### RECOMMENDED MOUNTING FOOTPRINT



<b>DOCUMENT NUMBER:</b>	<b>98AON79913F</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>UDFN8 2.2X2, 0.575P</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

North American Technical Support:  
Voice Mail: 1 800-282-9855 Toll Free USA/Canada  
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative