

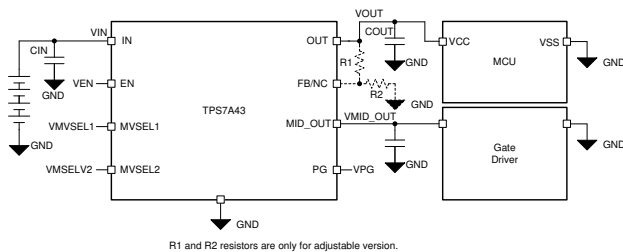
# TPS7A43 50-mA, 85-V, Low $I_Q$ , Dual Output Low-Dropout Linear Voltage Regulator With Precision Enable & Power-Good

## 1 Features

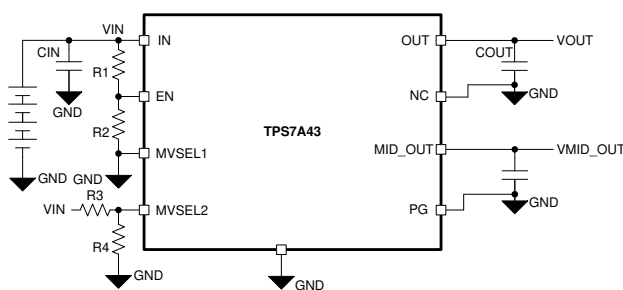
- Input voltage: 4 V to 85 V
- Ultra-low  $I_Q$ : 6.5  $\mu$ A
- Wide output voltage range:
  - Adjustable: 1.24 V to 14.5 V
  - Fixed: 1.25 V to 5.0 V
- Intermediate output (MID\_OUT): 10 V, 12 V, 15 V
- Precision enable
- 1% accuracy over temperature
- Power-good (PG) output (open-drain)
- Thermal shutdown and overcurrent protection
- Operating junction temperature:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package: HVSSOP-10 ( $R_{\theta JA} = 53.7^{\circ}\text{C/W}$ )

## 2 Applications

- [Cordless power tools](#)
- [DC motors and fans](#)
- [Programmable logic controllers \(PLCs\)](#)
- [Field transmitter and process sensors](#)
- [Smoke and heat detectors](#)
- [EV charging infrastructure](#)
- [Battery packs](#)



### Powering Cordless Power Tools



Setting MID\_OUT voltage to 12 V or 15 V using R3 and R4 resistors.

### Powering the MCU for Battery Packs

## 3 Description

The TPS7A43 low-dropout (LDO) linear voltage regulator introduces a combination of a 4-V to 85-V input voltage range with very-low quiescent current ( $I_Q$ ).

This device can support a wide range of input voltages (for example, a 15s battery and 24-V to 48-V line power) and withstand line transient voltages up to 85 V. These features help modern appliances meet increasingly stringent energy requirements, and help extend battery life in portable-power solutions.

The TPS7A43 is available in both fixed and adjustable output versions. Fixed output options are available in standard voltage options and the adjustable output version uses external feedback resistors to set the output voltage from 1.24 V to 14.5 V. The main output (OUT) has a 1% output regulation accuracy that provides precision regulation for most microcontroller (MCU) references. The device also provides a second intermediate output (MID\_OUT) that can be used to bias gate drivers in place of a discrete regulator. The MID\_OUT uses two logic pins (MVSEL1 and MVSEL2) to adjust the intermediate output rail between 10 V, 12 V, or 15 V.

The TPS7A43 features a precision enable input that helps enable or disable the LDO at a fixed and accurate threshold voltage using a resistor divider from the input.

The power-good (PG) output is used to monitor the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output can be used for sequencing multiple power sources in the system. The built-in current limit and thermal shutdown help protect the regulator in the event of a load short or fault.

### Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A43	HVSSOP (10)	3.00 mm × 3.00 mm

- (1) For all available packages, see the package option addendum at the end of the datasheet.



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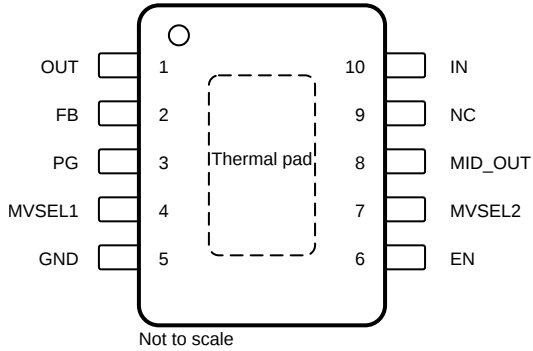
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## 4 Revision History

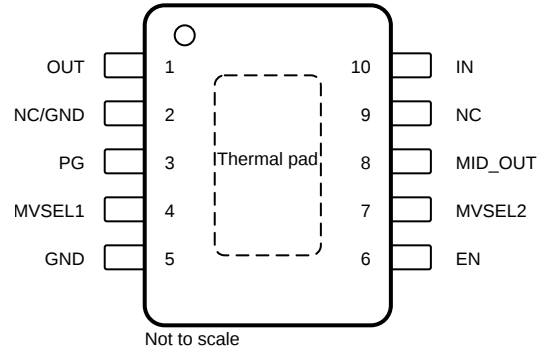
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial Release

## 5 Pin Configuration and Functions



**Figure 5-1. DGQ Package (Adjustable), Top View**



**Figure 5-2. DGQ Package (Fixed), 10-Pin HVSSOP, Top View**

**Table 5-1. Pin Functions**

NAME	PIN		I/O	DESCRIPTION
	DGQ (Adjustable)	DGQ (Fixed)		
EN	6	6	Input	Precision enable pin. Driving this pin to logic high enables the device. Driving this pin to logic low disables the device. This pin can be left floating to enable the device because the device features an internal pullup resistor to the IN pin. If this pin is tied to the IN pin then the input voltage must not exceed 18 V; see the <a href="#">Recommended Operating Conditions</a> table.
FB	2	—	Input	Feedback pin. Input to the control-loop error amplifier. This pin is used to set the output voltage of the device with the use of external resistors. For adjustable-voltage version devices only. This pin must not be left floating.
GND	5	5	—	Ground pin.
IN	10	10	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground; see the <a href="#">Recommended Operating Conditions</a> table. Place the input capacitor as close to the IN and GND pins of the device as possible.
MID_OUT	8	8	Output	MID output pin. A capacitor is required from MID_OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor from MID_OUT to ground. Follow the recommended capacitor value as listed in the <a href="#">Recommended Operating Conditions</a> table. Place the MID output capacitor as close to the MID_OUT and GND pins of the device as possible.
MVSEL1	4	4	Input	Mid output voltage select pin. The MVSEL1 and MVSEL2 pins can be used to set the MID_OUT output voltage; see the <a href="#">Electrical Characteristics</a> table for details on how to set the MID_OUT voltage using the MVSEL1 and MVSEL2 pins.
MVSEL2	7	7	Input	Mid output voltage select pin. The MVSEL2 and MVSEL1 pins can be used to set the MID_OUT output voltage; see the <a href="#">Electrical Characteristics</a> table for details on how to set the MID_OUT voltage using the MVSEL1 and MVSEL2 pins.
NC	9	9	—	No internal connection. This pin must be left floating.
NC/GND	—	2	—	No internal connection. This pin can be left floating or tied to the GND plane to improve thermal performance.
OUT	1	1	Output	Output pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor from OUT to ground. Follow the recommended capacitor value as listed in the <a href="#">Recommended Operating Conditions</a> table. Place the output capacitor as close to the OUT and GND pins of the device as possible.
PG	3	3	Output	Power-good pin; an open-drain output indicates when the output voltage reaches $V_{IT(PG, RISING)}$ (typical). If not used, this pin can be left floating or tied to the GND plane to improve thermal performance.

Table 5-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	DGQ (Adjustable)	DGQ (Fixed)		
Thermal pad	Pad	Pad	—	Exposed pad of the package. Connect this pad to ground or leave floating. Connect the thermal pad to a large-area GND plane for improved thermal performance.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage <sup>(2)</sup>	V <sub>IN</sub>	-0.3	90	V
	V <sub>OUT</sub> <sup>(3)</sup> (adjustable version)	-0.3	V <sub>MID</sub> + 0.3	
	V <sub>OUT</sub> (fixed version)	-0.3	5.5	
	V <sub>MID_OUT</sub> <sup>(4)</sup>	-0.3	V <sub>IN</sub> + 0.3	
	V <sub>FB</sub>	-0.3	5.5	
	V <sub>EN</sub>	-0.3	20	
	V <sub>MVSEL1</sub>	-0.3	20	
	V <sub>MVSEL2</sub>	-0.3	20	
Current	Maximum output	Internally limited		A
	Maximum MID output	Internally limited		
Temperature	Operating junction, T <sub>J</sub>	-50	150	°C
	Storage, T <sub>stg</sub>	-65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages with respect to GND.

(3) V<sub>MID\_OUT</sub> + 0.3 V or 20 V (whichever is smaller).

(4) V<sub>IN</sub> + 0.3 V or 20 V (whichever is smaller).

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±750	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage	4		85	V
V <sub>MID_OUT</sub>	MID output voltage	10		15	V
V <sub>OUT</sub>	Output voltage (adjustable version)	1.24		V <sub>MID_OUT</sub> - V <sub>DO(OUT)</sub>	V
V <sub>OUT</sub>	Output voltage (fixed version)	1.25		5.5	V
I <sub>OUT</sub>	Output current	0		50 - I <sub>MID_OUT</sub>	mA
I <sub>MID_OUT</sub>	MID rail output current	0		50	mA
V <sub>MVSEL1</sub>	MID voltage select input voltage 1	0		18	V
V <sub>MVSEL2</sub>	MID voltage select input voltage 2	0		18	V
V <sub>EN</sub>	Enable voltage	0		18	V
V <sub>PG</sub> <sup>(1)</sup>	Power-good voltage	0		18	V
C <sub>IN</sub> <sup>(2)</sup>	Input capacitor		0.1		μF
C <sub>OUT</sub> <sup>(2)</sup>	Output capacitor	1	2.2	100	μF
C <sub>MID_OUT</sub> <sup>(2) (3)</sup>	MID output capacitor	3 x C <sub>OUT</sub>			μF
T <sub>J</sub>	Operating junction temperature	-40		125	°C

- (1) Select pullup resistor to limit PG pin sink current when PG output is driven low. See *Power Good* section for details.  
(2) All capacitor values are assumed to derate to 50% of the nominal capacitor value.  
(3) Maintain a 3:1 ratio between C<sub>MID\_OUT</sub> vs C<sub>OUT</sub> for stability

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS7A43		UNIT
		HVSSOP (DGQ)		
		8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	53.7		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	76.6		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	26.8		°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.6		°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	26.7		°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	9.6		°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

specified at  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 1.5\text{V}$  or  $4\text{V}$ , whichever is greater, FB tied to OUT (adjustable version only),  $I_{OUT} = 1\text{mA}$ ,  $I_{MID\_OUT} = \text{open}$ ,  $V_{EN} = 2\text{V}$ ,  $V_{MVSEL1} = 0.9\text{V}$ ,  $V_{MVSEL2} = 0.9\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_{MID\_OUT} = 4.7\mu\text{F}$ , and  $C_{OUT} = 1\mu\text{F}$  (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\Delta V_{OUT}$	Output voltage accuracy	Adjustable version, $V_{OUT} = V_{FB}$		1.228	1.24	1.252	V
$\Delta V_{OUT}$		Fixed output version, $T_J = 25^\circ\text{C}$		-0.5		0.5	%
$\Delta V_{OUT}$		Fixed output version		-1		1	
$V_{FB}$	Feedback voltage	Adjustable version only			1.24		V
$\Delta V_{OUT(\Delta V_{IN})}$	Line regulation <sup>(1)</sup>	$(V_{OUT(nom)} + 1\text{V or }4\text{V}) \leq V_{IN} \leq 85\text{V}$		-0.1		0.1	%
$\Delta V_{OUT(\Delta V_{IN})}$		$V_{MID\_OUT(nom)} + 1.5\text{V} \leq V_{IN} \leq 85\text{V}$		-0.01		0.01	
$\Delta V_{OUT(\Delta I_{OUT})}$	Load regulation	$1\text{mA} \leq I_{OUT} \leq 50\text{mA}$ , $I_{MID\_OUT} = 0\text{mA}$		-0.5		0.5	%
$\Delta V_{MID\_OUT}$	MID output voltage accuracy	$V_{IN} = V_{MID\_OUT} + 1.5\text{V}$	$V_{MVSEL1} \leq V_{MVSEL1(LOW)}$ , $V_{MVSEL2} \leq V_{MVSEL2(LOW)}$	14.25	15	15.75	V
			$V_{MVSEL1} \leq V_{MVSEL1(LOW)}$ or $V_{MVSEL1} \geq V_{MVSEL1(HIGH)}$ , $V_{MVSEL2} \geq V_{MVSEL2(HIGH)}$	11.4	12	12.6	
			$V_{MVSEL1} \geq V_{MVSEL1(HIGH)}$ , $V_{MVSEL2} \leq V_{MVSEL2(LOW)}$	9.5	10	10.5	
$\Delta V_{MID\_OUT(\Delta V_{IN})}$	Line regulation of MID output <sup>(1)</sup>	$(V_{MID\_OUT(nom)} + 1.5\text{V} \leq V_{IN} \leq 85\text{V}$ , $I_{MID\_OUT} = 1\text{mA}$ , $I_{OUT} = 0\text{mA}$		-0.1		0.1	%
$\Delta V_{MID\_OUT(\Delta I_{OUT})}$	Load regulation of MID output	$1\text{mA} \leq I_{MID\_OUT} \leq 50\text{mA}$ , $V_{IN} = V_{MID\_OUT} + 1.5\text{V}$ , $I_{OUT} = 0\text{mA}$		-0.3		0.3	%
$V_{DO(OUT)}$	Dropout voltage of $V_{MID\_OUT}$ to $V_{OUT}$ <sup>(2)</sup>	$I_{OUT} = 50\text{mA}$				200	mV
$V_{DO(MID\_OUT)}$	Dropout voltage of $V_{IN}$ to $V_{MID\_OUT}$ <sup>(2)</sup>	$I_{MID\_OUT} = 50\text{mA}$				600	mV
$I_{CL(OUT)}$	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(nom)}$		100	125	165	mA
$I_{CL(MID\_OUT)}$	MID output current limit	$V_{OUT} = 0.9 \times V_{MID\_OUT(nom)}$ , $V_{IN} = V_{MID\_OUT} + 1.5\text{V}$		100	125	160	mA
$I_{GND}$	Ground pin current	$I_{OUT} = I_{MID\_OUT} = 0\text{mA}$ , $V_{IN} = V_{MID\_OUT} + 1.5\text{V}$	$T_J = 25^\circ\text{C}$		5.5	7	$\mu\text{A}$
			$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$			9	$\mu\text{A}$
$I_{SHUTDOWN}$	Shutdown current	$V_{EN} \leq V_{EN(LOW)}$ , $V_{MID\_OUT(nom)} + 1.5\text{V} \leq V_{IN} \leq 85\text{V}$ , $I_{OUT} = I_{MID\_OUT} = 0\text{mA}$			710	1900	nA
$I_{FB}$	FB pin current				10		nA
$I_{MVSEL1}$	MVSEL1 pin current	$V_{MVSEL1} = 17\text{V}$			10		nA
$I_{MVSEL2}$	MVSEL2 pin current	$V_{MVSEL2} = 17\text{V}$			10		nA
$I_{EN}$	EN pin current	$V_{EN} = 17\text{V}$			10		nA
$V_{MVSEL1(HIGH)}$	MVSEL1 pin high-level input voltage			0.9			V
$V_{MVSEL1(LOW)}$	MVSEL1 pin low-level input voltage					0.3	V
$V_{MVSEL2(HIGH)}$	MVSEL2 pin high-level input voltage			0.9			V
$V_{MVSEL2(LOW)}$	MVSEL2 pin low-level input voltage					0.3	V
$V_{EN(HI)}$	Enable rising threshold	Device enabled		1.2	1.24	1.35	V

## 6.5 Electrical Characteristics (continued)

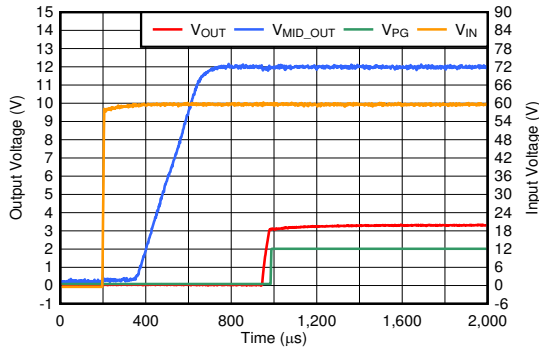
specified at  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 1.5\text{V}$  or  $4\text{V}$ , whichever is greater, FB tied to OUT (adjustable version only),  $I_{OUT} = 1\text{ mA}$ ,  $I_{MID\_OUT} = \text{open}$ ,  $V_{EN} = 2\text{ V}$ ,  $V_{MVSEL1} = 0.9\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{MID\_OUT} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{EN(LOW)}$	Enable falling threshold	Device disabled	1.15	1.19	1.27	V
$V_{EN(HYST)}$	Enable pin hysteresis			50		mV
$V_{IT(PG,RISING)}$	PG pin threshold rising	$R_{PULLUP} = 10\text{ k}\Omega$ , $V_{OUT}$ rising, $V_{IN} \geq V_{UVLO(RISING)}$		93	96.5	$\%V_{OUT}$
$V_{HYS(PG)}$	PG pin hysteresis	$R_{PULLUP} = 10\text{ k}\Omega$ , $V_{OUT}$ falling, $V_{IN} \geq V_{UVLO(RISING)}$		3		$\%V_{OUT}$
$V_{IT(PG,FALLING)}$	PG pin threshold falling	$R_{PULLUP} = 10\text{ k}\Omega$ , $V_{OUT}$ falling, $V_{IN} \geq V_{UVLO(RISING)}$	84	90		$\%V_{OUT}$
$V_{OL(PG)}$	PG pin low level output voltage	$V_{OUT} < V_{IT(PG,FALLING)}$ , $I_{PG-SINK} = 500\text{ }\mu\text{A}$			0.4	V
$I_{LKG(PG)}$	PG pin leakage current	$V_{OUT} > V_{IT(PG,RISING)}$ , $V_{PG} = 18\text{ V}$		5	130	nA
$PSRR_{(OUT)}$	Power-supply rejection ratio of OUT rail	$I_{OUT} = 20\text{ mA}$	f = 10 Hz	85		dB
			f = 100 Hz	85		
			f = 1 kHz	90		
			f = 100 kHz	75		
$PSRR_{(MID\_OUT)}$	Power-supply rejection ratio of MID_OUT rail	$I_{MID\_OUT} = 20\text{ mA}$	f = 10 Hz	60		dB
			f = 100 Hz	55		dB
			f = 1 kHz	50		dB
			f = 100 kHz	50		dB
$V_n$	Output noise voltage	$BW = 10\text{ Hz to }100\text{ kHz}$ , $V_{OUT} = 1.2\text{ V}$		124		$\mu\text{V}_{RMS}$
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		170		$^\circ\text{C}$

- (1) Line regulation from Input of the LDO to the final output of the LDO.
- (2)  $V_{DO}$  is measured with  $V_{IN} = 0.97 \times V_{OUT(nom)}$  for fixed output voltage versions.  $V_{DO}$  is not measured for fixed output voltage versions when  $V_{OUT} \leq 2.5\text{ V}$ . For the adjustable output device,  $V_{DO}$  is measured with  $V_{FB} = 0.97 \times V_{FB(nom)}$ .

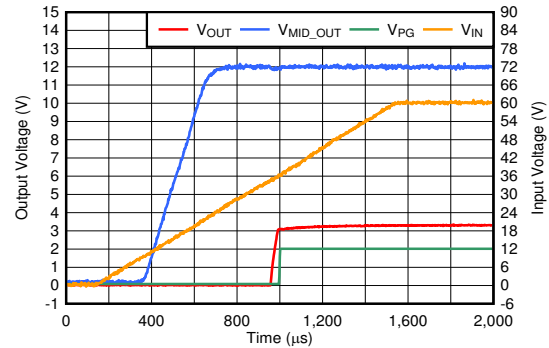
## 6.6 Typical Characteristics

at operating temperature  $T_J = 25^\circ\text{C}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $I_{MID\_OUT} = \text{open}$ ,  $V_{EN} = 2\text{ V}$ ,  $V_{MVSEL1} = 0.9\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{MID\_OUT} = 4.7\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ , and  $V_{IN} = V_{MID\_OUT} + 1.5\text{ V}$  (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$



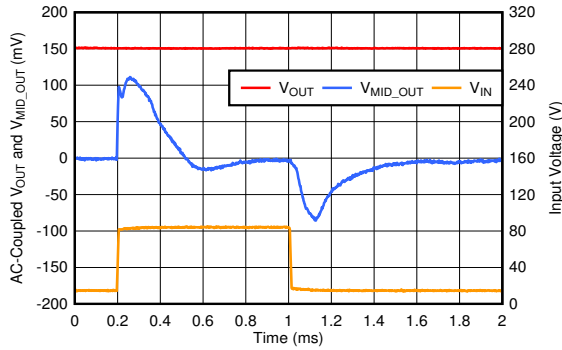
$V_{MVSEL1} = 0\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $V_{IN}$  ramp rate =  $10\text{ V}/\mu\text{s}$

**Figure 6-1. Fast Startup**



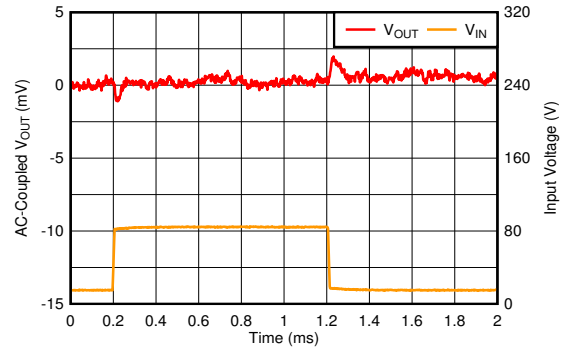
$V_{MVSEL1} = 0\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $V_{IN}$  ramp rate =  $45\text{ mV}/\mu\text{s}$

**Figure 6-2. Slow Startup**



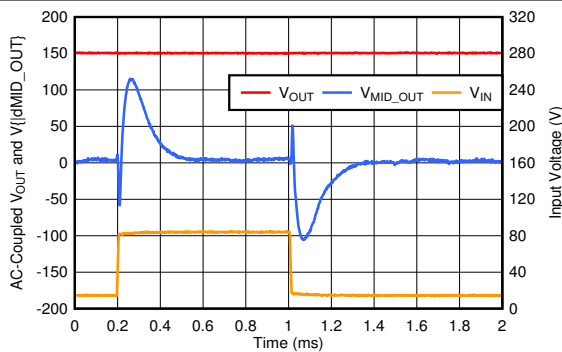
$V_{IN} = 15\text{ V to }85\text{ V}$ ,  $V_{IN}$  ramp rate =  $10\text{ V}/\mu\text{s}$ ,  $V_{MVSEL1} = 0\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $I_{MID\_OUT} = \text{open}$

**Figure 6-3. Line Transient**



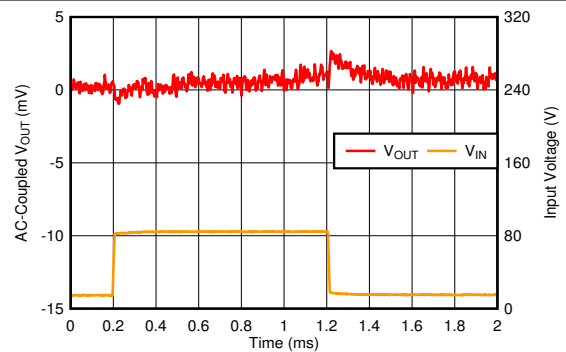
$V_{IN} = 15\text{ V to }85\text{ V}$ ,  $V_{IN}$  ramp rate =  $10\text{ V}/\mu\text{s}$ ,  $V_{MVSEL1} = 0\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $I_{MID\_OUT} = \text{open}$

**Figure 6-4. Line Transient (Zoom on  $V_{OUT}$ )**



$V_{IN} = 15\text{ V to }85\text{ V}$ ,  $V_{IN}$  ramp rate =  $10\text{ V}/\mu\text{s}$ ,  $V_{MVSEL1} = 0\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $I_{OUT} = I_{MID\_OUT} = 50\text{ mA}$

**Figure 6-5. Line Transient**



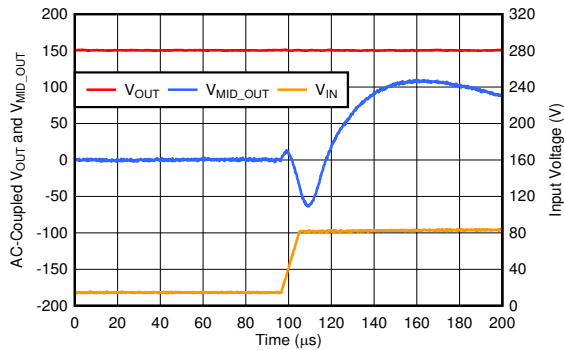
$V_{IN} = 15\text{ V to }85\text{ V}$ ,  $V_{IN}$  ramp rate =  $10\text{ V}/\mu\text{s}$ ,  $V_{MVSEL1} = 0\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $I_{OUT} = I_{MID\_OUT} = 50\text{ mA}$

**Figure 6-6. Line Transient (Zoom on  $V_{OUT}$ )**



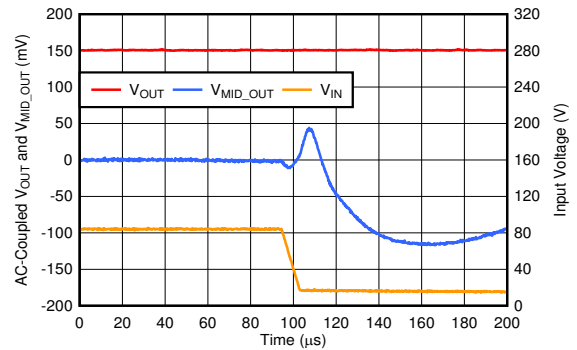
### 6.6 Typical Characteristics (continued)

at operating temperature  $T_J = 25^\circ\text{C}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $I_{MID\_OUT} = \text{open}$ ,  $V_{EN} = 2\text{ V}$ ,  $V_{MVSEL1} = 0.9\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{MID\_OUT} = 4.7\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ , and  $V_{IN} = V_{MID\_OUT} + 1.5\text{ V}$  (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$



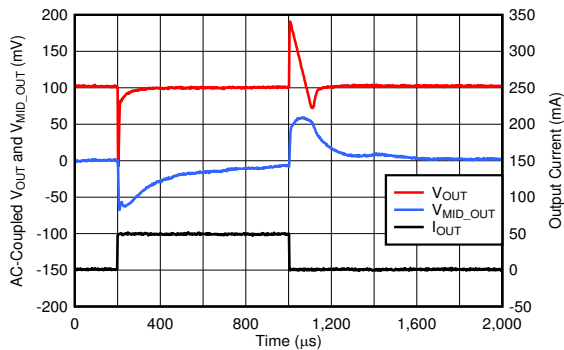
$V_{IN} = 15\text{ V to }85\text{ V}$ ,  $V_{IN}$  ramp rate =  $10\text{ V}/\mu\text{s}$ ,  $V_{MVSEL1} = 0\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $I_{OUT} = I_{MID\_OUT} = 50\text{ mA}$

**Figure 6-7. Line Transient  $V_{IN}$  Rising Edge**



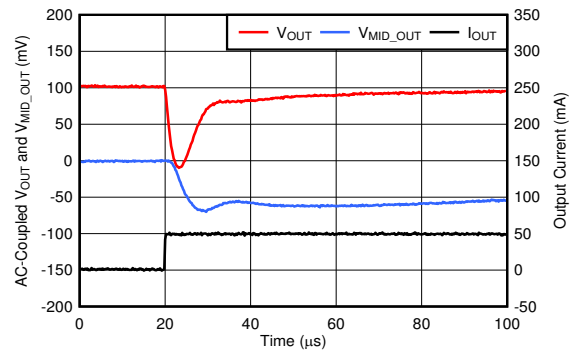
$V_{IN} = 15\text{ V to }85\text{ V}$ ,  $V_{IN}$  ramp rate =  $10\text{ V}/\mu\text{s}$ ,  $V_{MVSEL1} = 0\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $I_{OUT} = I_{MID\_OUT} = 50\text{ mA}$

**Figure 6-8. Line Transient  $V_{IN}$  Falling Edge**



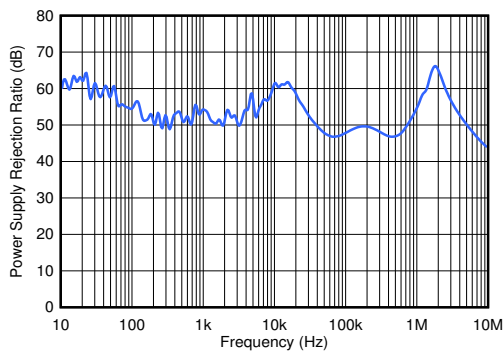
$V_{IN} = 50\text{ V}$ ,  $V_{MVSEL1} = 0\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $I_{MID\_OUT} = 1\text{ mA}$ ,  $I_{OUT}$  slew rate =  $1\text{ A}/\mu\text{s}$

**Figure 6-9. Load Transient**



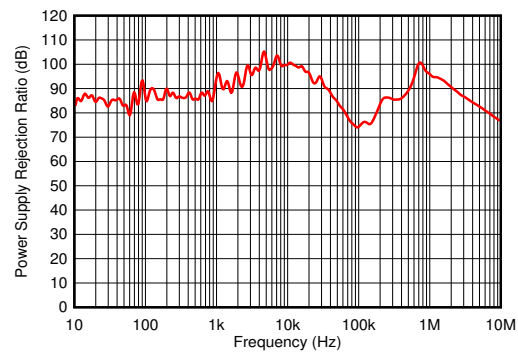
$V_{IN} = 50\text{ V}$ ,  $V_{MVSEL1} = 0\text{ V}$ ,  $V_{MVSEL2} = 0.9\text{ V}$ ,  $I_{MID\_OUT} = 1\text{ mA}$ ,  $I_{OUT}$  slew rate =  $1\text{ A}/\mu\text{s}$

**Figure 6-10. Load Transient,  $I_{OUT}$  Rising Edge**



$C_{IN} = \text{open}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $V_{MID\_OUT} = 12\text{ V}$ ,  $C_{MID\_OUT} = 3.3\text{ }\mu\text{F}$ ,  $I_{MID\_OUT} = 20\text{ mA}$ , and  $I_{OUT} = \text{open}$

**Figure 6-11.  $V_{MID\_OUT}$  PSRR vs Frequency**



$C_{IN} = \text{open}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $V_{MID\_OUT} = 12\text{ V}$ ,  $C_{MID\_OUT} = 3.3\text{ }\mu\text{F}$ ,  $I_{MID\_OUT} = \text{open}$ , and  $I_{OUT} = 20\text{ mA}$

**Figure 6-12.  $V_{OUT}$  PSRR vs Frequency**

## 7 Detailed Description

### 7.1 Overview

The TPS7A43 is an 85-V, low quiescent current, low-dropout (LDO) linear regulator. The low  $I_Q$  performance makes the device an excellent choice for battery-powered or line-power applications that are expected to meet increasingly stringent standby-power standards.

The device high accuracy over temperature and power-good indication make this device an excellent choice for meeting a wide range of microcontroller power requirements. The device features a selectable MID\_OUT voltage pin to provide a secondary voltage rail for various handheld power tool applications.

For increased reliability, the TPS7A43 also incorporates precision enable, output current limit, active discharge, and thermal shutdown protection. The operating junction temperature is  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and adds margin for applications concerned with higher working ambient temperatures.

### 7.2 Functional Block Diagrams

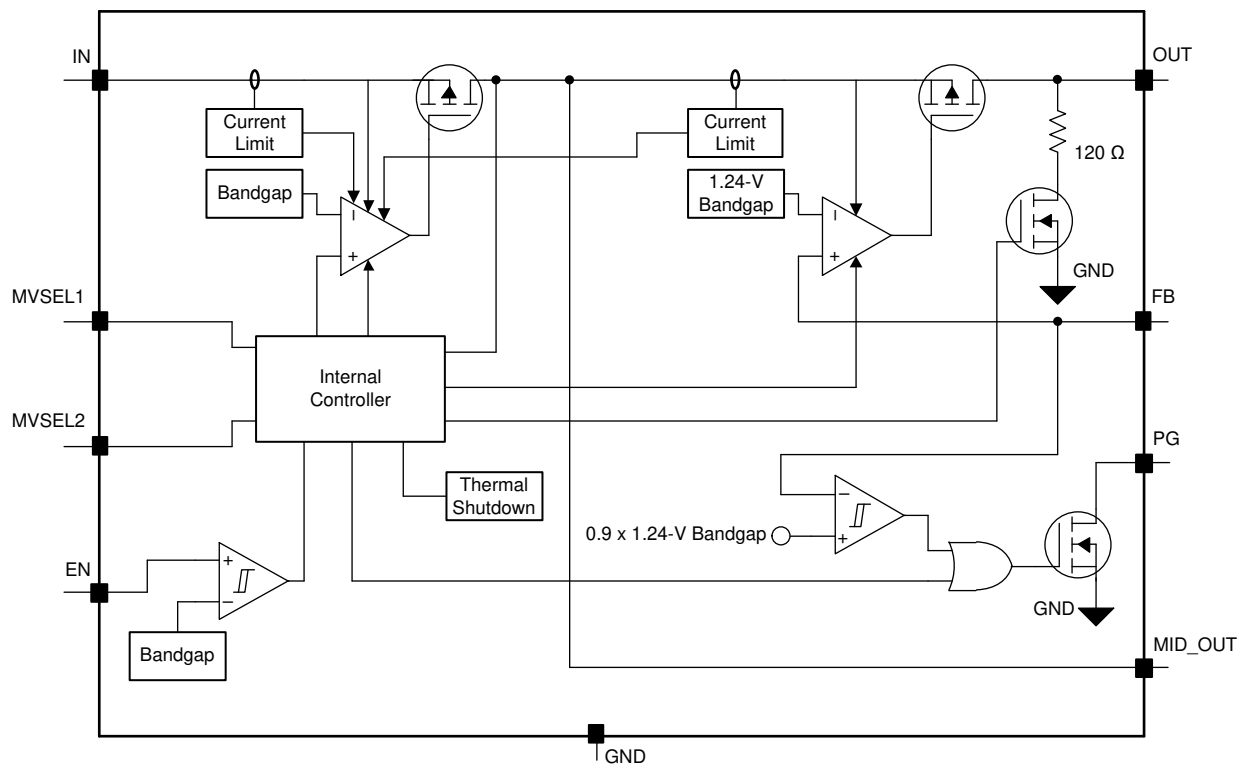


Figure 7-1. Adjustable Version

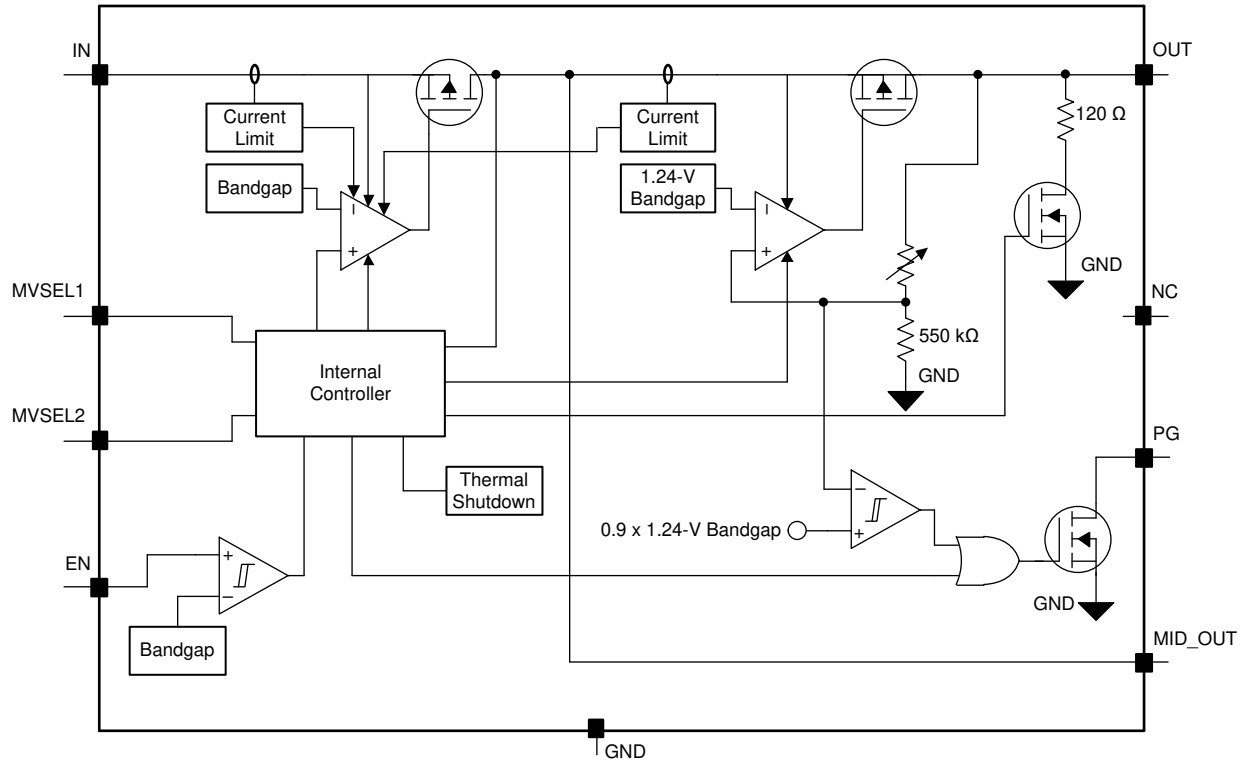


Figure 7-2. Fixed Version

## 7.3 Feature Description

### 7.3.1 MID\_OUT Voltage Selection

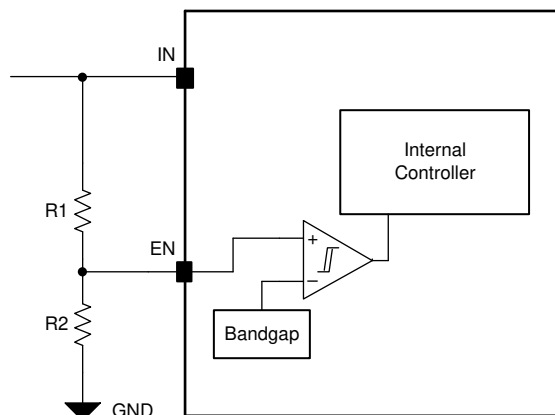
The TPS7A43 features a MID\_OUT voltage pin that provides a secondary output voltage supply in addition to the OUT pin, which is the main output voltage supply. The MID\_OUT voltage can be set using the MVSEL1 and MVSEL2 pins; see the [MID\\_OUT Voltage Setting](#) section for more details.

### 7.3.2 Precision Enable

The TPS7A43 features a precision enable circuit. The enable pin (EN) is active high; thus, enable the device by forcing the voltage of the enable pin to exceed the minimum EN pin high-level voltage (see the [Electrical Characteristics](#) table). Turn off the device by forcing the voltage of the enable pin to drop below the maximum EN pin low-level input voltage (see the [Electrical Characteristics](#) table). This device has an internal pullup resistor to the IN pin that enables the device when the EN pin is left floating.

If this pin is tied to the IN pin; the input voltage must not exceed 18 V; see the [Recommended Operating Conditions](#) table.

As shown in [Figure 7-3](#), an external resistor divider circuit can be used to enable the device using the input voltage.



**Figure 7-3. Enable the Device Using the Input Voltage**

The  $V_{EN(HI)}$  (maximum) threshold and the minimum input voltage to the application can be used to set the  $R_1$  to  $R_2$  resistor divider ratio. The values of the  $R_2$  and  $R_1$  resistors then can be calculated to minimize the leakage current through the divider.

### 7.3.3 Dropout Voltage

Dropout voltage ( $V_{DO}$ ) is defined as the input voltage minus the output voltage ( $V_{IN} - V_{OUT}$ ) at the rated output current ( $I_{RATED}$ ), where the pass transistor is fully on.  $I_{RATED}$  is the maximum  $I_{OUT}$  listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ( $R_{DS(ON)}$ ) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the  $R_{DS(ON)}$  of the device.

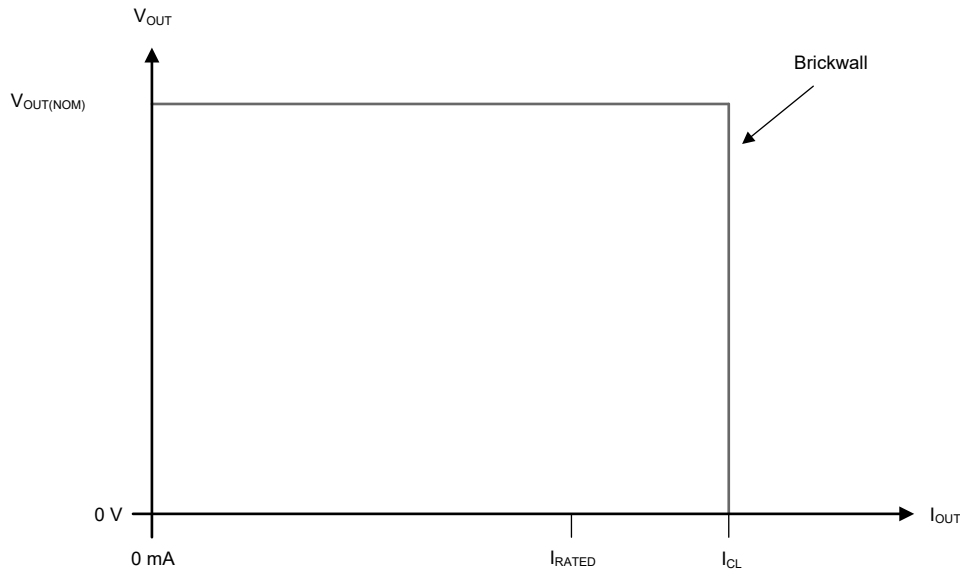
$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

### 7.3.4 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brickwall scheme. In a high-load current fault, the brickwall scheme limits the output current to the current limit ( $I_{CL}$ ).  $I_{CL}$  is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power  $[(V_{IN} - V_{OUT}) \times I_{CL}]$ . If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application report](#).

Figure 7-4 shows a diagram of the current limit.



**Figure 7-4. Current Limit**

### 7.3.5 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature ( $T_J$ ) of the pass transistor rises to  $T_{SD(shutdown)}$  (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to  $T_{SD(reset)}$  (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large  $V_{IN} - V_{OUT}$  voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

When the thermal limit is triggered with the load current near the value of the current limit, the output may oscillate prior to the output switching off.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

### 7.3.6 Power Good

The power-good (PG) pin is an open-drain output and can be connected to a regulated supply through an external pullup resistor. The maximum pullup voltage is listed as  $V_{PG}$  in the *Recommended Operating Conditions* table. For the PG pin to have a valid output, the voltage on the IN pin must be greater than  $V_{UVLO(RISING)}$ , as listed in the *Electrical Characteristics* table. When the  $V_{OUT}$  exceeds  $V_{IT(PG,RISING)}$ , the PG output is high impedance and the PG pin voltage pulls up to the connected regulated supply. When the regulated output falls below  $V_{IT(PG,FALLING)}$ , the open-drain output turns on and pulls the PG output low after a short deglitch time. If output voltage monitoring is not needed, the PG pin can be left floating or connected to ground.

The recommended maximum PG pin sink current ( $I_{PG-SINK}$ ) and the leakage current into the PG pin ( $I_{LKG(PG)}$ ) are listed in the *Electrical Characteristics* table.

The PG pullup voltage ( $V_{PG\_PULLUP}$ ), the desired minimum power-good output voltage ( $V_{PG(MIN)}$ ), and  $I_{LKG(PG)}$  limit the maximum PG pin pullup resistor value ( $R_{PG\_PULLUP}$ ).  $V_{PG\_PULLUP}$ , the PG pin low-level output voltage ( $V_{OL(PG)}$ ), and  $I_{PG-SINK}$  limit the minimum  $R_{PG\_PULLUP}$ . Maximum and minimum values for  $R_{PG\_PULLUP}$  can be calculated from the following equations:

$$R_{PG\_PULLUP(MAX)} = (V_{PG\_PULLUP} - V_{PG(MIN)}) / I_{LKG(PG)\_MAX} \quad (2)$$

$$R_{PG\_PULLUP(MIN)} = (V_{PG\_PULLUP} - V_{OL(PG)}) / I_{PG-SINK} \quad (3)$$

For example, if the PG pin is connected to a pullup resistor with a 3.3-V external supply, from the *Electrical Characteristics*,  $R_{PG\_PULLUP(MAX)}$  is 25 M $\Omega$ . From the *Electrical Characteristics* table,  $R_{PG\_PULLUP(MIN)}$  is 6.6 k $\Omega$ .

## 7.4 Device Functional Modes

### 7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**Table 7-1. Device Functional Mode Comparison**

OPERATING MODE	PARAMETER			
	$V_{IN}$	$V_{EN}$	$I_{OUT}$	$T_J$
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

### 7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ( $V_{OUT(nom)} + V_{DO}$ )
- The output current is less than the current limit ( $I_{OUT} < I_{CL}$ )
- The device junction temperature is less than the thermal shutdown temperature ( $T_J < T_{SD}$ )
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout,  $V_{IN} < V_{OUT(NOM)} + V_{DO}$ , directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ( $V_{OUT(NOM)} + V_{DO}$ ), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

### 7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off and internal circuits are shutdown.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 MID\_OUT Voltage Setting

The MID\_OUT voltage has three different output voltage levels (10 V, 12 V, and 15 V), as listed in [Table 8-1](#), depending on the MVSEL1 and MVSEL2 pins voltage settings.

**Table 8-1. MID\_OUT Voltage Setting**

SET $V_{MVSEL1}$	SET $V_{MVSEL2}$	MID_OUT
$0.9\text{ V} \leq V_{MVSEL1} \leq 17\text{ V}$	$0\text{ V} \leq V_{MVSEL2} \leq 0.4\text{ V}$	10 V
$0\text{ V} \leq V_{MVSEL1} \leq 17\text{ V}$	$0.9\text{ V} \leq V_{MVSEL2} \leq 17\text{ V}$	12 V
$0\text{ V} \leq V_{MVSEL1} \leq 0.4\text{ V}$	$0\text{ V} \leq V_{MVSEL2} \leq 0.4\text{ V}$	15 V

For adjustable voltage options of the TPS7A43, and to maintain voltage regulation on the MID\_OUT and OUT pins, the input voltage must be kept  $\geq \text{MID\_OUT} + V_{DO(\text{MID\_OUT})}$ . Additionally, to maintain regulation on the OUT pin, the MID\_OUT voltage must be set  $\geq V_{OUT(\text{nom})} + V_{DO(\text{OUT})}$ .

TI recommends setting the MVSEL1 and MVSEL2 voltages for both the fixed and adjustable voltage options before enabling the device to set the MID\_OUT voltage level; however, the MID\_OUT voltage setting can be changed to a different level after the device had powered up.

#### 8.1.2 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage.  $V_{OUT}$  is set using the feedback divider resistors,  $R_1$  and  $R_2$ , according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (4)$$

To ignore the FB pin current error term in the  $V_{OUT}$  equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (5)$$

#### 8.1.3 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.



### 8.1.4 Input and Output Capacitor Requirements

An input capacitor is not required for stability except when the device maximum current is sourced from the MID\_OUT pin. However, adding an input capacitor is always good analog design practice to counteract reactive input sources and improve transient response, input ripple, and PSRR. Starting with the nominal input capacitor value is required if large, fast transient load or line transients are anticipated on the MID\_OUT pin or if the device is located several inches from the input power source.

A minimum of a 3:1 capacitor ratio between  $C_{MID\_OUT}$  and  $C_{OUT}$  is required for proper operation of the TPS7A43 LDO and TI recommends 4.7- $\mu$ F capacitor to be connected from the MID\_OUT pin to GND.

A minimum 1- $\mu$ F output capacitor is required for  $V_{OUT}$  stability. A maximum 100- $\mu$ F output capacitor can be used as long as the 3:1 ratio between  $C_{MID\_OUT}$  and  $C_{OUT}$  is maintained.

### 8.1.5 Power Dissipation ( $P_D$ )

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation ( $P_D$ ).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

#### Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ( $T_A$ ) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) of the combined PCB and device package and the temperature of the ambient air ( $T_A$ ).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (7)$$

Thermal resistance ( $R_{\theta JA}$ ) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

### 8.1.6 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi ( $\Psi$ ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter ( $\psi_{JT}$ ) and junction-to-board characterization parameter ( $\psi_{JB}$ ). These parameters provide two methods for calculating the junction temperature ( $T_J$ ), as described in the following equations. Use the junction-to-top characterization parameter ( $\psi_{JT}$ ) with the temperature at the center-top of device package ( $T_T$ ) to calculate the junction temperature. Use the junction-to-board characterization parameter ( $\psi_{JB}$ ) with the PCB surface temperature 1 mm from the device package ( $T_B$ ) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (8)$$

where:

- $P_D$  is the dissipated power
- $T_T$  is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (9)$$

where

- $T_B$  is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 8.2 Typical Application

This section discusses the implementation of the TPS7A43 in cordless power tools application. [Figure 8-1](#) shows a typical circuit diagram for this application.

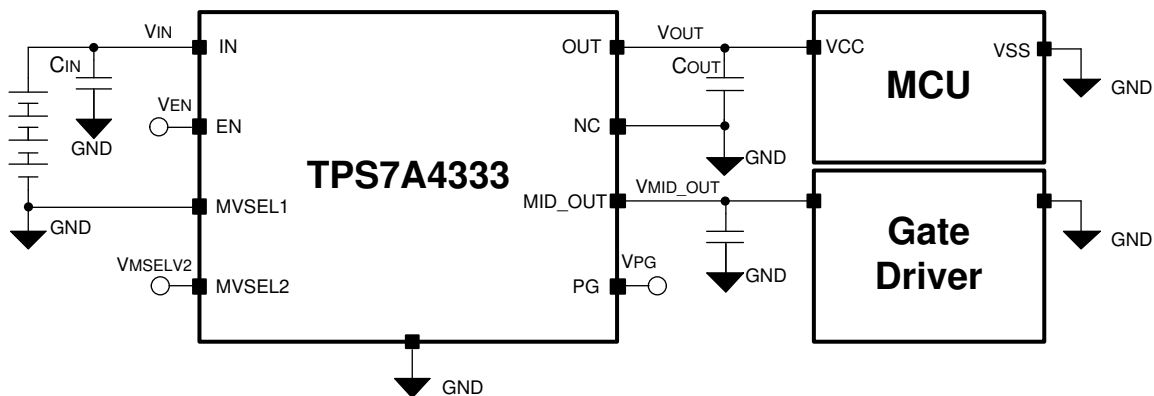


Figure 8-1. Powering Cordless Power Tools

### 8.2.1 Design Requirements

[Table 8-2](#) summarizes the design requirements for [Figure 8-1](#).

Table 8-2. Design Parameters

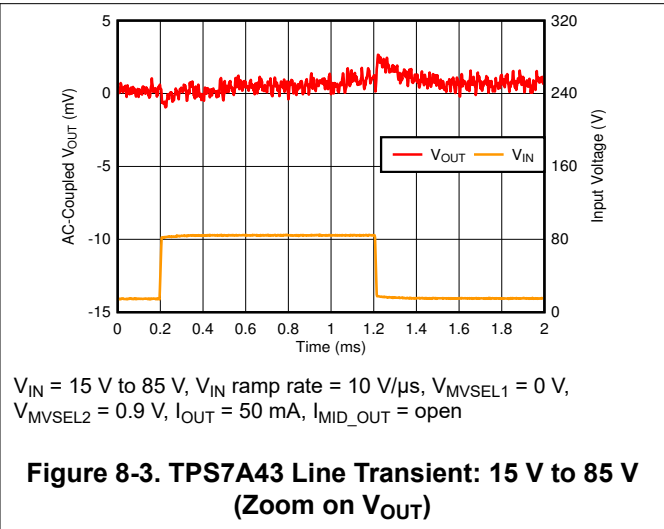
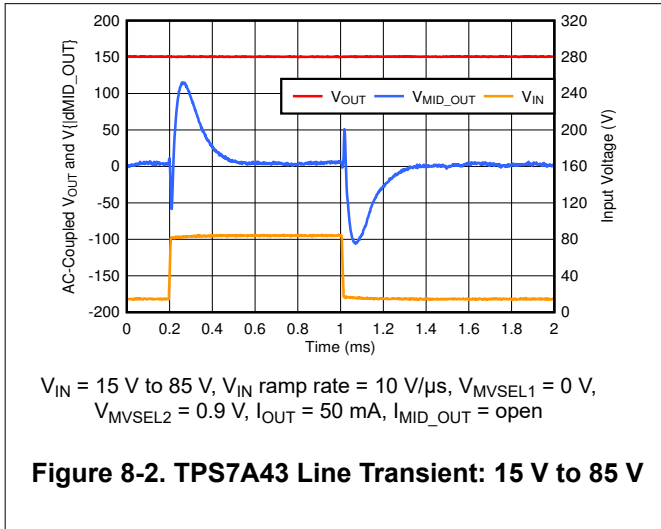
PARAMETER	DESIGN VALUES
$V_{IN}$	15 V (min), 85 V (transient max)
$V_{OUT}$	3.3 V $\pm$ 2 %
$V_{MID\_OUT}$	12 V $\pm$ 5 %
$I_{(IN)}$ (no load)	< 9 $\mu$ A
$I_{OUT}$ (typical), (max)	20 mA, 50 mA
$I_{MID\_OUT}$ (typical), (max)	open, 1 mA
$T_A$	60 °C (max)

### 8.2.2 Detailed Design Procedure

A 3.3-V fixed output voltage device is selected for this application and the MVSEL1 pin is tied to GND to simplify this design. The gate driver circuit is driven using the  $V_{MID\_OUT}$  voltage by setting the MVSEL1 and MVSEL2 pins by means of the MCU and GND reference.

The input and output capacitors are selected in accordance with the *Recommended Operating Conditions* table.

### 8.2.3 Application Curves



## 9 Power Supply Recommendations

The device is designed to operate from an input supply voltage range of 4 V to 85 V. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least  $V_{MID\_OUT(nom)} + 1.5\text{ V}$ . Connect a low output impedance power supply directly to the input pin of the TPS7A43.

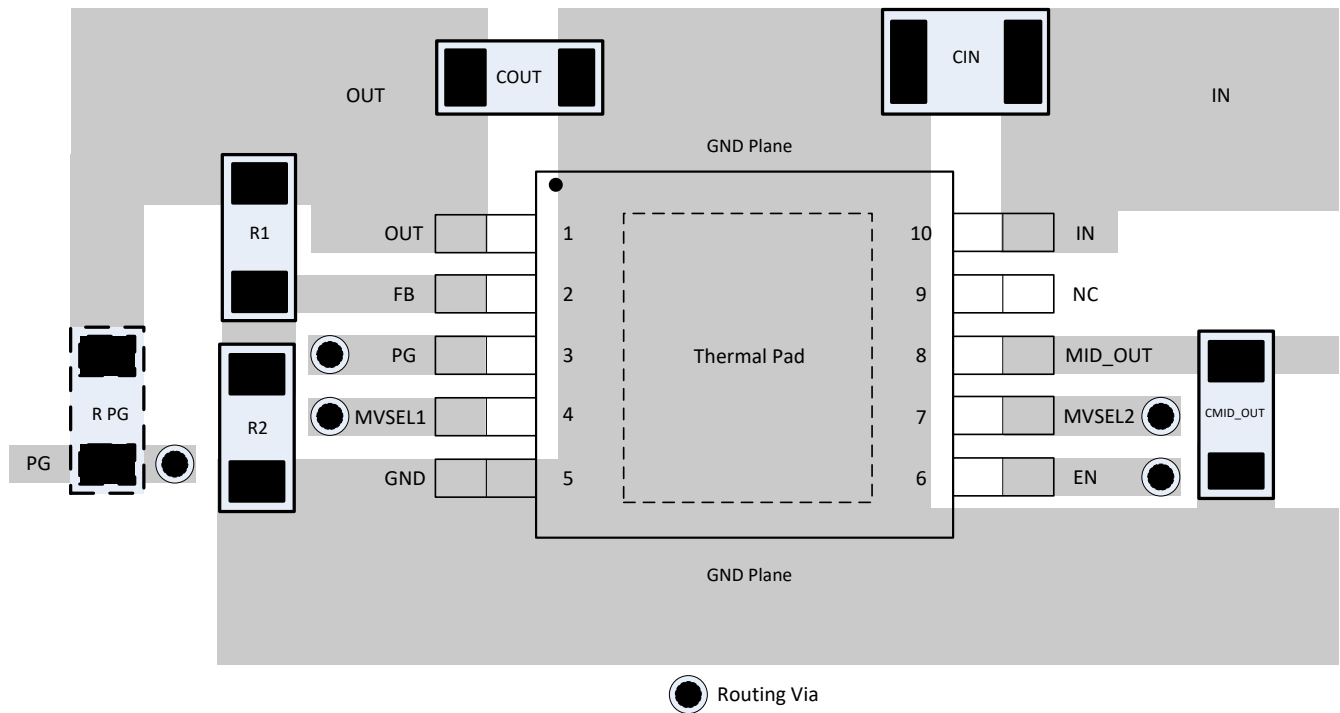
## 10 Layout

### 10.1 Layout Guidelines

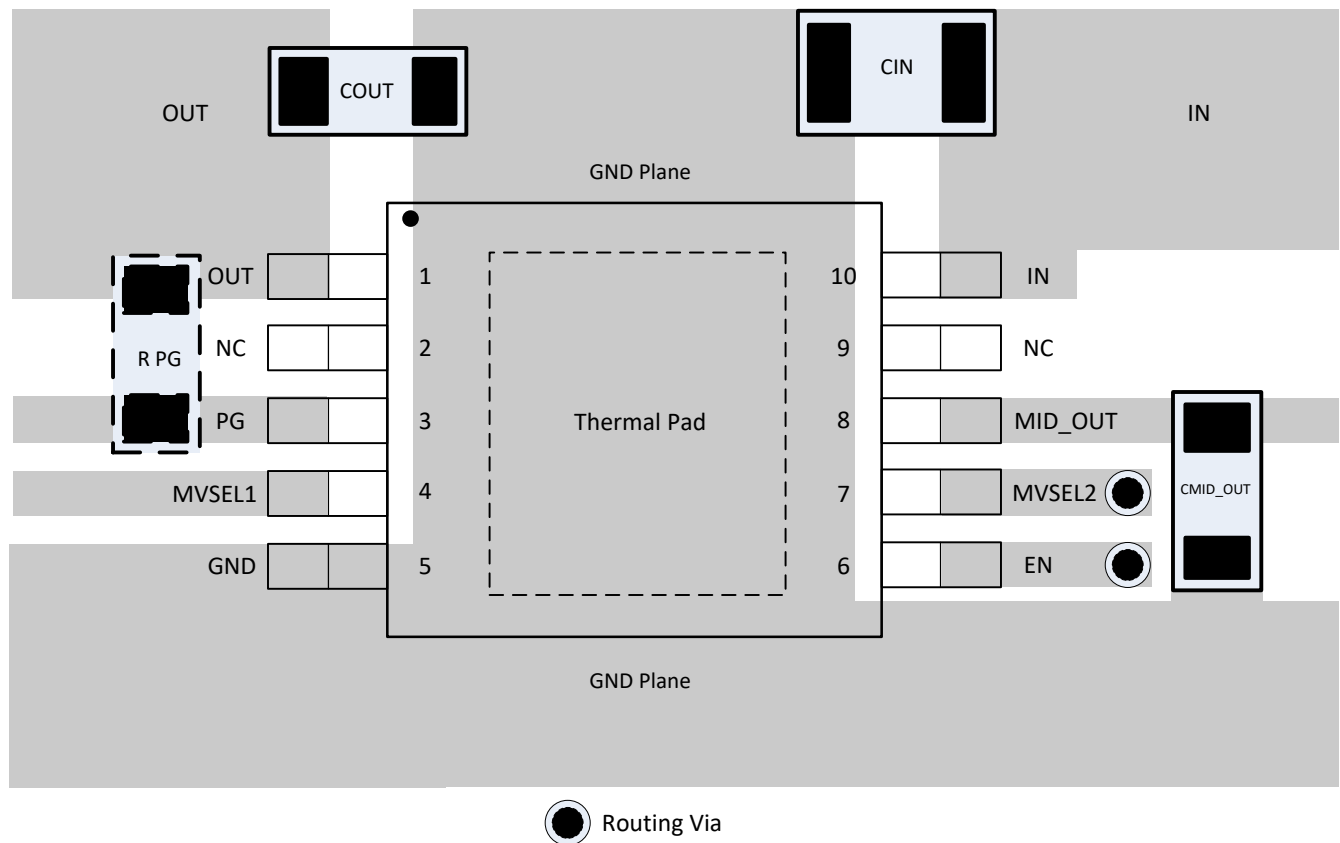
- Place input and output capacitors as close to the device pins as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device and under the thermal pad to distribute heat.
- Only place tented thermal vias directly beneath the thermal pad of the DGQ package. An untented via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

## 10.2 Layout Examples

ADVANCE INFORMATION



**Figure 10-1. Adjustable Version Layout Example**



**Figure 10-2. Fixed Version Layout Example**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Device Nomenclature

**Table 11-1. Device Nomenclature (1)**

PRODUCT	V <sub>OUT</sub>
TPS7A43xx(x) yyy z	<p><b>xx(x)</b> is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; for output voltages with a resolution of 50 mV, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). 01 indicates adjustable output version.</p> <p><b>yyy</b> is the package designator.</p> <p><b>z</b> is the package quantity. R is for large quantity reel, T is for small quantity reel.</p>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.




### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7A4301DGQR	ACTIVE	HVSSOP	DGQ	10	2500	TBD	Call TI	Call TI	-40 to 125		
PTPS7A4333DGQR	ACTIVE	HVSSOP	DGQ	10	2500	TBD	Call TI	Call TI	-40 to 125		
PTPS7A4350DGQR	ACTIVE	HVSSOP	DGQ	10	2500	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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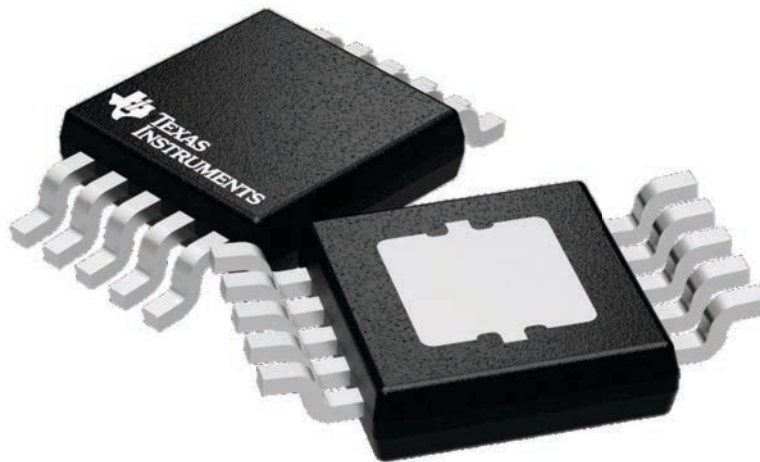
## GENERIC PACKAGE VIEW

**DGQ 10**

**PowerPAD™ HVSSOP - 1.1 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

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