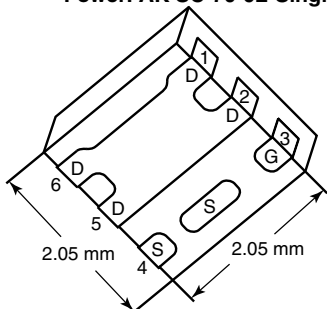


P-Channel 12 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) (Max.)	I _D (A) ^a	Q _g (Typ.)
- 12	0.0130 at V _{GS} = - 4.5 V	- 31	29 nC
	0.0145 at V _{GS} = - 3.7 V	- 30	
	0.0195 at V _{GS} = - 2.5 V	- 26	
	0.0400 at V _{GS} = - 1.8 V	- 7	

PowerPAK SC-70-6L-Single



Ordering Information:
SiA467EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

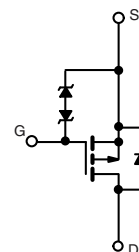
- TrenchFET® Power MOSFET
- Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_g and UIS Tested
- Typ ESD Protection: 5000 V (HBM)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

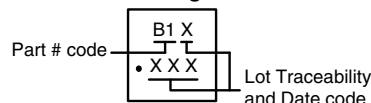
APPLICATIONS

- Portable Devices such as Smart Phones, Tablet PCs and Mobile Computing
 - Battery Switch
 - Load Switch
 - Power Management



P-Channel MOSFET

Marking Code



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 12	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 31
		T _C = 70 °C	- 25
		T _A = 25 °C	- 13 ^{b, c}
		T _A = 70 °C	- 11 ^{b, c}
Pulsed Drain Current (t = 300 μs)	I _{DM}	- 60	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	- 2.9 ^{b, c}
Single Avalanche Current	I _{AS}	- 11	mJ
Single Avalanche Energy	E _{AS}	5.8	
Maximum Power Dissipation	P _D	T _C = 25 °C	19
		T _C = 70 °C	12
		T _A = 25 °C	3.5 ^{b, c}
		T _A = 70 °C	2.2 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 50 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	28	36	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	5.3	6.5	

Notes

- T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 12			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 6.4		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			2.4		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.4		- 1	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 2	μA
		V _{DS} = 0 V, V _{GS} = ± 4.5 V			± 0.5	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 12 V, V _{GS} = 0 V			- 1	
		V _{DS} = - 12 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	- 10			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 5 A		0.0105	0.0130	Ω
		V _{GS} = - 3.7 V, I _D = - 5 A		0.0120	0.0145	
		V _{GS} = - 2.5 V, I _D = - 4 A		0.0155	0.0195	
		V _{GS} = - 1.8 V, I _D = - 2 A		0.0260	0.0400	
Forward Transconductance ^a	g _{fs}	V _{GS} = - 6 V, I _D = - 5 A		31		S
Dynamic^b						
Input Capacitance	C _{iss}	V _{DS} = - 6 V, V _{GS} = 0 V, f = 1 MHz		2520		pF
Output Capacitance	C _{oss}			570		
Reverse Transfer Capacitance	C _{rss}			545		
Total Gate Charge	Q _g	V _{DS} = - 6 V, V _{GS} = - 8 V, I _D = - 14 A		48	72	nC
				29	44	
Gate-Source Charge	Q _{gs}	V _{DS} = - 6 V, V _{GS} = - 4.5 V, I _D = - 14 A		4		
Gate-Drain Charge	Q _{gd}			6.6		
Gate Resistance	R _g	f = 1 MHz	1.8	9	18	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 6 V, R _L = 0.6 Ω I _D ≅ - 10 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		25	50	ns
Rise Time	t _r			25	50	
Turn-Off Delay Time	t _{d(off)}			90	180	
Fall Time	t _f			50	100	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 6 V, R _L = 0.6 Ω I _D ≅ - 10 A, V _{GEN} = - 8 V, R _g = 1 Ω		10	20	
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			120	240	
Fall Time	t _f			45	90	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 16	A
Pulse Diode Forward Current	I _{SM}				- 60	
Body Diode Voltage	V _{SD}	I _S = - 10 A, V _{GS} = 0 V		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 10 A, di/dt = 100 A/μs, T _J = 25 °C		20	40	ns
Body Diode Reverse Recovery Charge	Q _{rr}			7	15	nC
Reverse Recovery Fall Time	t _a			9		ns
Reverse Recovery Rise Time	t _b			11		

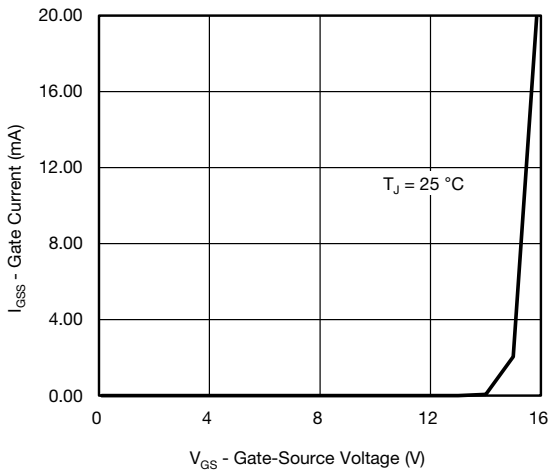
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
 b. Guaranteed by design, not subject to production testing.

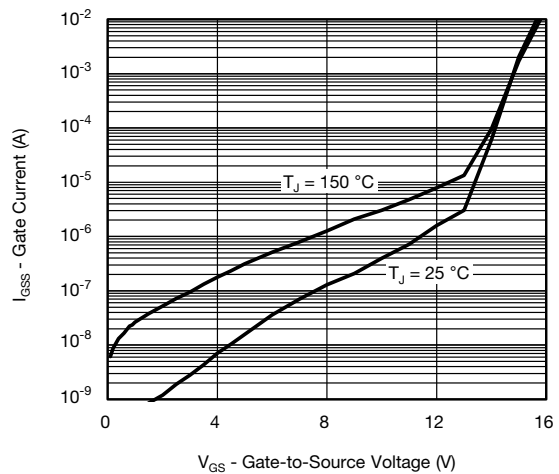
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



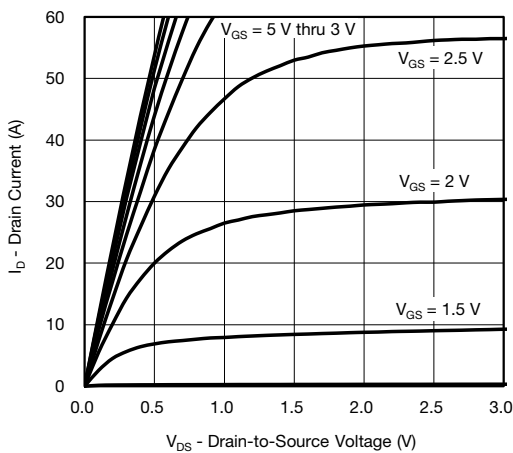
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



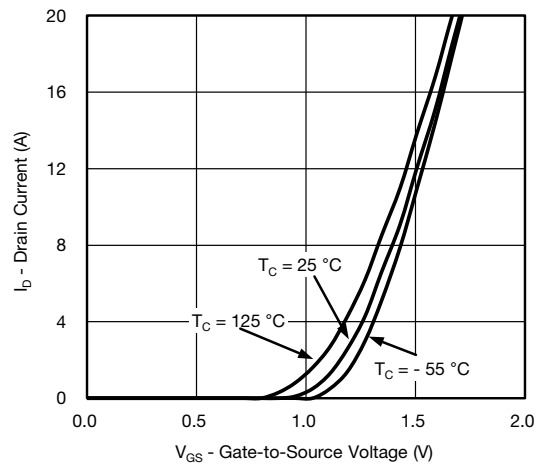
Gate Current vs. Gate-Source Voltage



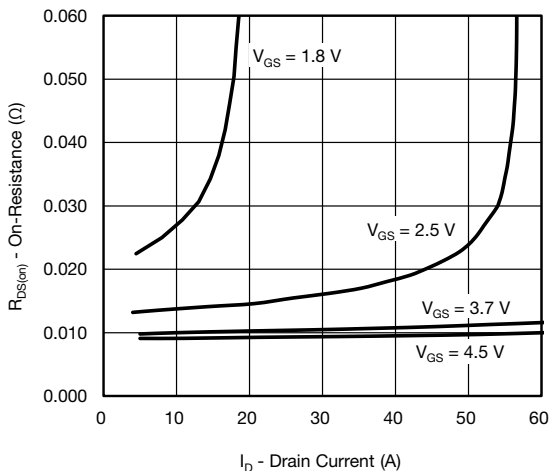
Gate Current vs. Gate-to-Source Voltage



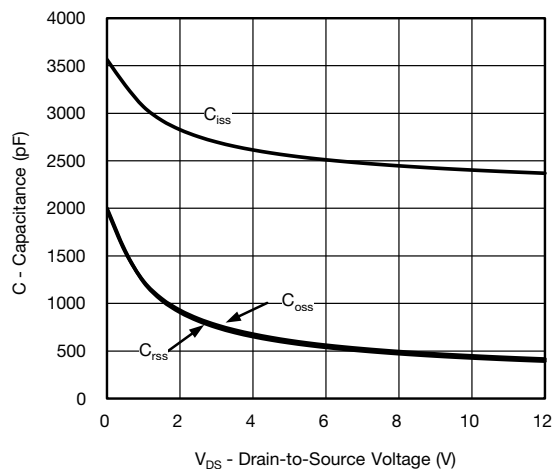
Output Characteristics



Transfer Characteristics



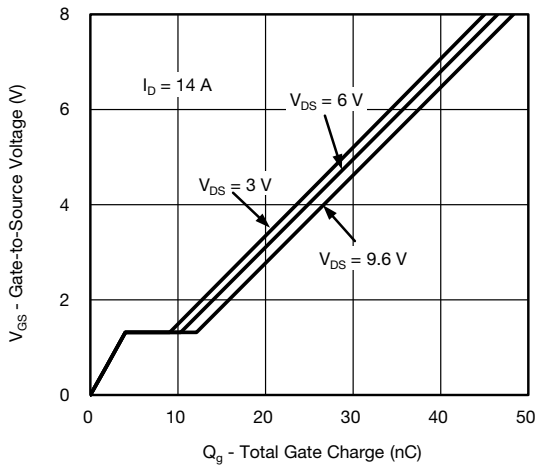
On-Resistance vs. Drain Current and Gate Voltage



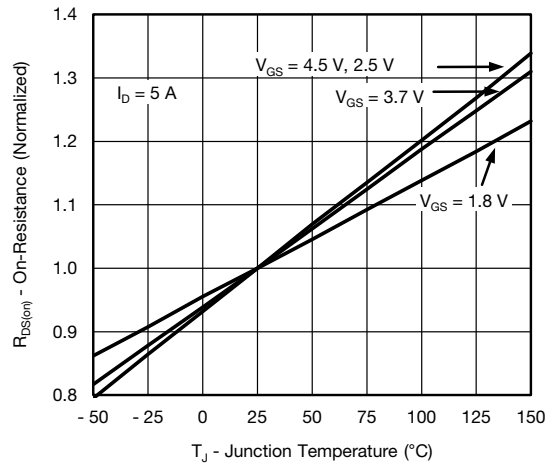
Capacitance



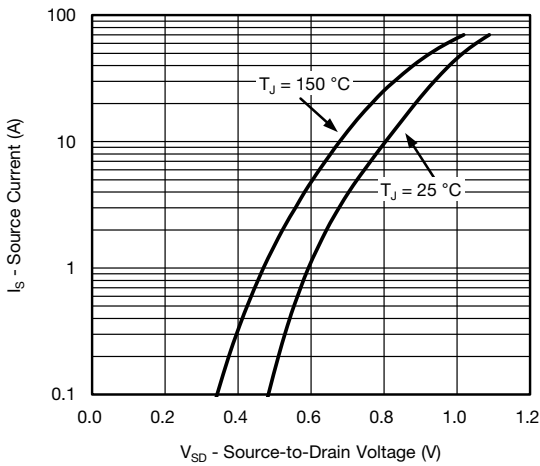
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



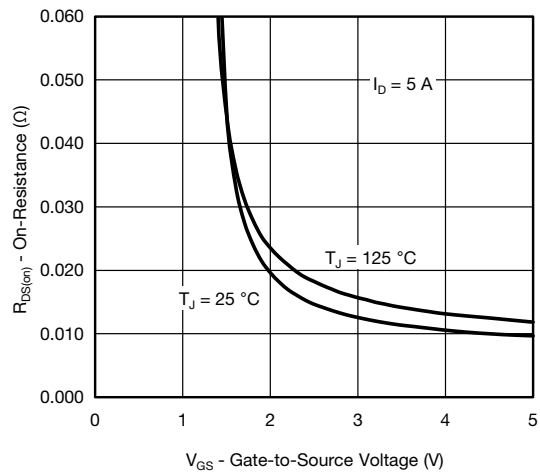
Gate Charge



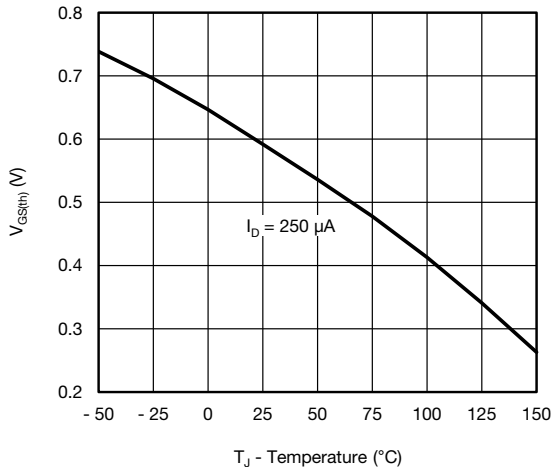
On-Resistance vs. Junction Temperature



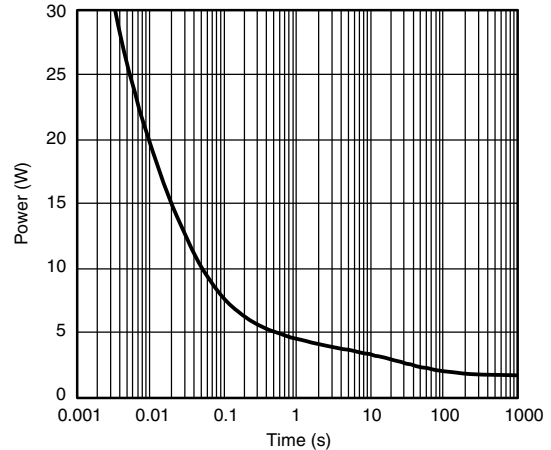
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



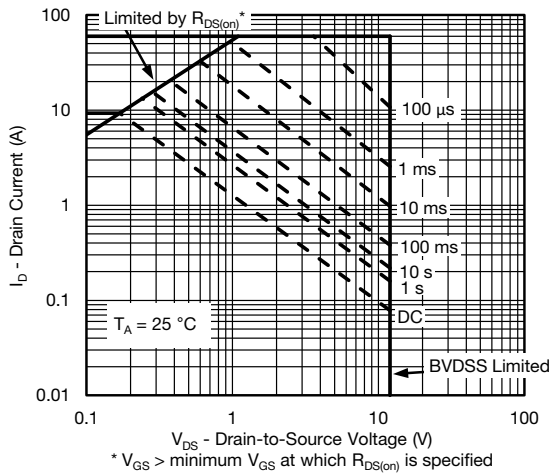
Threshold Voltage



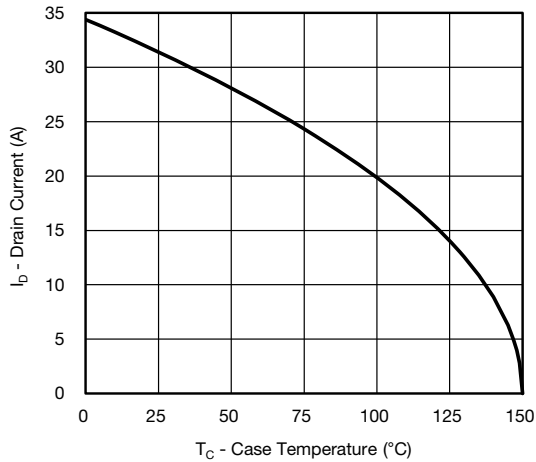
Single Pulse Power, Junction-to-Ambient



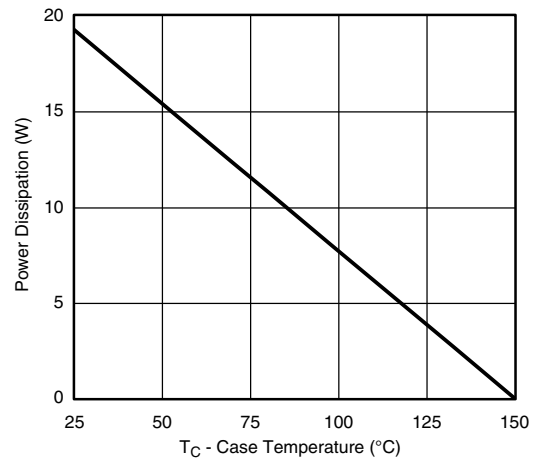
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating*

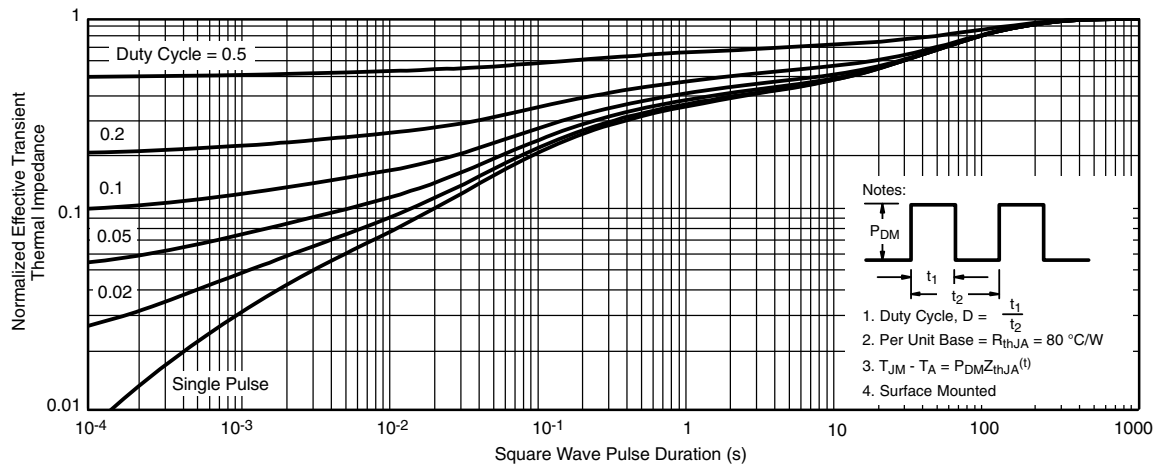


Power Derating

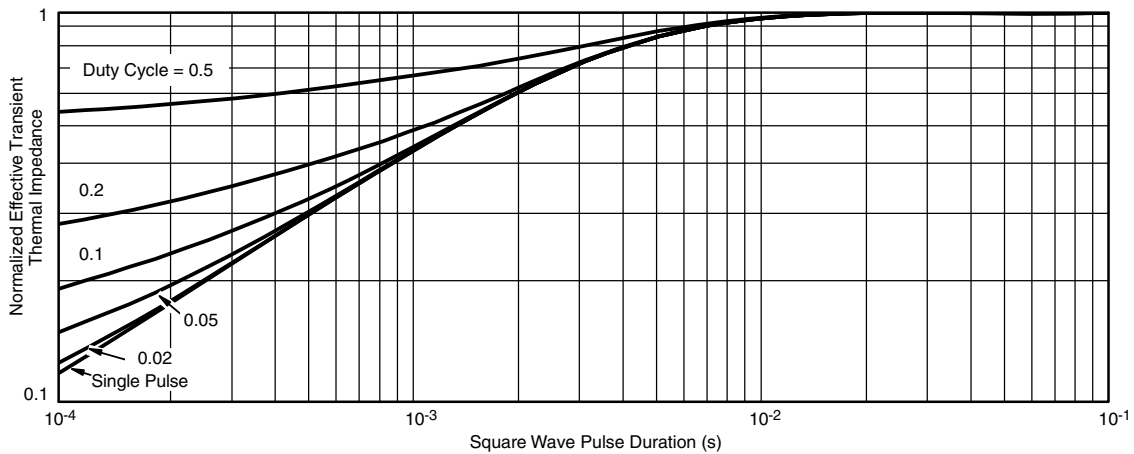
* The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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