ISOFACE™

ISO1I811T

Isolated 8 Channel Digital Input with IEC61131-2 Type 1/2/3 Characteristics

Data Sheet

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ISO1I811T

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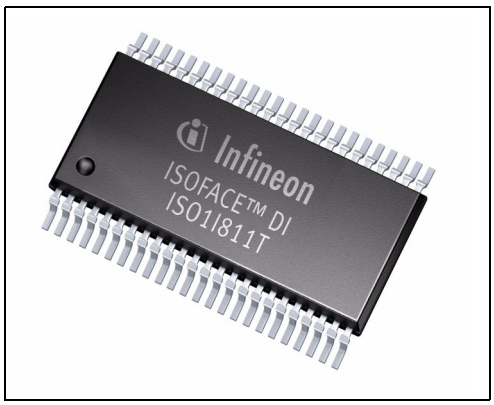
Previous Version: Preliminary Data Sheet V1.0

Page	Subjects (major changes since last revision)
V2.0	Data Sheet
Page 25	Parallel Interface timing table updated
Page 26	Serial Interface timing table updated

Isolated 8 Channel Digital Input with IEC61131-2 Type 1/2/3 Characteristics



Product Highlights

- **Minimization of power dissipation due to constant current characteristic**
- **Status LED output for each input**
- **Digital averaging of the input signals to suppress interference pulses**
- **Isolation between Input and Output using Coreless Transformer Technology**

Features

- Complete system integration (up to eight digital sensor or switch inputs, galvanic isolation and intelligent micro-controller or bus-ASIC interface)
- 8-channel input according to IEC61131-2 (Type 1/2/3)
- Integrated galvanic isolation 500VAC (EN60664-1, UL1577)
- 3.3/5V SPI and parallel micro-controller interface
- Adjustable deglitching filters
- Up to 125 kHz sampling frequency
- V_{BB} under-voltage detection
- Package: TSSOP-48, 8 mm x 12.5 mm

Typical Application

Programmable Logic Controllers(PLC)

Industrial PC

General Control Equipment

Description

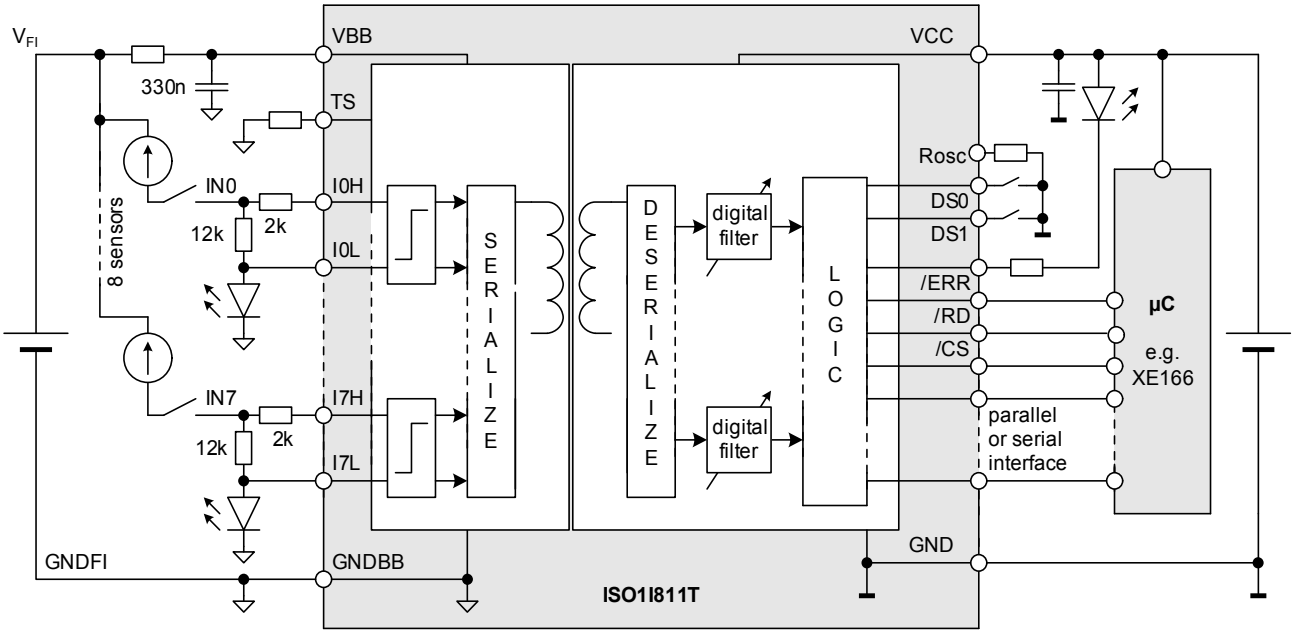
The ISO1I811T is an electrically isolated 8 bit data input interface in TSSOP-48 package.

This part is used to detect the signal states of eight independent input lines according to IEC61131-2 Type 1/2/3 (e.g. two-wire proximity switches) with a common ground (GNDFI).

For operation in accordance with IEC61131-2, it is necessary for the ISO1I811T to be wired with resistors according to the application diagram.

The 8 bit parallel/serial µC compatible interface allows the IC to directly connect to a µC system. The µC interface also supports a direct control mode and is designed to operate with 3.3/5V CMOS compatible levels.

The data transfer and isolation from input to output side is realized by the integrated Coreless Transformer Technology.



1 Pin Configuration and Functionality

The pin configuration slightly differs for the parallel or the serial interface.

1.1 Pin Configuration

The ordering, type and functions of the IC pins are listed in the **Table 1**.

Table 1 Pin Configuration

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl 1)	Type 2)	Function	Symbol	Ctrl.	Type	Function
1	GND		A	Logic Ground	GND			
2	SEL	I	PU	Serial Parallel Mode Select	SEL			
3	n.c.			not connected	n.c.			
4	ROSC		A	Clock Frequency Adjustment	ROSC			
5	VCC		A	Positive 5/3.3V logic supply	VCC			
6	$\overline{\text{ERR}}$	O	OD, PU	Error output	$\overline{\text{ERR}}$			
7	GND		A	Logic Ground	GND			
8	D0	O	PPZ	Data output bit0	SDI	I	PD	SPI Data input
9	D1	O	PPZ	Data output bit1	GND			
10	D2	O	PPZ	Data output bit2	GND			
11	D3	O	PPZ	Data output bit3	GND			
12	D4	O	PPZ	Data output bit4	GND			
13	D5	O	PPZ	Data output bit5	SCLK	I	PD	SPI Shift Clock input
14	D6	O	PPZ	Data output bit6	GND			
15	D7	O	PPZ	Data output bit7	SDO	O	PPZ	SPI Data output
16	$\overline{\text{CS}}$	I	PU	Chip Select	$\overline{\text{CS}}$			
17	$\overline{\text{RD}}$	I	PU	Data Read Input	n.c.			not connected
18	GND		A	Logic Ground	GND			
19	DS0	I	PD	Filter Select Input 0	DS0			
20	DS1	I	PD	Filter Select Input 1	DS1			
21	GND		A	Logic Ground	GND			
22	n.c.			not connected	n.c.			
23	n.c.			not connected	n.c.			
24	GND		A	Logic Ground	GND			
25	GNDBB		A	Input Ground	GNDBB			
26	VBB		A	Positive input supply voltage	VBB			
27	I0L		A	Input 0 Low, LED Out	I0L			
28	I0H		A	Input 0 High	I0H			
29	I1L		A	Input 1 Low, LED Out	I1L			
30	I1H		A	Input 1 High	I1H			
31	GNDBB		A	Input Ground	GNDBB			
32	I2L		A	Input 2 Low, LED Out	I2L			

Table 1 Pin Configuration

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl [1]	Type [2]	Function	Symbol	Ctrl.	Type	Function
33	I2H		A	Input 2 High	I2H			
34	I3L		A	Input 3 Low, LED Out	I3L			
35	I3H		A	Input 3 High	I3H			
36	TS		A	Sensor Type 1/2/3 Select	TS			
37	GNDBB		A	Input Ground	GNDBB			
38	n.c.			not connected	n.c.			
39	I4L		A	Input 4 Low, LED Out	I4L			
40	I4H		A	Input 4 High	I4H			
41	I5L		A	Input 5 Low, LED Out	I5L			
42	I5H		A	Input 5 High	I5H			
33	GNDBB		A	Input Ground	GNDBB			
44	I6L		A	Input 6 Low, LED Out	I6L			
45	I6H		A	Input 6 High	I6H			
46	I7L		A	Input 7 Low, LED Out	I7L			
47	I7H		A	Input 7 High	I7H			
48	GNDBB		A	Input Ground	GNDBB			

1) Direction of the pin: I = input, O = output, IO = Input/Output

2) Type of the pin: A = analog, OD = Open-Drain, PU = internal Pull-Up resistor, PD = internal Pull-Down resistor, PPZ = Push-Pull pin with High-Impedance functionality

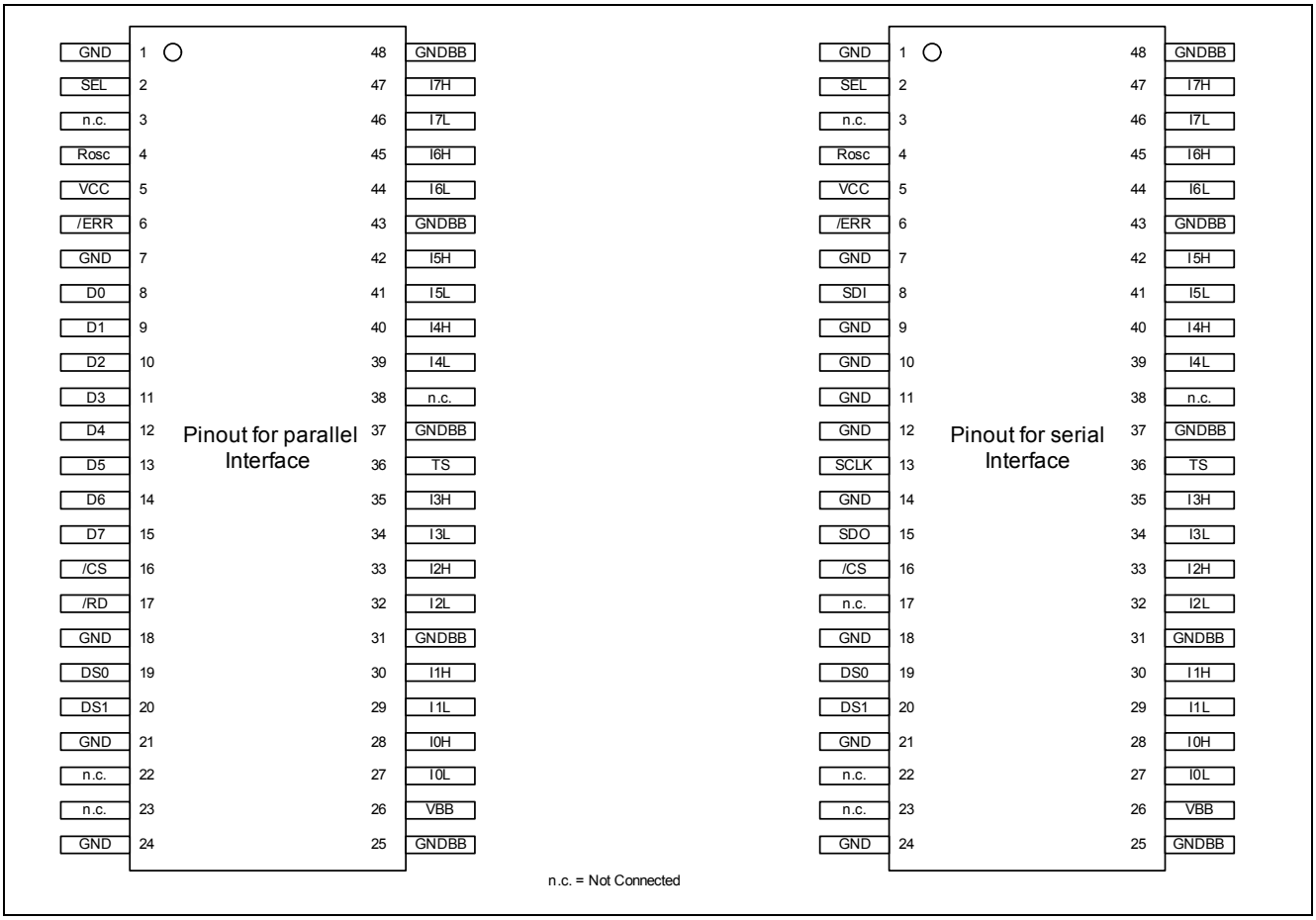


Figure 1 TSSOP-48 Pinout for Parallel and Serial Interface

1.2 Pin Functionality

The meaning and the functions of the IC pins are described below.

1.2.1 Pins of Sensor Interface

VBB (Positive supply 9.6-35V sensor supply)

VBB supplies the sensor input stage.

GNDBB (Ground for VBB domain)

This pin acts as the ground reference for the sensor input stage, that is supplied by VBB.

I0H... I7H (Input channel 0 ... 7)

Sensor inputs with current sink characteristic according IEC61131-2 Type 1/2/3 which has been selected by pin TS

I0L... I7L (LED output channel 0 ... 7)

This pin provides the output signal to switch on the LED if the input voltage and current has been detected as “High” according the selected type.

TS (Type Select)

By connecting a resistor between TS and GNDBB the sensor type (Type 1/2/3) can be selected (refer to **Table 9** for corresponding resistor value). This pin is for static configuration (pin-strapping). The voltage level at pin TS is not allowed to be changed during operation.

1.2.2 Pins of Serial and Parallel logic Interface

Some pins are common for both interface types, some others are specific for the parallel or serial access.

VCC (Positive 3.3 / 5V logic supply)

VCC supplies the output interface that is electrically isolated from the sensor input stage. The interface can be supplied with 3.3 / 5V.

GND (Ground for VCC domain)

This pin is the ground reference for the uC-interface that is supplied by VCC.

ROSC (Clock Adjustment)

A high precision resistor has to be connected between ROSC and GND to guarantee the frequency accuracy of the sampling clock. For details see **Chapter 3.3**.

$\overline{\text{ERR}}$ (Error Output)

The low active $\overline{\text{ERR}}$ signal contains the OR-wired information of the sensor input missing voltage (MV) detection and the internal data transmission failure detection unit. The output pin $\overline{\text{ERR}}$ provides an open drain functionality. A current source is also connected to the pin $\overline{\text{ERR}}$. In normal operation the signal $\overline{\text{ERR}}$ is high. See **Chapter 3.5** for more details.

DS0, DS1 (Filter Select)

The internal filter delay can be selected by pulling those pins to VCC or to GND (see **Table 10**). These pins are for static configuration (pin-strapping).

$\overline{\text{CS}}$ (Chip Select)

When this pin is in a logic Low state, the IC interface is enabled and data can be transferred.

SEL (Serial or Parallel Mode Select)

When this pin is in a logic High state, the IC operates in Serial Mode. For Parallel Mode operation the pin has to be pulled into logic Low state. This pin has an internal Pull-UP resistor.

The following pins are provided by the parallel interface

D7:D0 (Data output bit7 ... bit0)

The pins D0 .. D7 are the outputs for data read.

$\overline{\text{RD}}$ (Read Select)

By pulling this pin down, a read transaction is initiated on the data bus and the data becomes valid.

The following pins are provided by the serial interface

SCLK (Serial interface shift clock)

Output data is updated with the falling edge of this input clock signal.

SDI (Serial interface input data)

SDI is put into a FIFO dedicated to the sensor data bits (no internal registers Write operation supported, only daisy chain). Input data is sampled with the rising edge of SCLK.

SDO (Serial interface data)

SDO provides the sensor data bits.

2 Blockdiagram

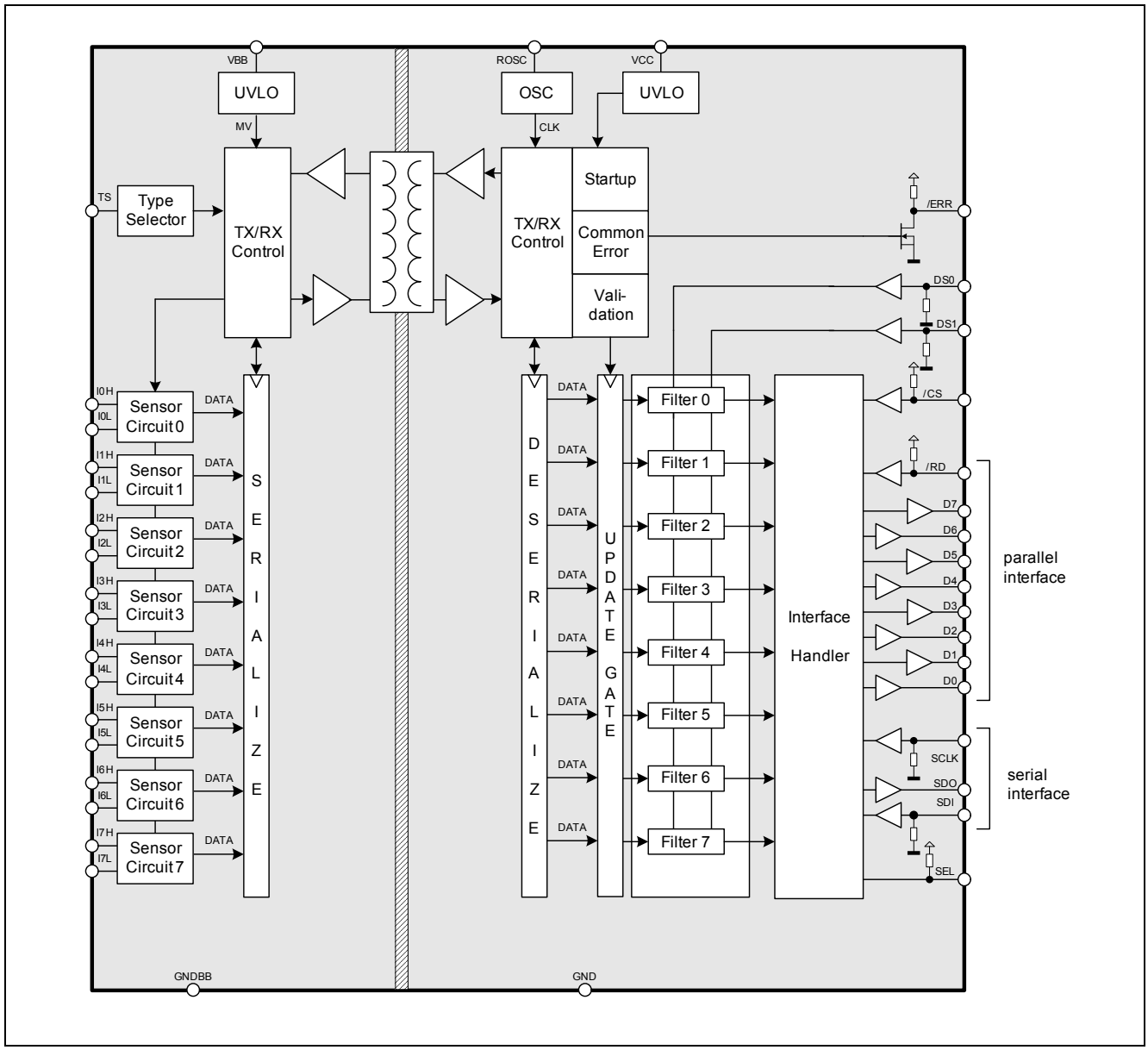


Figure 2 Block Diagram

3 Functional Description

The ISO1I811T is an electrically isolated 8 bit data input interface. This part is used to detect the signal states of eight independent input lines according to IEC61131-2 Type 1/2/3 (e.g. two-wire proximity switches) with a common ground (GNDBB).

3.1 Introduction

The current in the input circuit is determined by the switching element in state “0” and by characteristics of the input stage in state “1”.

The octal input device is intended for a configuration comprising of two specified external resistors per channel, as shown in **Figure 5 “Typical Application for Sensor Input Type 1, 2, and 3” on Page 13**. As a result the power dissipation within the package is at a minimum.

The voltage dependent current through the external resistor R_{EXT} is compensated by a negative differential resistance of the current sink across pins IxH and IxL, therefore input INx behaves like a constant current sink.

The comparator assigns level 1 or 0 to the voltage present at input IxH. To improve interference protection, the comparator is provided with hysteresis. A status LED is connected in series with the input circuit (R_{EXT} and current sink).

If no LED is used an external resistor of 2 kΩ should be connected between IxL and GNDBB. The specified switching thresholds may change if the resistor is used.

The LED drive short-circuits the status LED if the comparator detects “0”. A constant current sink in parallel with the LED reduces the operating current of the LED, and a voltage limiter ensures that the input circuit remains operational if the LED is interrupted, but the specified switching thresholds may change.

For each channel an adjustable digital filter is provided which samples the comparator signal at a rate selected by the pins DS0 and DS1. The digital filter is designed to provide averaging characteristics. If the input value remains the same for the selected number of sampling values, then the output changes to the corresponding state.

The control interface is compatible to standard microcontrollers. Furthermore a direct control mode can be selected that allows the direct control of the outputs D0...D7 by means of the inputs I0H...I7H without any additional logic signal. The µC compatible interfaces allows a direct connection to the ports of a microcontroller without the need for other components. The diagnostic logic on the chip monitors the internal data transfer as well as the sensor input supply. The information is sent via the internal coreless transformer to the pin $\overline{\text{ERR}}$ at the µC-Interface side.

3.2 Power Supply

The IC contains two electrically isolated voltage domains that are independent from each other. The microcontroller interface is supplied via pin VCC and the input stage is supplied via pin VBB. The different voltage domains can be switched on at different times. **Figure 3** shows the Start Up behaviour if both voltage domains are powered by an external power supply. If the VCC and VBB voltage have reached their operating range and the internal data transmission has been started successfully, the IC indicates the end of the Start Up procedure by setting the pin $\overline{\text{ERR}}$ to logic high.

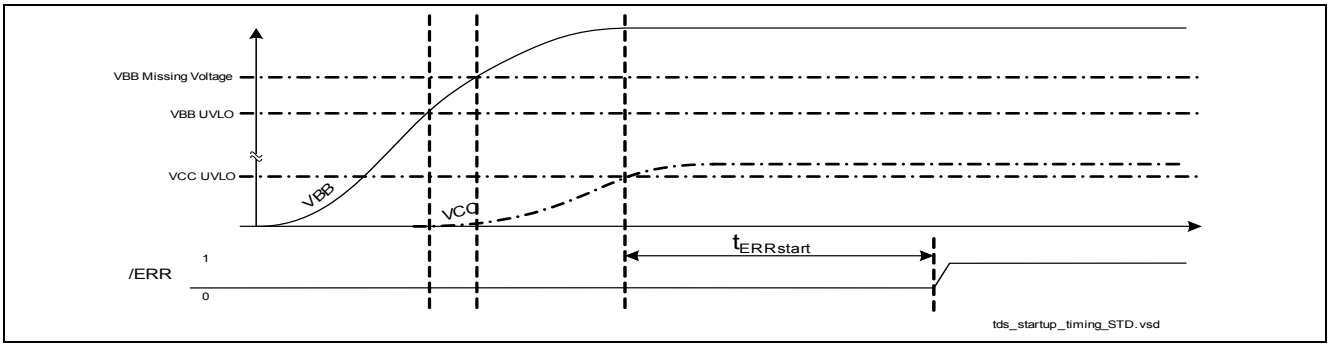


Figure 3 Start-Up

3.3 Internal Oscillator

An external resistor has to be connected to ROSC pin and allows the adjustment of the frequency as shown in **Figure 4**.

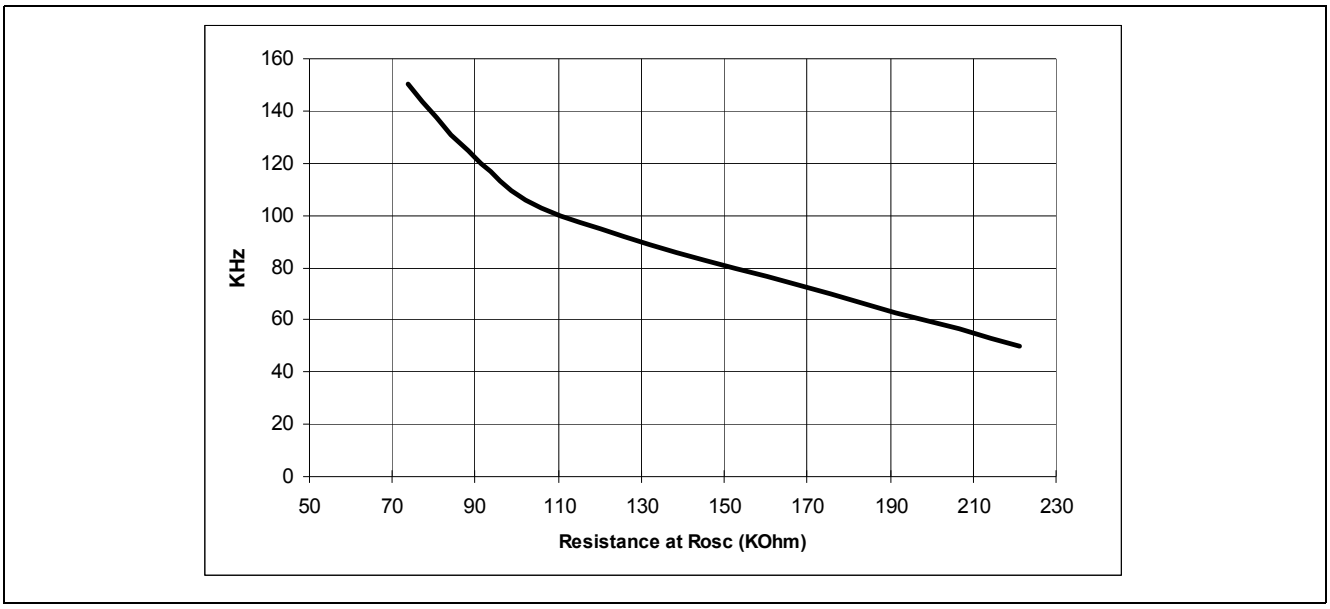


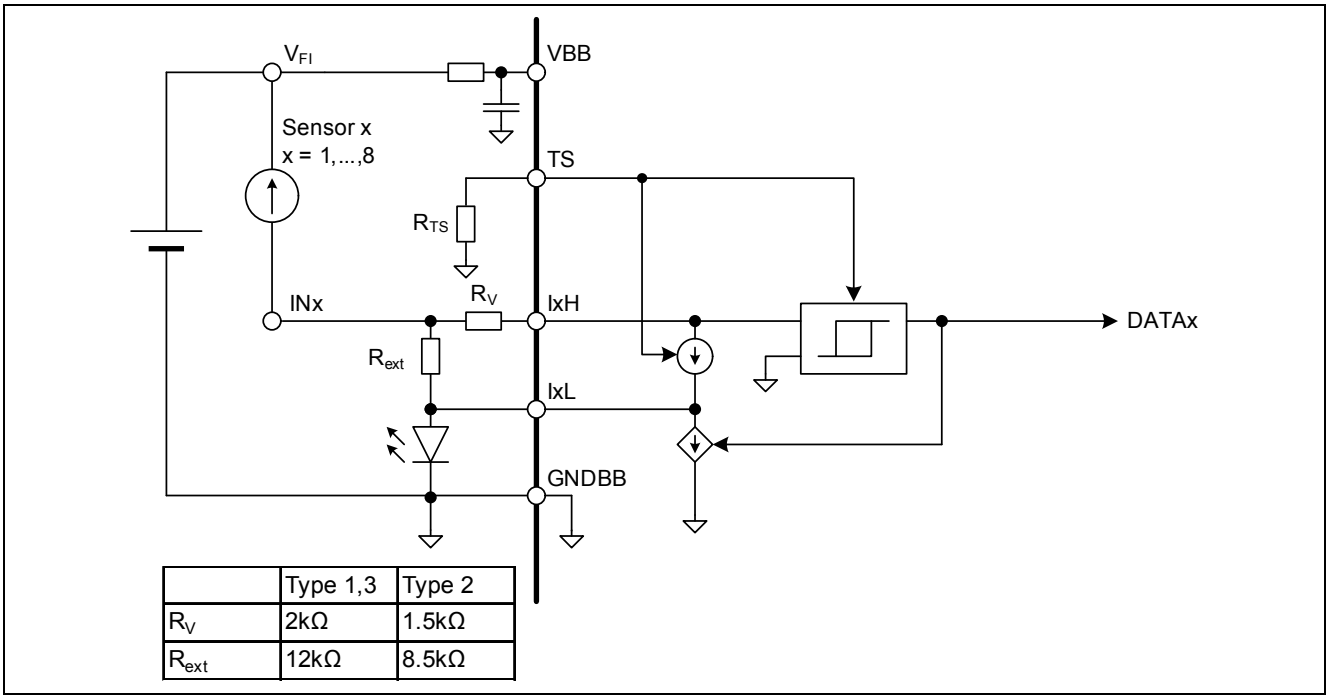
Figure 4 Internal Frequency Setting at ROSC

The internal oscillator provides the scan clock for the sampling of the sensor data as well as for the internal digital averaging filters. Therefore the filter times as defined in the **Table 10** for the typical frequency of 125 KHz will change accordingly. As an example, it is possible to define filter time longer than 20 ms by reducing the internal oscillator frequency.

3.4 Sensor Input

The sensor input structure is shown in **Figure 5**. Due to its active current a V-I-characteristic as shown in **Figure 6** is maintained. This V-I-curve is well within the IEC 61131 standard requirements of Type 1 and Type 3 sensors, respectively. Type 2 sensors are supported as well with the restriction that two input channels have to be used in parallel i.e. only 4 channels are available.

It is recommended to choose for the external resistors Rext, RV, RLED an accuracy of 2 % (< 5% is mandatory) otherwise the V/I-characteristic shown in **Figure 6** cannot be guaranteed.



	Type 1,3	Type 2
R_V	2kΩ	1.5kΩ
R_{ext}	12kΩ	8.5kΩ

Figure 5 Typical Application for Sensor Input Type 1, 2, and 3

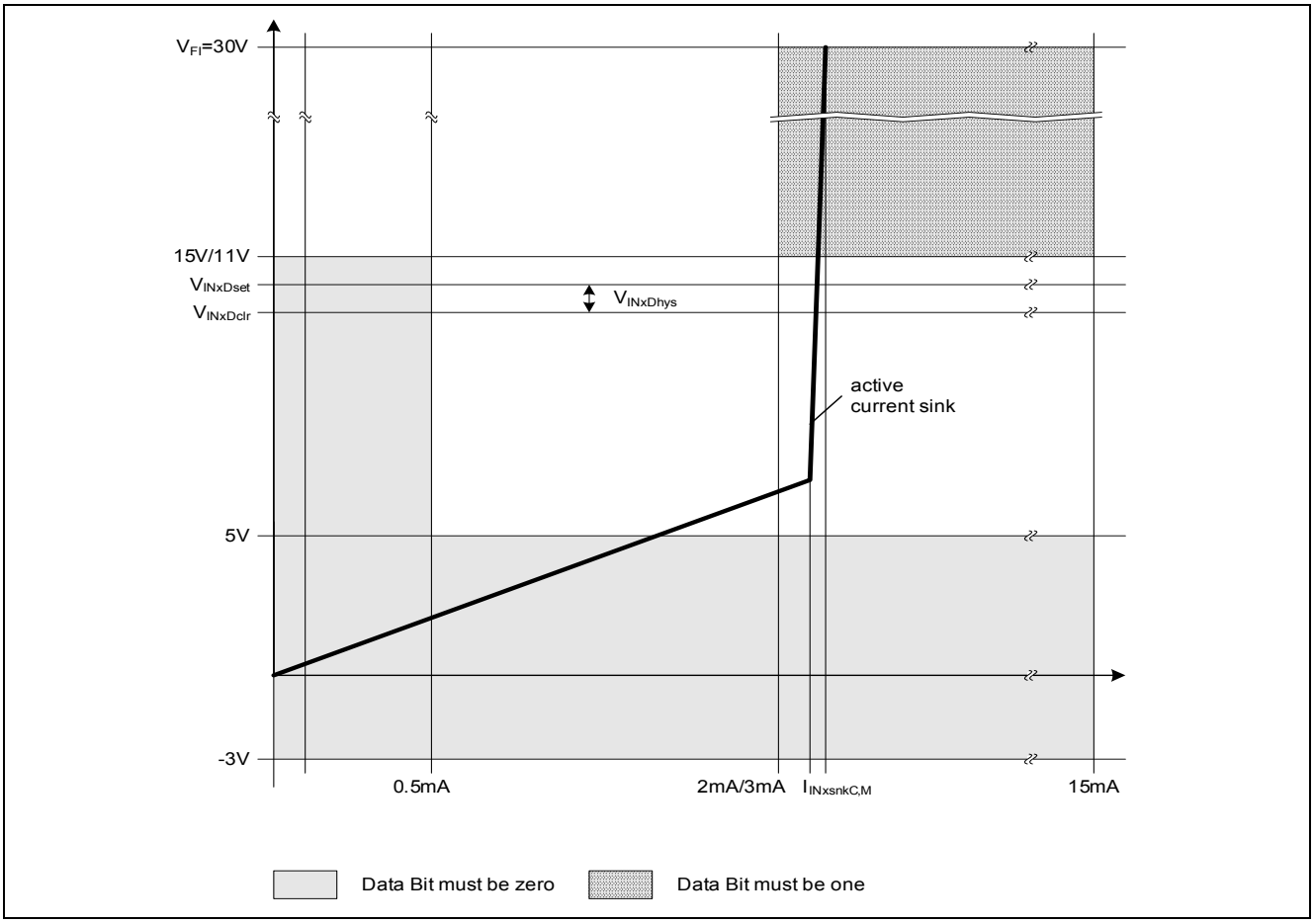


Figure 6 Sensor Input Characteristics

3.5 Common Error Output

The input (VBB) missing voltage status which is transmitted via the integrated coreless transformer to the output block and the internal data transmission monitoring information are evaluated in the common error output block, see **Figure 7**.

In case of an internal data transmission error the data bits are replaced by the last valid transmission. Moreover, if four consecutive erroneous data transmissions (TE1=1, see **Figure 7**) occur, an internal error signal TE4 (see **Figure 7**) is set. The average filters are reset. This status is held until four consecutive error-free transmissions (TE1=0) occur. An example timing diagram is shown in **Figure 7**. The internal W4S (Wait for Sense) signal indicates whether the Sense Input interface is operating properly or not.

This internal error signal is OR-wired with the current VBB missing voltage status. Since the output error signal is active low, the OR-wired result is negated.

The output stage at pin $\overline{\text{ERR}}$ has an open drain functionality with a pull-up resistor. See **Table 12** for the electrical characteristics.

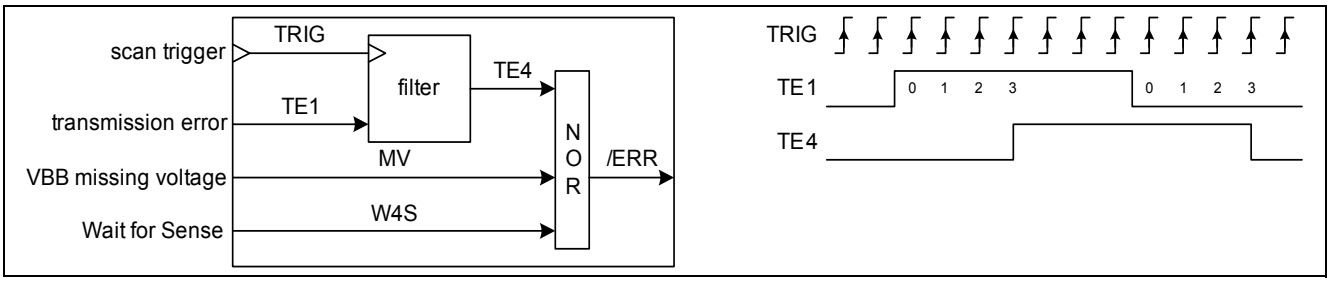


Figure 7 Common Error Output

3.6 Programmable Digital Input Filter

The sensor data bits can be filtered by a configurable digital input filter. If selected, the filter changes its output according to an averaging rule with a selectable average length. When the sensor state changes without any spikes and noise the change is delayed by the averaging length. Sensor spikes that are shorter than the averaging length are suppressed. **Figure 8** shows the behavior of the filter.

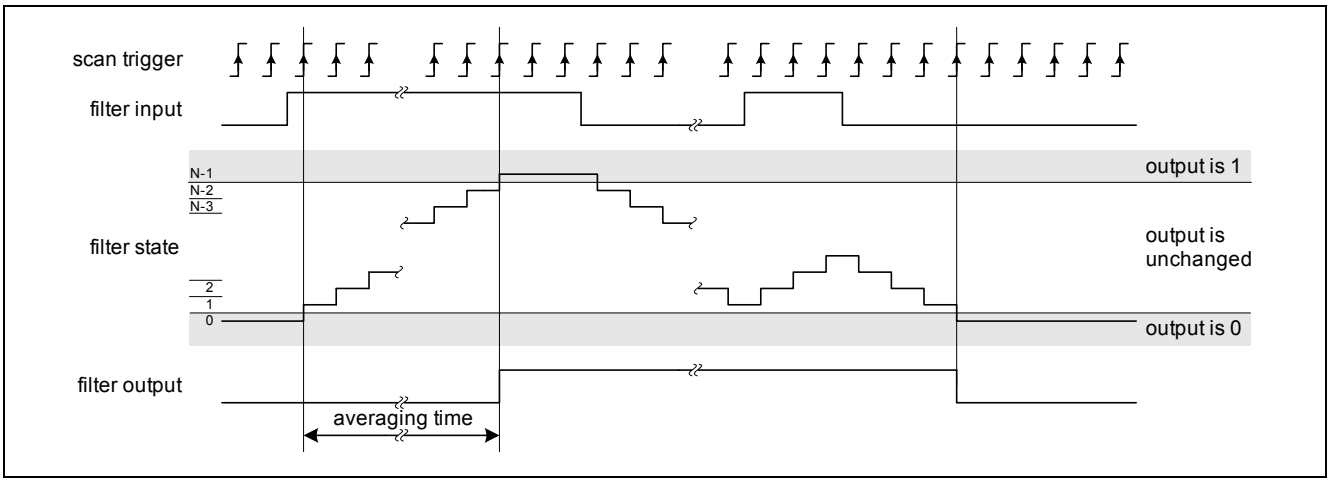


Figure 8 Digital Filter Behavior

The averaging length is selected using the configuration pins DS0 and DS1. See **Table 10** for the different setting options including filter bypass. The filters are dimensioned for the nominal internal sampling $f_{scannom}$. The corresponding filter delays can be adjusted by changing the oscillator frequency i.e. by tuning the resistor at the ROSC pin.

3.7 Parallel Interface Mode

The ISO1I811T contains a parallel interface that can be selected by pulling the SEL Pin to logic low state. It can be directly controlled by the microcontroller output ports. (**Figure 9**, left side). The output pins D7:D0 are in state “Z” as long as $\overline{CS}$=1. Otherwise, new sensor data bits bits are sampled with the falling edge of $\overline{RD}$ and provided at pins D7:D0.

The parallel interface can also be switched over to a direct control mode to observe continuously the changes of the inputs I0H ... I7H by means of the corresponding outputs D7:D0 without additional logic signals. To activate the parallel direct control mode pin $\overline{CS}$ and pin $\overline{RD}$ have to be connected both to ground (permanently as in **Figure 9**, right side or by the microcontroller ports). The Direct Control Mode is entered when at least $\overline{CS}$ and $\overline{RD}$ are held low for t_{direct} (**Table 14**).

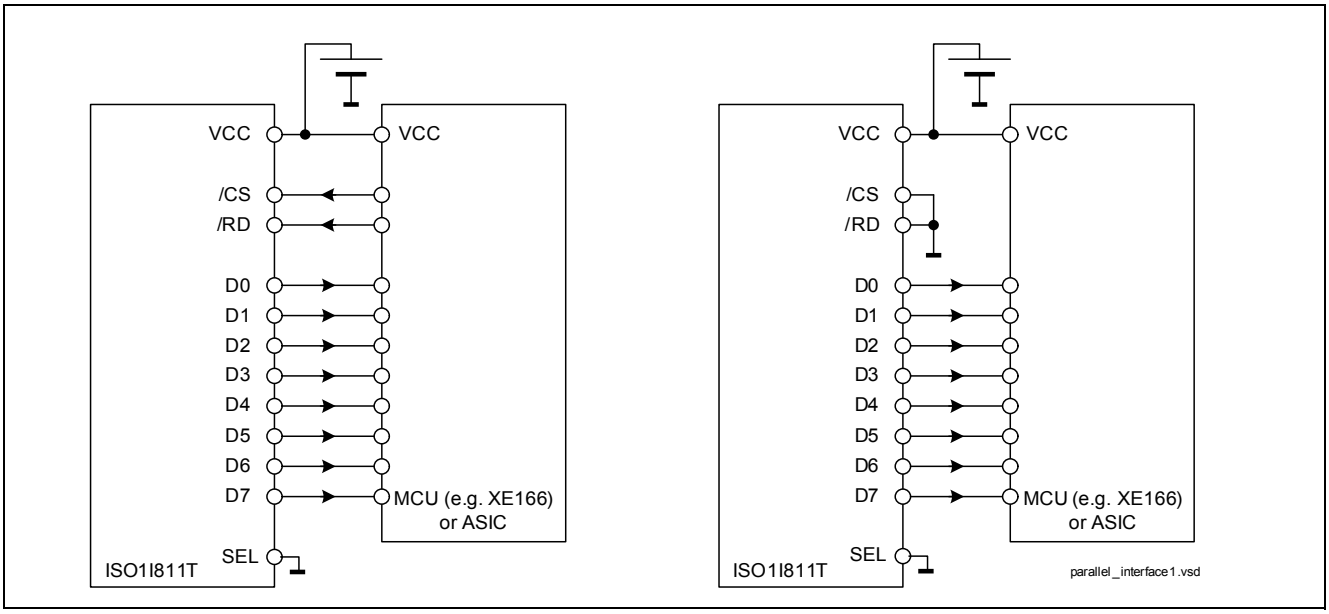


Figure 9 Parallel Bus Configuration for µC-Control-Mode (left) or Direct Control Mode (right)

The timing requirements for the parallel interface are shown in **Figure 10** and in **Table 14**.

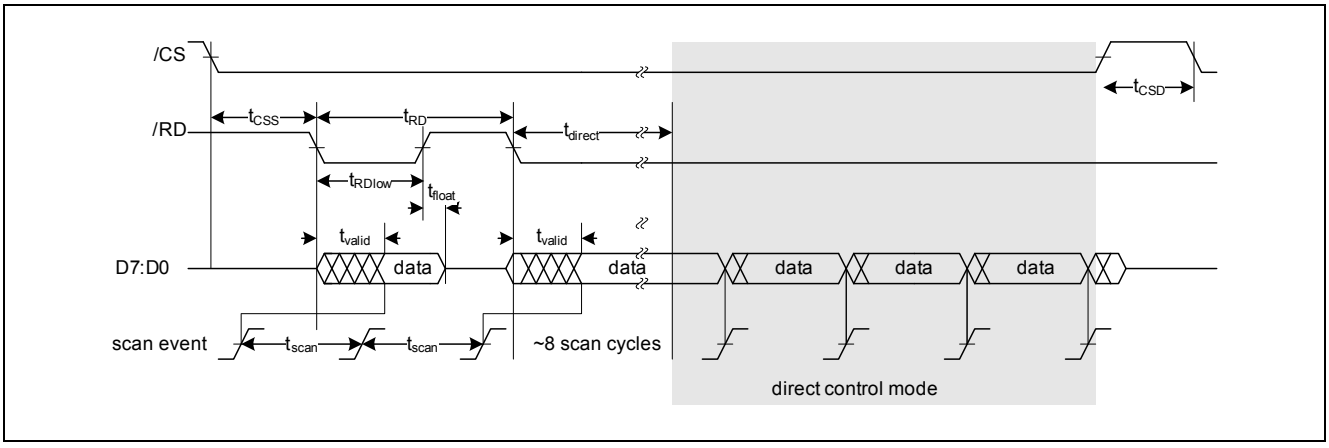


Figure 10 Parallel Bus Timing

3.8 Serial Interface Mode

The ISO1I811T contains a serial interface that can be activated by pulling the SEL pin to logic High state. It can be directly controlled by the microcontroller output ports. The output pin SDO is in state “Z” as long as $\overline{CS}$=1. Otherwise, the bits are sampled with the falling edge of $\overline{CS}$. Subsequently with every falling edge of SCLK the bits are provided serially to the pin SDO. At the same time, the input to SDI is put into an 8bit FIFO buffer sampled with the rising edge of SCLK. When all 8 internally sampled bits have been put to SDO, the buffered bits from the input SDI are provided to the serial output pin SDO (Daisy Chain Mode).

The timing requirements for the parallel interface are shown in **Figure 11** and in **Table 15**.

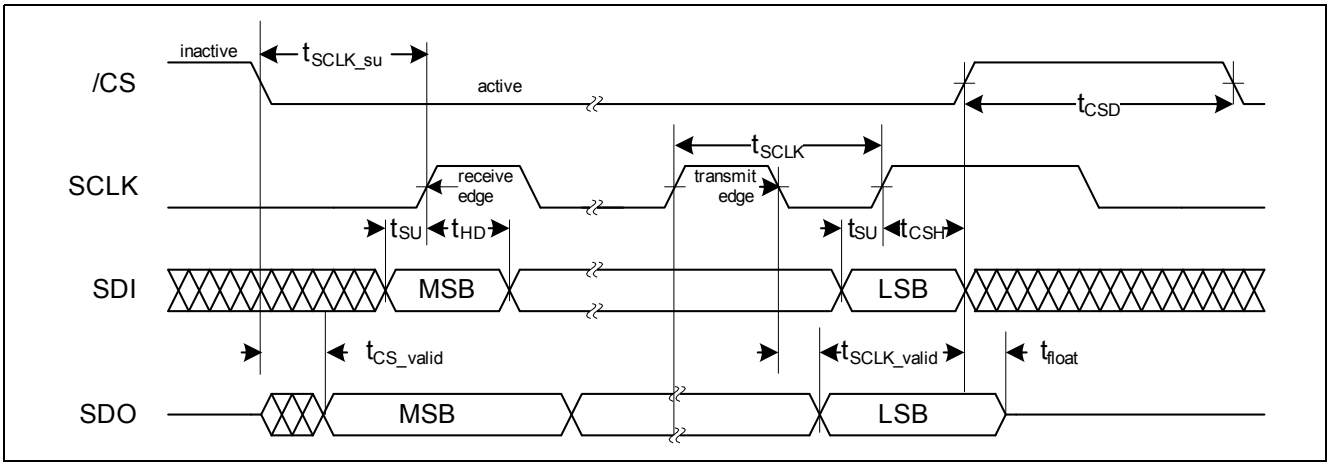


Figure 11 Serial Bus Timing

Several SPI topologies are supported: pure bus topology and daisy-chain (**Figure 12**). Of course independent individual control with dedicated SPI controller interfaces for each slave IC are possible, as well.

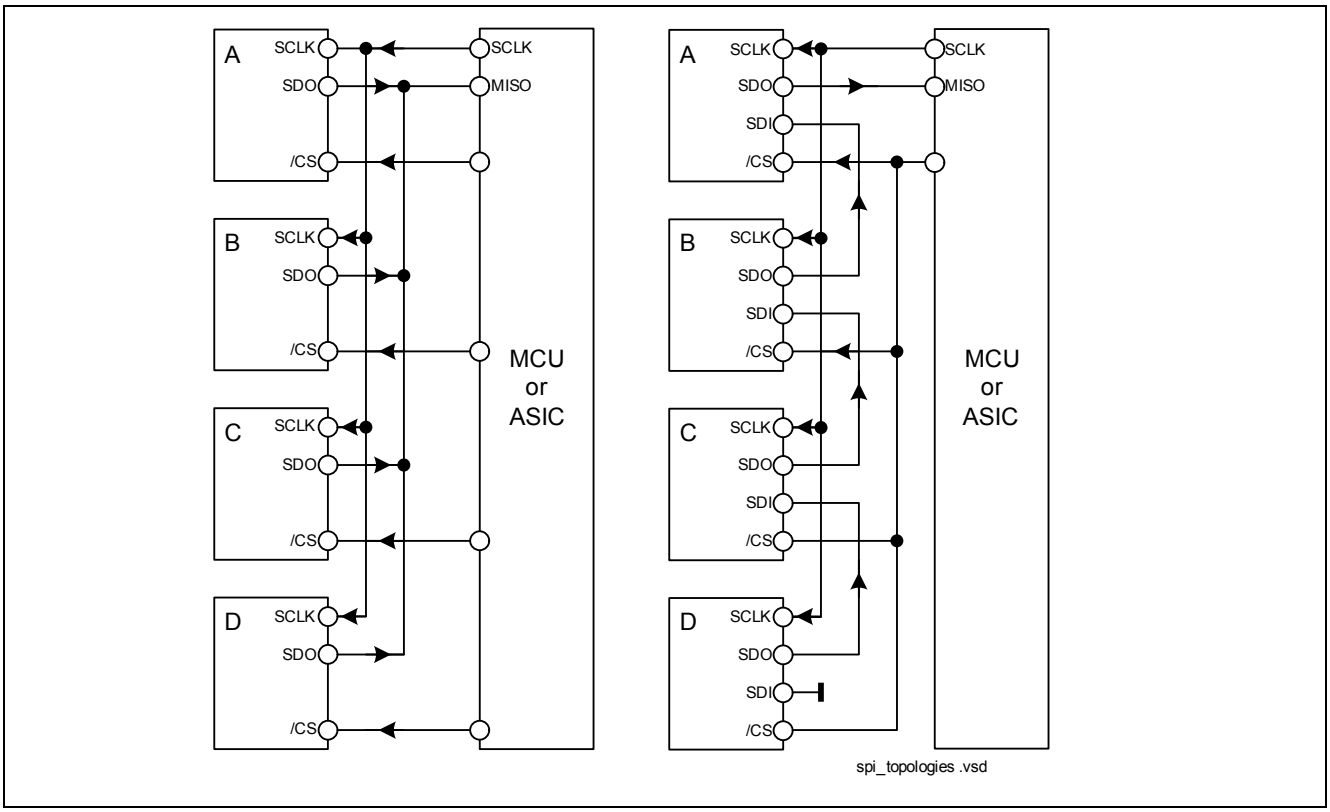


Figure 12 Example SPI Topologies

4 Standard Compliance

The ISO1I811T allows the design of a sensor interface compliant with the standard requirements listed below:

System Insulation Characteristics as shown in **Table 3**,

System Maximum Ratings as shown in **Table 2**.

There requirements are valid for an application using the ISO1I811T including external circuitry (as proposed in **Figure 13**), not for the IC alone.

Note: When the IC is not supplied via V_{BB}, probing of the digital input interface is still possible due to the external circuitry, i.e. the 12k resistor and the LED. In addition to the current through the LED a small current I_{IxH} flows through the pins IxH and IxL.

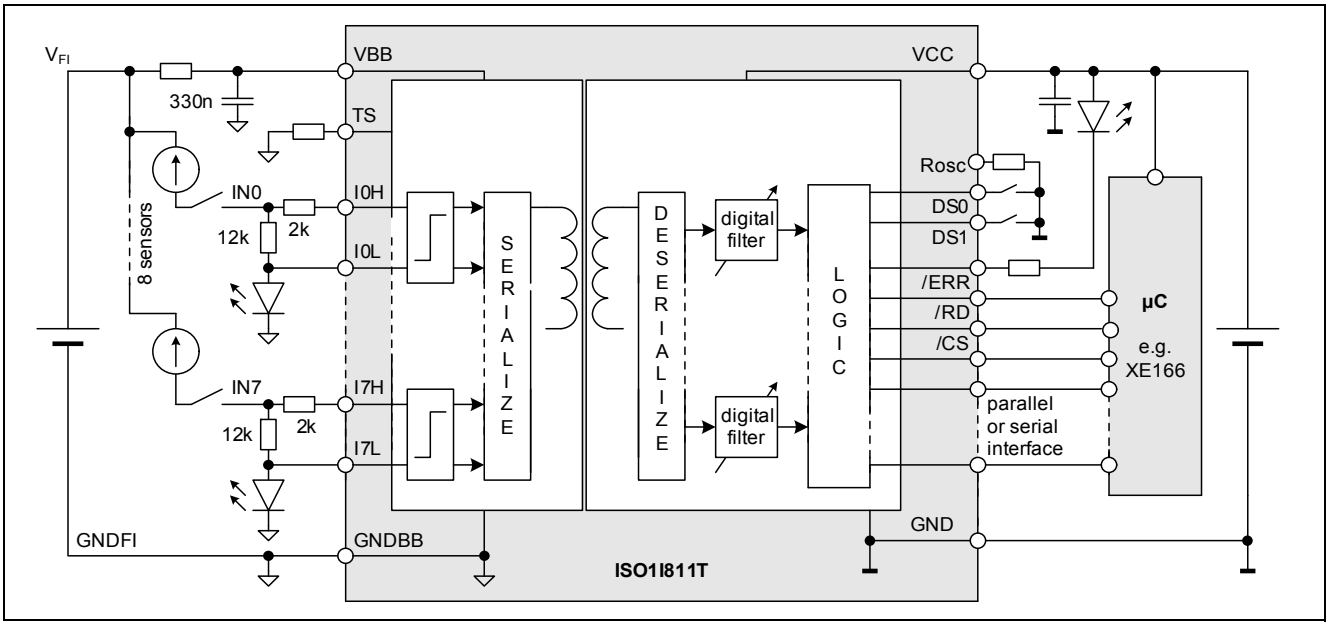


Figure 13 Recommended Application Circuit

Table 2 System Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Field Input Voltage Overvoltage 1300 ms	V_{FIov}	-45		+45	V	
Input Voltage INx	V_{INx}	-45		+45	V	

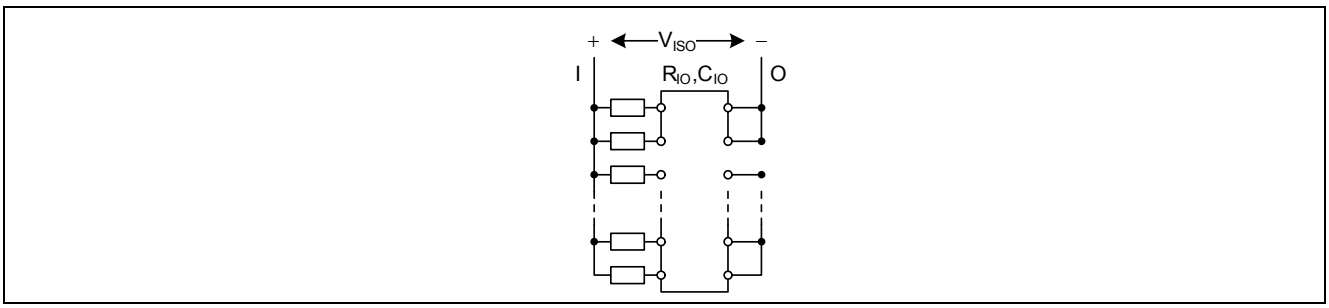


Figure 14 System Insulation Characteristics

Table 3 System Insulation Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pollution Degree (DIN VDE 0110/1.89, DIN EN 60664-1)			2			
Minimum External Clearance	CLR	6.7			mm	
Minimum External Creepage	CPG	6.2			mm	
Maximum Working Insulation Voltage	V_{ISO}	500			V_{AC}	1 min duration[1)]

1) not subject to production test, verified by characterization

Approvals:

UL1577

Certificate Number: 20120309-E311313

5 Electrical Characteristics

This section comprises:

- Operating Conditions and Power Supply (see **Section 5.2**)
- Electrical Characteristics Input Side (see **Section 5.3**)
- Electrical Characteristics Microcontroller Interface (see **Section 5.4**)

Tolerance values always contain the sum of process-related tolerance values and tolerance-values based on the temperature drift within the specified temperature range.

5.1 Absolute Maximum Ratings

All voltages at pins 25 to 48 are measured with respect to ground GNDBB. All voltages at pins 1 to 24 are measured with respect to GND. The voltage levels are valid if other ratings are not violated. The two voltage domains VCC, GND and VBB, GNDBB are internally electrically isolated.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only for functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4 Absolute Maximum Ratings

Parameter	Symbol	Value		Unit	Note / Test Condition
		Min.	Max.		
Continuous Voltage at pin VBB	V_{VBB}	-0.3	45	V	Power Dissipation must not exceed max-value
Peak Voltage VBB, Overvoltage 500 ms	V_{VBB}	-0.3	45	V	
Supply Voltage VCC	V_{VCC}	-0.3	6.5	V	
Continuous Voltage at logic pins 1 - 24 (except VCC and GND pins)	V_{LOG}	-0.3	6.5	V	
Continuous Voltage at pin TS		-0.3	6.5	V	
Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_S	-50	150	°C	
Power Dissipation	P_{tot}		800	mW	
Input Voltage Range	V_{IxH}	-45	45	V	
Input Voltage Range	V_{IxL}	-0.3	5	V	
Error Pin Sink Current ($\overline{ERR}$=0)	$I_{ERRsink}$		5	mA	VERR < 0.25·V_{VCC}
Electrostatic discharge voltage (Human Body Model) according to JESD22-A114-B	V_{ESD}	–	2.5	kV	
Electrostatic discharge voltage (Charge Device Model) according to ESD STM5.3.1 - 1999	V_{ESD}	–	1.5	kV	

5.2 Operating Conditions and Power Supply

For proper operation of the device, absolute maximum rating (**Section 4**) and the parameter ranges in **Table 5** must not be violated. Exceeding the limits of operating condition parameters may result in device malfunction or spec violations. The power supply pins VBB and VCC have the characteristics given in **Table 7**.

Table 5 Operating Range

Parameter at T_j = -40 ... 125°C	Symbol	Value		Unit	Note / Test Condition
		Min.	Max.		
Supply Voltage Logic VCC	V_{VCC}	2.85	5.5	V	related to GND
Supply Voltage Senses VBB	V_{VBB}	9.6	35	V	related to GNDBB
Ambient Temperature	T_A	-40	85	°C	
Junction Temperature	T_J	-40	125	°C	
Common Mode Transient	dV_{ISO}/dt	-25	25	kV/µs	
Magnetic Field Immunity	$\|H_{IM}\|$	30		A/m	IEC61000-4-8

Table 6 Thermal Characteristics

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Limit Values		Unit	Note / Test Condition
		Min.	Max.		
Thermal resistance junction - case top	R_{thJC_Top}		15.0	K/W	measured on top side[1)]
Thermal resistance junction - case bottom	R_{thJC_Bot}		13.8	K/W	1)
Thermal resistance junction - pin	R_{thJP}		11.8	K/W	1)
Thermal resistance @ 2 cm² cooling area[2)] (thermal conductance only by radiation and free convection)	$R_{th(JA)}$		88.6	K/W	1)

1) not subject to production test, specified by design

2) Device on 50 mm x 50 mm x 1.5 mm epoxy PCB FR4 with 2 cm² (one layer, 35 µm thick) copper area. PCB is vertical without blow air.

Table 7 Electrical Characteristics of the Power Supply Pins

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VBB UVLO startup threshold	V_{VBBon}			9.6	V	
VBB UVLO shutdown threshold	V_{VBBoff}	8.0			V	
VBB UVLO Hysteresis	V_{VBBhys}		1		V	
VBB missing voltage OFF (MV) threshold	$V_{VBBmvoff}$			13.9	V	
VBB missing voltage ON (MV) threshold	$V_{VBBmvon}$	12.1			V	
Glitch filters for VBB missing voltage and undervoltage	T_{VBBfil}		40		µs	1)
Undervoltage Current for VBB	I_{VBBuv}		3.5		mA	$V_{VBB} < V_{VBBon}$

Table 7 Electrical Characteristics of the Power Supply Pins (cont'd)

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Quiescent Current VBB	I_{VBBq}		4.5		mA	V_{VBB} = 24 V, I_{INx} = 0, VCC = 0V
Startup Delay (time between VBBon/VCCon and $\overline{ERR}$ high)	$t_{ERRstart}$		130		µs	Digital Filter bypassed [1]
Startup Delay (time between VBBon/VCCon and first data output)	t_{VXXon}		130		µs	Digital Filter bypassed [1]
VCC UVLO startup threshold	V_{VCCon}			2.85	V	
VCC UVLO shutdown threshold[2]	V_{VCCoff}	2.5			V	
VCC UVLO threshold hysteresis	V_{VCChys}		0.1		V	
Quiescent Current VCC	I_{VCCq}		3.1		mA	V_{VCC} = 5 V, V_{VBB} = 0V [1]
Quiescent Current VCC	I_{VCCq}		2.3		mA	V_{VCC} = 3.3 V, V_{VBB} = 0V [1]

1) valid for $f_{scantyp}$ = 100kHz

2) Note that the specified operation of the IC requires V_{VCC} as given in **Table 5**

5.3 Electrical Characteristics Input Side

The electrical characteristics of the input side (pins 25-48) are given in **Table 8**. Note that some parameters refer to IN0 to IN7 which are nodes of external circuitry (see **Figure 5** or **Figure 13**). Electrical characteristics with respect to these nodes are given for the system including the external circuitry and not for the IC alone.

See also **Figure 6** for the different threshold parameters.

Table 8 Sensors Inputs

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sink Current Limit at Saturation Edge Type 1/3	$I_{INxsnkC13}$	2.3			mA	$V_{VBB}=V_{VBBon}$, V_{INx}=6.7V, V_{IxL}=1.2V
Sink Current Limit at Saturation Edge Type 2	$I_{INxsnkC2}$	3.3			mA	$V_{VBB}=V_{VBBon}$, V_{INx}=6.7V, V_{IxL}=1.2V
Sink Current Limit at Maximum Input Voltage Type 1/3	$I_{INxsnkM13}$			3.4	mA	V_{VBB}=35V, V_{INx}=30V, V_{IxL}=2.5V
Sink Current Limit at Maximum Input Voltage Type 2	$I_{INxsnkM2}$			4.8	mA	V_{VBB}=35V, V_{INx}=30V, V_{IxL}=2.5V
LED Supply Current at Maximum Input Voltage, Type 1/3	I_{IxLmax}	2.1		3.1	mA	V_{VBB}=35V, V_{INx}=30V, V_{IxL}=2.5V
LED Supply Current at Maximum Input Voltage, Type 2	I_{IxLmax}	3.1		4.5	mA	V_{VBB}=35V, V_{INx}=30V, V_{IxL}=2.5V
LED Supply Current at High Threshold Type 3	I_{IxL1}	1.5		2.5	mA	$V_{VBB}=V_{VBBon}$, V_{INx}=11V, V_{IxL}=2.5V
LED Supply Current at High Threshold Type 2	I_{IxL2}	2.3		3.6	mA	$V_{VBB}=V_{VBBon}$, V_{INx}=11V, V_{IxL}=2.5V
LED Supply Current at High Threshold Type 1	I_{IxL3}	1.6		2.6	mA	$V_{VBB}=V_{VBBon}$, V_{INx}=15V, V_{IxL}=2.5V
LED Voltage	V_{FLED}	1.9		3.0	V	1)
Sense Voltage Switching Threshold, L→H (Type 1)	$V_{INxDset(1)}$			15	V	V_{VBB}=24V V_{IxL}=2.5V 2)
Sense Voltage Switching Threshold H→L (Type 1)	$V_{INxDclr(1)}$	11			V	V_{VBB}=24V V_{IxL}=2.5V 2)
Hysteresis H↔L (Type 1)	$V_{INxDhys(1)}$		1		V	
Sense Voltage Switching Threshold L→H (Type 2)	$V_{INxDset(2)}$			11	V	V_{VBB}=24V V_{IxL}=2.5V 2)
Sense Voltage Switching Threshold H→L (Type 2)	$V_{INxDclr(2)}$	7			V	V_{VBB}=24V V_{IxL}=2.5V 2)
Hysteresis H↔L (Type 2)	$V_{INxDhys(2)}$		0.65		V	
Sense Voltage Switching Threshold L→H (Type 3)	$V_{INxDset(3)}$			11	V	V_{VBB}=24V V_{IxL}=2.5V 2)
Sense Voltage Switching Threshold H→L (Type 3)	$V_{INxDclr(3)}$	7			V	V_{VBB}=24V V_{IxL}=2.5V 2)

Table 8 Sensors Inputs (cont'd)

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Hysteresis H↔L (Type 3)	$V_{INxDhys(3)}$		0.7		V	
Input Sink Current when V_{VBB}=0	I_{IxHq}		300		µA	V_{VBB}=0V V_{IxH}=30V, IxI = open

1) not subject to production test, specified by design; recommended for proper operation

2) clamped to 2.5V if "logic 1", internally limited if logic "0"

Table 9 Setting at the Configuration Pin TS

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TS Pull-Down Resistance for Type 1 Selection	R_{TSpd1}		33		Ω	1)
TS Pull-Down Resistance for Type 2 Selection	R_{TSpd2}		33		kΩ	2) 1)
TS Pull-Down Resistance for Type 3 Selection	R_{TSpd3}		330		kΩ	1)
Max. TS Pin Load Capacitance	C_{TSmax}			20	pF	1)

1) required for operation

2) Only 4 channels can be used for this case.

5.4 Electrical Characteristics Microcontroller Interface

Timing characteristics refer to C_L < 50 pF and R_L > 10 kΩ.

Table 10 Sensor Scanning and Averaging

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Scan Frequency Range	$f_{scanrge}$	50		150	kHz	1) refer to **Figure 4**
Input Scan Propagation Delay	$t_{ctdelay}$		40		µs	applies equally to all channels 2)
Filter Bypass delay	t_{bypass}		10		µs	2)
Input Scan Jitter	Δt_{scan}			10	µs	2)
Input Scan Processing Delay	t_{delay}		60		µs	2)
Digital Filter Monitoring Time N=125_D	t_{FILT01}		1.0		ms	DS0=L, DS1=H 2)
Digital Filter Monitoring Time N=400_D	t_{FILT02}		3.2		ms	DS0=H, DS1=L2)
Digital Filter Monitoring Time N=1248_D	t_{FILT03}		10.0		ms	DS0=L, DS1=L 2)
Digital Filter Monitoring Time Filter is Bypassed	$t_{FILToff}$		10		µs	DS0=H, DS1=H 2)

1) not subject to production test, specified by design

2) valid for $f_{scantyp}$ = 100kHz

Table 11 Setting at the Configuration Pin (CLKADJ) see also Figure 4

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ROSC Resistance to GND	R_{OSC}	73.2		221	kΩ	E96 resistor
ROSC Pin Regulated Voltage	$V_{ROSCreg}$		1.2		V	
Max. ROSC Pin Load Capacitance	$C_{ROSCmax}$			5	pF	1)

1) required for operation

Table 12 Error Pin ($\overline{ERR}$)

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Error Pin Pull-Up Resistance ($\overline{ERR}$=1)	R_{ERRpu}		50		kΩ	
$\overline{ERR}$-Maximum Switching Frequency	f_{SW}	10		125	kHz	1)
Error Pin low voltage	V_{ERROL}			0.25·V_{VCC}	V	I_{FIOL} = 5mA

1) not subject to production test, specified by design

Table 13 Logical Pins ($\overline{RD}$, DS0/1, $\overline{CS}$, D7:D0, SCLK, SDO, SDI, SEL)

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Voltage High Level	V_{IH}	0.7·V_{VCC}		V_{VCC}+0.3	V	
Input Voltage Low Level	V_{IL}	-0.3		0.3·V_{VCC}	V	
Input Voltage Hysteresis	V_{Ihys}		100		mV	
Output Voltage High Level	V_{OH}	0.75·V_{VCC}		V_{VCC}	V	I_{OH} = 5mA
Output Voltage Low Level	V_{OL}	0		0.25·V_{VCC}	V	I_{OL} = 5mA

Table 14 Parallel Interface

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Pull Up Resistance ($\overline{RD}$, $\overline{CS}$)	R_{PU}		50		kΩ	
Read Request Frequency	f_{RD}	0.06[1)]		5	MHz	repeated read access during $\overline{CS}$ = low
Read Request Period (1/f_{RD})	t_{RD}	200		15000[2)]	ns	
$\overline{CS}$ Setup time (falling edge of $\overline{CS}$ to falling edge of $\overline{RD}$)	t_{CSS}	55			ns	
$\overline{CS}$ Disable time (minimum $\overline{CS}$ high time between two accesses)	t_{CSD}	35			µs	
D7:D0 Output disable time	t_{float}			80	ns	
D7:D0 Output Valid (by Read)	t_{valid}			80	ns	
$\overline{RD}$ Low duration (by Read)	t_{RDlow}	100			ns	
Waiting Time for $\overline{CS}$=$\overline{RD}$=0 until transparent mode is entered	t_{direct}	50			µs	1) 3)

1) Minimum value to ensure that the direct control mode is not entered, see also t_{RD} and t_{direct}

2) After 50 µs the interface may enter the direct control mode, see also t_{direct}

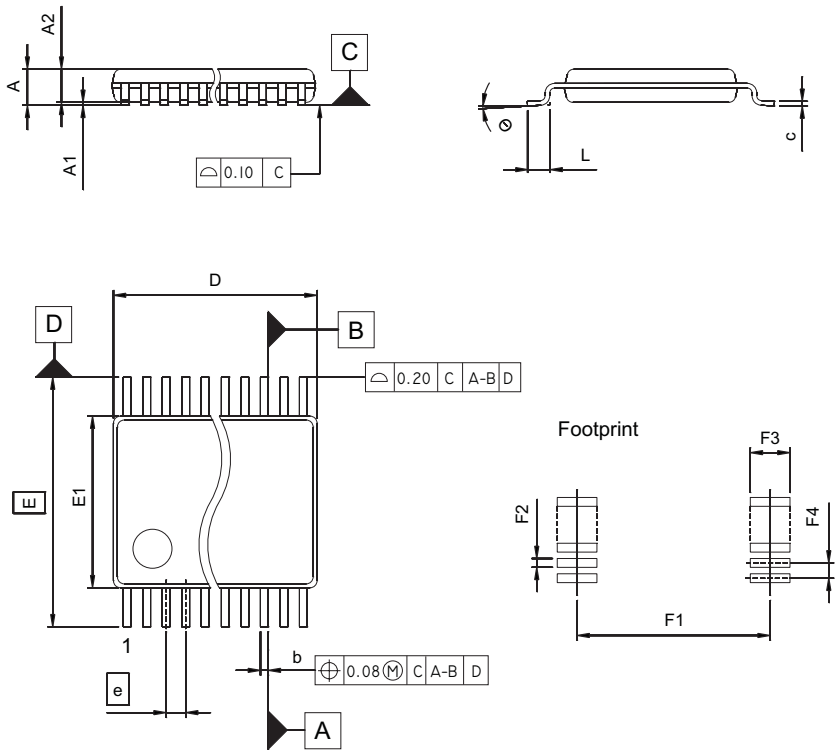
3) not subject to production test, specified by design

Table 15 Serial Interface

Parameter at T_j = -40 ... 125°C, V_{bb}=9.6...35V, V_{CC}=2.85...5.5V, unless otherwise specified	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Pull Up Resistance ($\overline{CS}$)	R_{PU}		50		kΩ	
Input Pull Down Resistance (SCLK, SDI)	R_{PD}		50		kΩ	
Serial Clock Frequency	f_{SCLK}			5	MHz	
Serial Clock Period ($1/f_{SCLK}$)	t_{SCLK}	200			ns	
Serial Clock High Period	t_{SCLKH}	100			ns	
Serial Clock Low Period	t_{SCLKL}	100			ns	
Data setup time (required time SDI to rising edge of SCLK)	t_{SU}	5			ns	
Data hold time (rising edge of SCLK to SDI)	t_{HD}	15			ns	
Minimum $\overline{CS}$ Hold time (rising edge of SCLK to rising edge of $\overline{CS}$)	t_{CSH}	40			ns	
Minimum $\overline{CS}$ Disable time ($\overline{CS}$ high time between two accesses)	t_{CSD}	24			µs	1)
$\overline{CS}$ falling edge to SDO output valid time	t_{CS_valid}	50			ns	
$\overline{CS}$ falling edge to first rising SCLK edge	t_{SCLK_su}	80			ns	
SCLK falling edge to SDO output valid time	t_{SCLK_valid}			80	ns	
Minimum SDO Output disable time	t_{float}			65	ns	

1) valid for $f_{scantyp}$ = 100kHz

6 Package Outline



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.10	-	0.043
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.17	0.27	0.007	0.011
c	0.09	0.16	0.004	0.006
D	12.40	12.60	0.488	0.496
E	8.10 BSC		0.319 BSC	
E1	6.00	6.20	0.236	0.244
e	0.50 BSC		0.020 BSC	
N	48		48	
L	0.50	0.75	0.020	0.030
Θ	0°	8°	0°	8°
F1	7.80		0.307	
F2	0.29		0.011	
F3	1.30		0.051	
F4	0.50		0.020	

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SCALE 0 1.0 0 1.0 2mm

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Figure 6-1 Package Outline TSSOP-48 (tie bar not drawn in outline)

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages***
2. *Dimensions in mm.*

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