

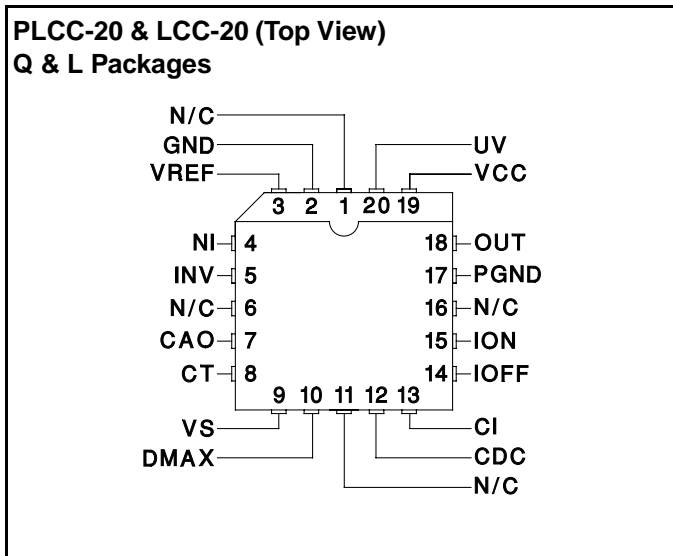
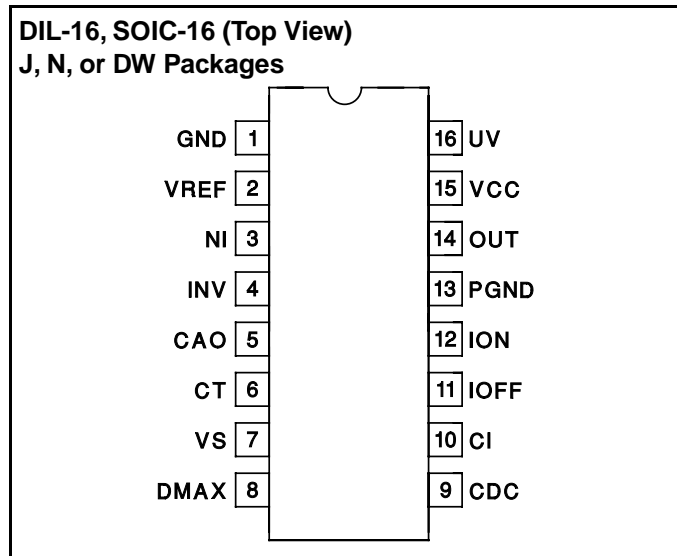
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pin 15)	22V
Output Current, Source or Sink (Pin 14)	
DC	0.5A
Pulse (0.5μs)	2.2A
Power Ground to Ground (Pin 1 to Pin 13)	±0.2V
Analog Input Voltages	
(Pins 3, 4, 7, 8, 12, 16)	-0.3 to 7V
Analog Input Currents, Source or Sink	
(Pins 3, 4, 7, 8, 11, 12, 16)	1mA

Analog Output Currents, Source or Sink (Pins 5 & 10)	5mA
Power Dissipation at TA = 60°C	1W
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 seconds)	+300°C

Notes: All voltages are with respect to ground (DIL and SOIC pin 1). Currents are positive into the specified terminal. Pin numbers refer to the 16 pin DIL and SOIC packages. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications are over the junction temperature range of -55°C to +125°C for the UC1548, -40°C to +85°C for the UC2548, and 0°C to +70°C for the UC3548. Test conditions are: VCC = 12V, CT = 400pF, CI = 100pF, IOFF = 100μA, CDC = 100nF, Cvs = 100pF, and Ivs = 400μA, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Real Time Current Waveform Synthesizer					
Ion Amplifier					
Offset Voltage		0.95	1	1.05	V
Slew Rate (Note 1)		20	25		V/μs
lib			-2	-20	μA
IOFF Current Mirror					
Input Voltage		0.95	1	1.05	V
Current Gain		0.9	1	1.1	A/A
Current Error Amplifier					
AVOL		60	100		dB
Vio	12V ≤ VCC ≤ 20V, 0V ≤ VCM ≤ 5V			10	mV
lib			-0.5	-3	μA
Voh	Io = -200μA	3.1	3.3	3.5	V
Vol	Io = 200μA		0.3	0.6	V
Source Current	Vo = 1V	1.4	1.6	2.0	mA
GBW Product	f = 200kHz	5	8		MHz
Slew Rate (Note 1)		8	10		V/μs
Oscillator					
Frequency	TA = 25°C	240	250	260	kHz
		235		265	kHz

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, all specifications are over the junction temperature range of -55°C to $+125^{\circ}\text{C}$ for the UC1548, -40°C to $+85^{\circ}\text{C}$ for the UC2548, and 0°C to $+70^{\circ}\text{C}$ for the UC3548. Test conditions are: $V_{CC} = 12\text{V}$, $C_T = 400\text{pF}$, $C_I = 100\text{pF}$, $I_{OFF} = 100\mu\text{A}$, $C_{DC} = 100\text{nF}$, $C_{VS} = 100\text{pF}$, and $I_{VS} = 400\mu\text{A}$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Duty Cycle Clamp					
Max Duty Cycle	$V(D_{MAX}) = 0.75 \cdot V_{REF}$	73.5	76.5	79.5	%
VCC Comparator					
Turn-on Threshold			13	14	V
Turn-off Threshold		9	10		V
Hysteresis		2.5	3	3.5	V
UV Comparator					
Turn-on Threshold		4.1	4.35	4.6	V
RHYSTERESIS	$V_{UV} = 4.2\text{V}$	77	90	103	$k\Omega$
Reference					
VREF	$T_A = 25^{\circ}\text{C}$	4.95	5	5.05	V
	$0 < I_O < 10\text{mA}$, $12 < V_{CC} < 20$	4.93		5.07	V
Line Regulation	$12\text{V} < V_{CC} < 20\text{V}$		4	15	mV
Load Regulation	$0 < I_O < 10\text{mA}$		3	15	mV
Short Circuit Current	$V_{REF} = 0\text{V}$	30	50	70	mA
Output Stage					
Rise & Fall Time (Note 1)	$C_I = 1\text{nF}$		20	45	ns
Output Low Saturation	$I_O = 20\text{mA}$		0.25	0.4	V
	$I_O = 200\text{mA}$		1.2	2.2	V
Output High Saturation	$I_O = -200\text{mA}$		2.0	3.0	V
UVLO Output Low Saturation	$I_O = 20\text{mA}$		0.8	1.2	V
ICC					
I _{START}	$V_{CC} = 12\text{V}$		0.2	0.4	mA
ICC (pre-start)	$V_{CC} = 15\text{V}$, $V(UV) = 0$		0.5	1	mA
ICC (run)			22	26	mA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CAO: Output of the current error amplifier. Also the resistor load for the collector of an optocoupler.

CDC: Connect a charge balance integration capacitor from CDC to GND to achieve an accurate duty cycle clamp. This capacitor also sets the soft start time.

CI: Output of the inductor current waveform synthesizer. Requires a capacitor to ground.

CT: A capacitor from CT to GND sets the oscillator frequency.

DMAX: Programs maximum duty cycle with a resistive divider from VREF to DMAX to GND.

GND: Signal ground.

INV: Inverting input of the current error amplifier.

IOFF: Programs the discharge slope of the capacitor on CI to emulate the down slope of the inductor current waveform.

ION: Input pin to inductor current waveform synthesizer. Apply a voltage proportional to switch current to this pin.

NI: Noninverting input of the current error amplifier.

OUT: Output driver for the gate of a power FET.

PGND: Power ground pin for the output driver. This ground circuit should be connected to GND at a single point.

UV: Line voltage sense pin to insure the chip only operates with sufficient line voltage. Program with a resistive divider from the converter input voltage to UV to GND.

VCC: Chip supply voltage. Bypass with a $1\mu\text{F}$ ceramic capacitor to PGND.

VREF: Precision voltage reference. Bypass with a $1\mu\text{F}$ ceramic capacitor to GND.

VS: Volt second clamp programming pin and feedforward ramp waveform for the pulse width modulator. Connect a resistor to the input line voltage and a capacitor to GND.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout block diagram is shown in Figure 1. The VCC comparator monitors chip supply voltage. Hysteretic thresholds are set at 13V and 10V to facilitate off-line applications. If the VCC comparator is low, ICC is low (<500µA) and the output is low.

The UV comparator monitors input line voltage (VIN). A pair of resistors divides the input line to UV. Hysteretic input line thresholds are programmed by Rv1 and Rv2. The thresholds are

$$V_{IN(on)} = 4.35V \cdot (1 + R_{v1}/R_{v2'})$$

$$V_{IN(off)} = 4.35V \cdot (1 + R_{v1}/R_{v2})$$

$$R_{v2'} = R_{v2} \parallel 90k.$$

The resulting hysteresis is

$$V_{IN(hys)} = 4.35V \cdot R_{v1} / 90k.$$

When the UV comparator is low, ICC is low (<500µA) and the output is low.

When both the UV and VCC comparators are high, the internal bias circuitry for the remainder of the chip is activated. The CDC pin (see discussion on Maximum Duty Cycle Control and Soft Start) and the Output are held low until VREF exceeds the 4.5V threshold of the VREF comparator. When VREF is good, control of the output driver is transferred to the PWM circuitry and CDC is allowed to charge.

If any of the three UVLO comparators go low, the UVLO latch is set, the output is held low, and CDC is discharged. This state will be maintained until all three comparators are high and the CDC pin is fully discharged.

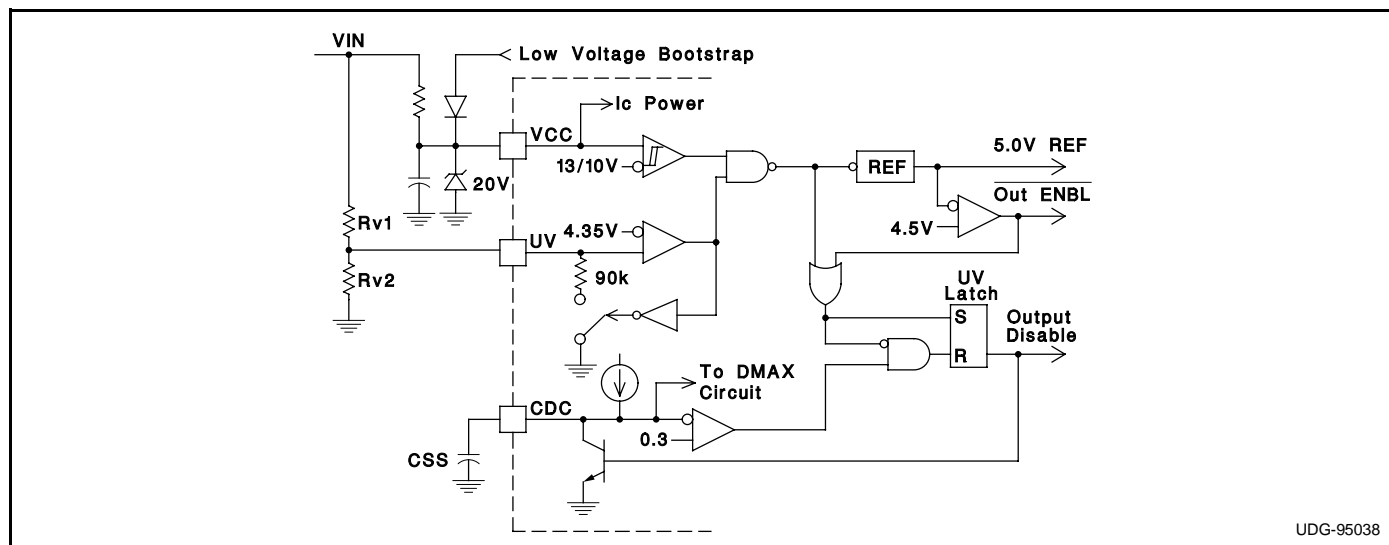


Figure 1: Undervoltage Lockout

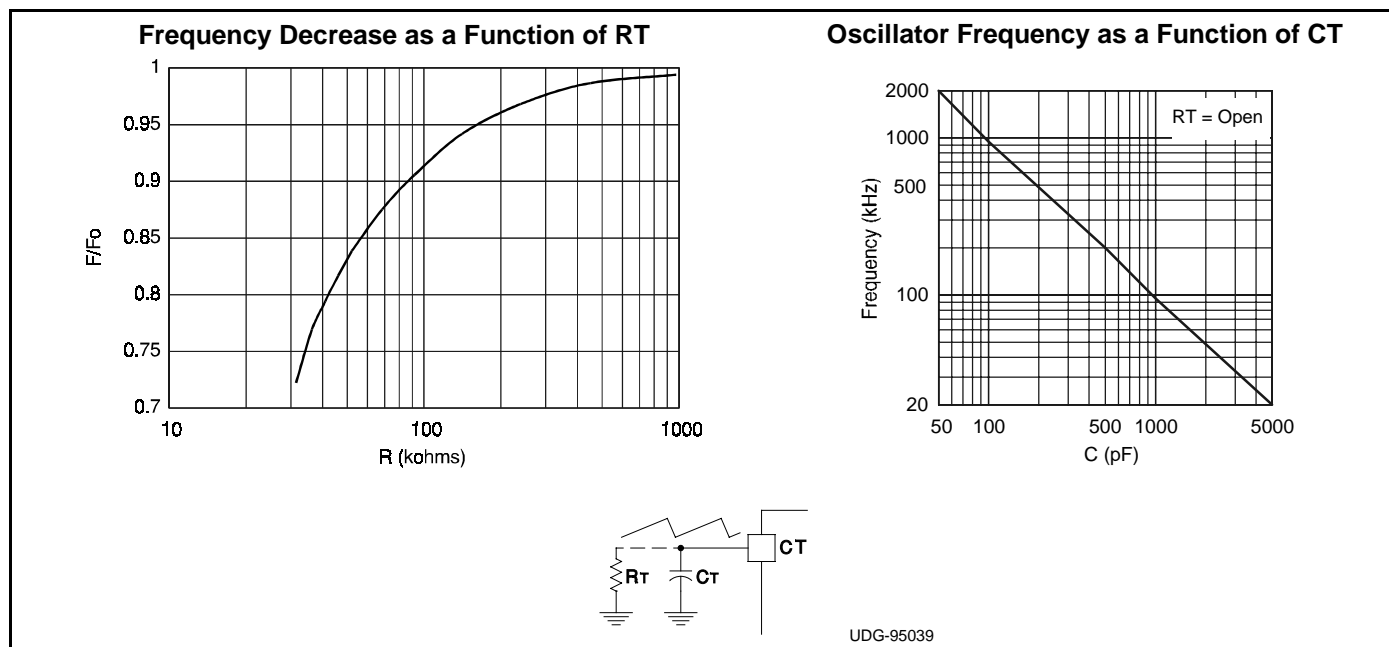


Figure 2: Oscillator Frequency

OSCILLATOR

A capacitor from the CT pin to GND programs oscillator frequency, as shown in Figure 2. Frequency is determined by:

$$F = 1 / (10k \cdot CT).$$

The sawtooth wave shape is generated by a charging current of $200\mu\text{A}$ and a discharge current of $1800\mu\text{A}$. The discharge time of the sawtooth is guaranteed dead time

for the output driver. If the maximum duty cycle control is defeated by connecting DMAX to VREF, the maximum duty cycle is limited by the oscillator to 90%. If an adjustment is required, an additional trim resistor R_T from CT to ground can be used to adjust the oscillator frequency. R_T should not be less than $40k\Omega$. This will allow up to a 22% decrease in frequency.

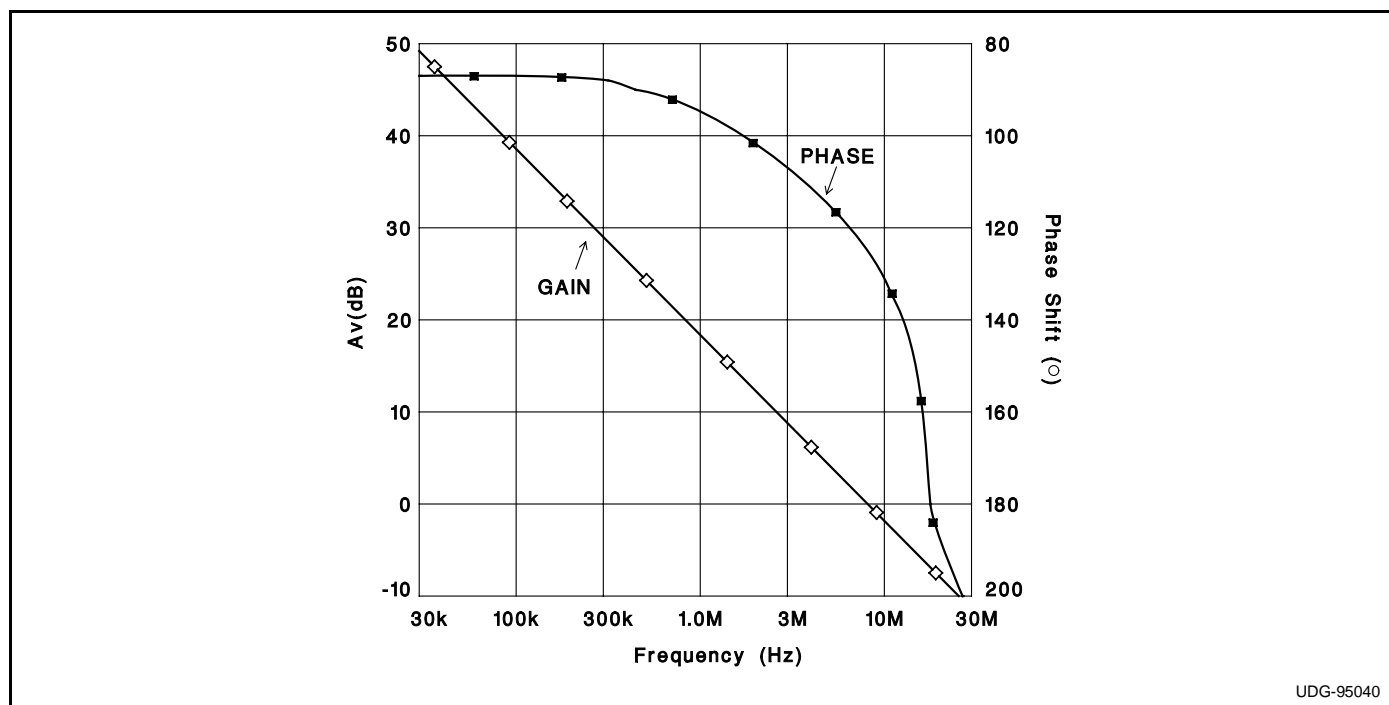


Figure 3: Error Amplifier Gain and Phase Response over Frequency

INDUCTOR CURRENT WAVEFORM SYNTHESIZER

Average current mode control is a very useful technique to control the value of any current within a switching converter. Input current, output inductor current, switch current, diode current or almost any other current can be controlled. In order to implement average current mode control, the value of the current must be explicitly known at all times. To control output inductor current (I_L) in a buck derived isolated converter, switch current provides inductor current information, but only during the on time of the switch. During the off time, switch current drops abruptly to zero, but the inductor current actually diminishes with a slope $dI_L/dt = -V_o/L$. This down slope must be synthesized in some manner on the primary side to provide the entire inductor current waveform for the control circuit.

The patented current waveform synthesizer (Figure 4) consists of a unidirectional voltage follower which forces the voltage on capacitor C_I to follow the on time switch current waveform. A programmable discharge current synthesizes the off time portion of the waveform. I_{ON} is

the input to the follower. The discharge current is programmed at I_{OFF} .

The follower has a one volt offset, so that zero current corresponds to one volt at C_I . The best utilization of the UC3548 is to translate maximum average inductor current to a 4 volt signal level. Given N and N_s (the turns ratio of the power and current sense transformers respectively), proper scaling of I_L to $V(C_I)$ requires a sense resistor R_s as calculated from:

$$R_s = 4V \cdot N_s \cdot N / I_L(\text{max}).$$

Restated, the maximum average inductor current will be limited to:

$$I_L(\text{max}) = 4V \cdot N_s \cdot N / R_s.$$

I_{OFF} and C_I need to be chosen so that the ratio of $dV(C_I)/dt$ to dI_L/dt is the same during switch off time as on time. Recommended nominal off current is $100\mu\text{A}$. This requires

$$C_I = (100\mu\text{A} \cdot N \cdot N_s \cdot L) / (R_s \cdot V_o(\text{nom}))$$

where L is the output inductor value and $V_o(\text{nom})$ is the converter regulated output voltage.

INDUCTOR CURRENT WAVEFORM SYNTHESIZER (cont.)

There are several methods to program IOFF. If accurate maximum current control is required, IOFF must track output voltage. The method shown in Figure 4 derives a voltage proportional to $V_{IN} \cdot D$ (where D = duty cycle). In a buck converter, output voltage is proportional to $V_{IN} \cdot D$. A resistively loaded diode connection to the bootstrap winding yields a square wave whose amplitude is proportional to V_{IN} and is duty cycle modulated by the control circuit. Averaging this waveform with a filter generates a primary side replica of secondary regulated V_o . A single pole filter is shown, but in practice a two or three pole filter provides better transient response. Filtered voltage is converted by R_{OFF} to a current to the IOFF pin to control C_I downslope.

If accurate system maximum current is not a critical requirement, Figure 5 shows the simplest method of downslope generation: a single resistor ($R_{OFF} = 40k$) from IOFF to V_{REF} . The discharge current is then $100\mu A$. The disadvantage to this approach is that the synthesizer continues to generate a down slope when the switch is off

even during short circuit conditions. Actual inductor downslope is closer to zero during a short circuit. The penalty is that the average current is understated by an amount approximately equal to the nominal inductor ripple current. Output short circuit is therefore higher than the designed maximum output current.

A third method of generating IOFF is to add a second winding to the output inductor core (Figure 6). When the power switch is off and inductor current flows in the free wheeling diode, the voltage across the inductor is equal to the output voltage plus the diode drop. This voltage is then transformed by the second winding to the primary side of the converter. The advantages to this approach are its inherent accuracy and bandwidth. Winding the second coil on the output inductor core while maintaining the required isolation makes this a more costly solution. In the example, $R_{OFF} = V_o / 100\mu A$. The $4 \cdot R_{OFF}$ resistor is added to compensate the one volt input level of the IOFF pin. Without this compensation, a minor current foldback behavior will be observed.

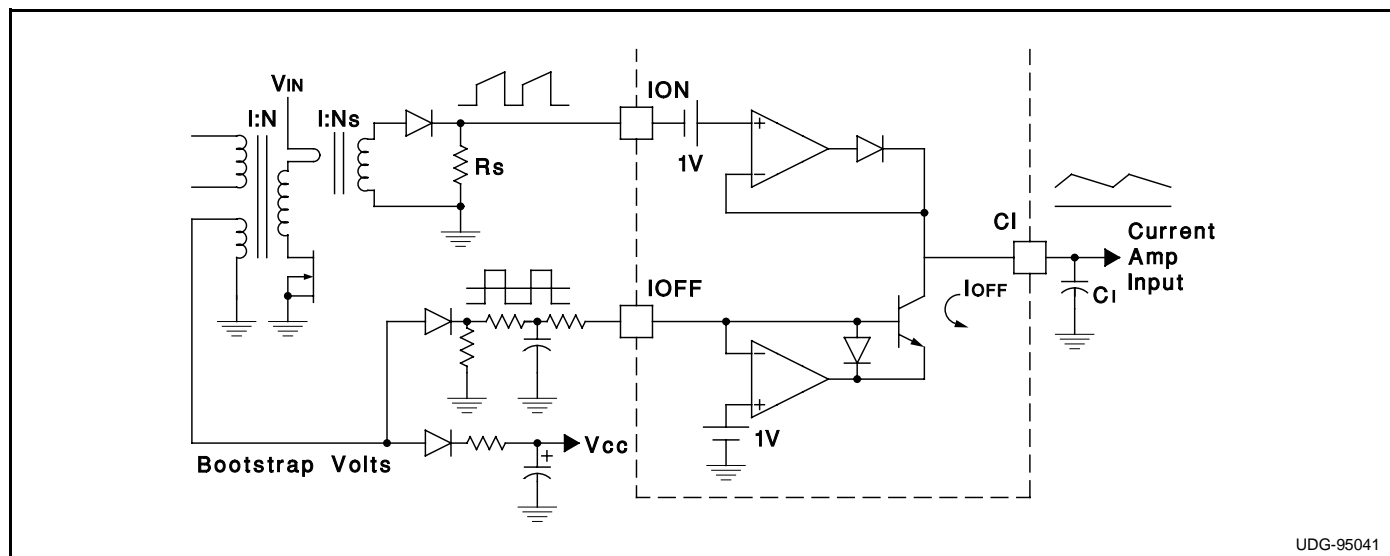


Figure 4: Inductor Current Waveform Synthesizer

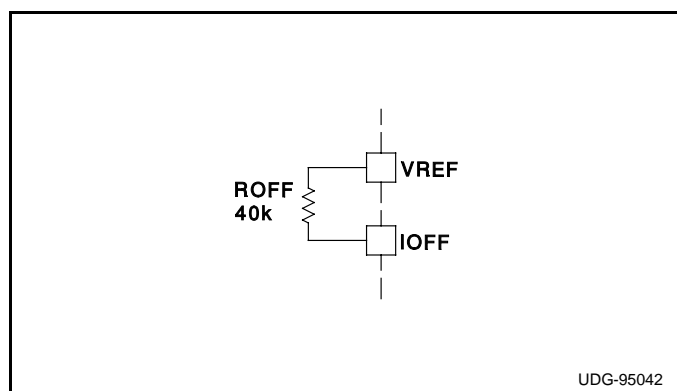


Figure 5: Fixed IOFF

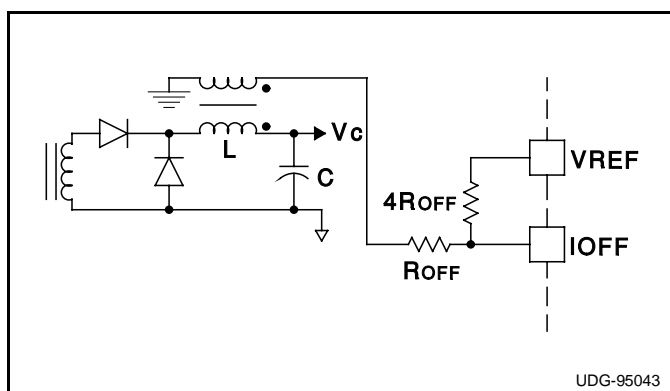


Figure 6: Second Inductor Winding Generation of IOFF

FEED FORWARD PULSE WIDTH MODULATION

Pulse width modulation is achieved by comparing the output of the current error amplifier to the feed forward ramp generated at VS (Figure 7). The charge slope of the ramp is determined by a resistor (RVS) from VS to VIN and a capacitor (CVS) from VS to GND. In the event that CAO is at its maximum voltage, typically 3.3V, the UC3548 will limit the power stage to a volt-second product of:

$$V_{IN} \cdot T_{ON(max)} = 3.3V \cdot R_{vs} \cdot C_{vs}$$

An isolated voltage control loop can be implemented with a secondary side reference, error amplifier and an optoisolator. The optoisolator can be used to override the current amplifier output which is current limited by a 2.5k resistor. In overcurrent situations, the voltage loop turns the optoisolator off and the current error amplifier then assumes duty cycle control resulting in accurately limited maximum output current.

MAXIMUM DUTY CYCLE AND SOFT START

A patented technique is used to accurately program maximum duty cycle. Programming is accomplished by a divider from VREF to DMAX (Figure 7). The value programmed is:

$$D(max) = R_{d1} / (R_{d1} + R_{d2})$$

For proper operation, the integrating capacitor, CDC, should be larger than $T(osc) / 80k$, where $T(osc)$ is the oscillator period. CDC also sets the soft start time constant, so values of CDC larger than minimum may be desired.

The soft start time constant is approximately:

$$T(ss) = 20k \cdot C_{dc}$$

GROUND PLANES

The output driver on the UC3548 is capable of 2A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed (Figure 8). A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not strictly necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The source of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1µF capacitors are recommended for both VCC and VREF. The capacitors from CT, CDC, CI and VS should likewise be connected to the signal ground plane.

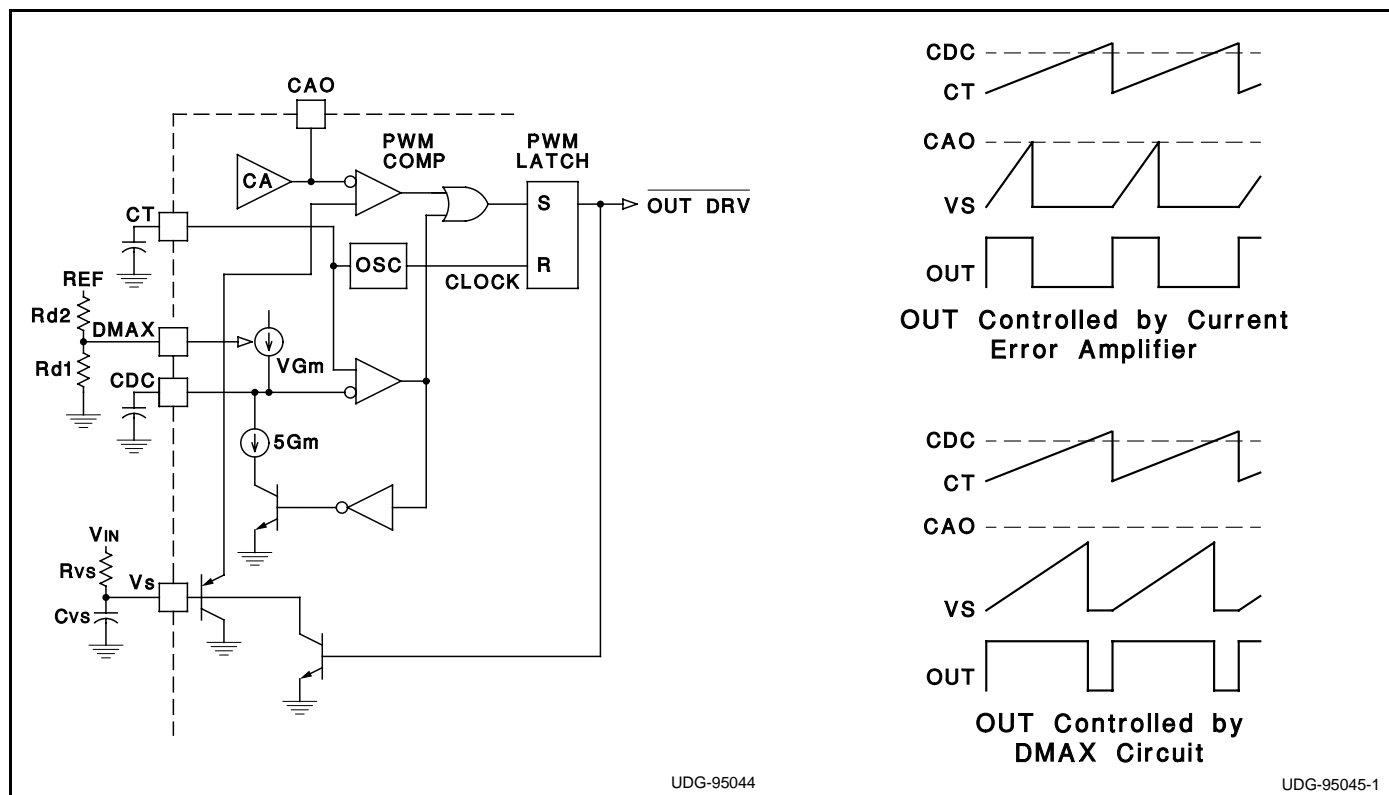
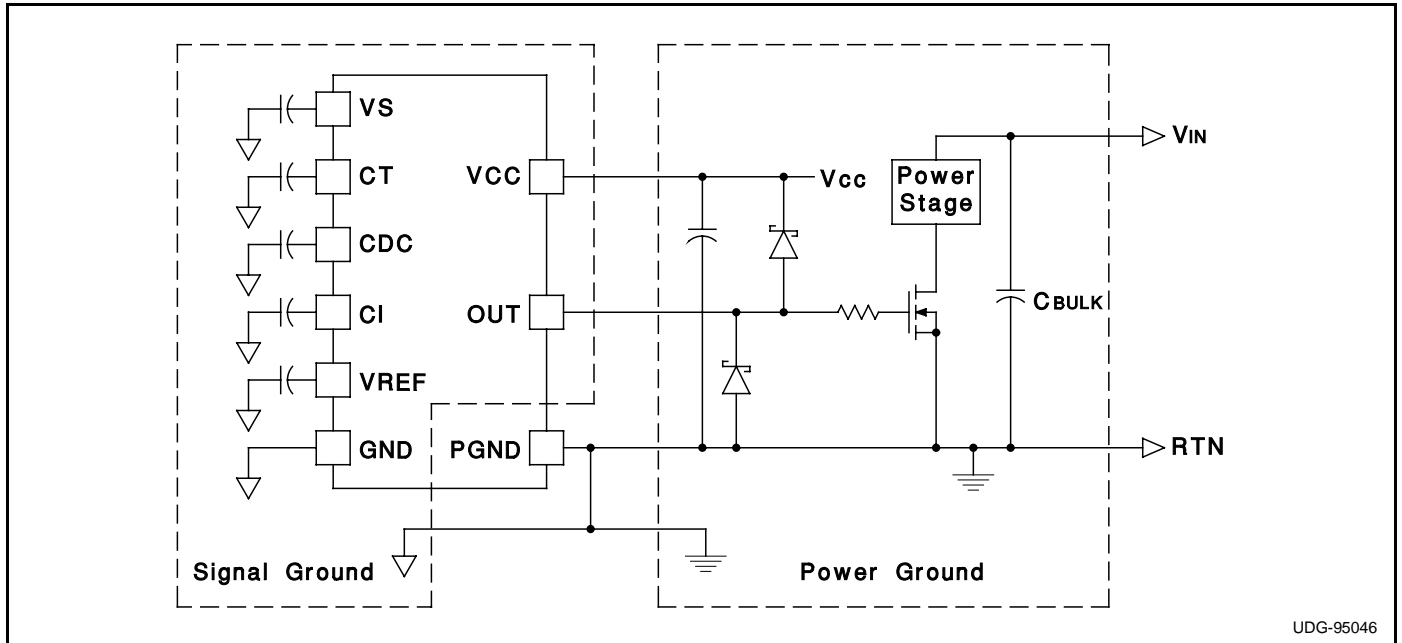
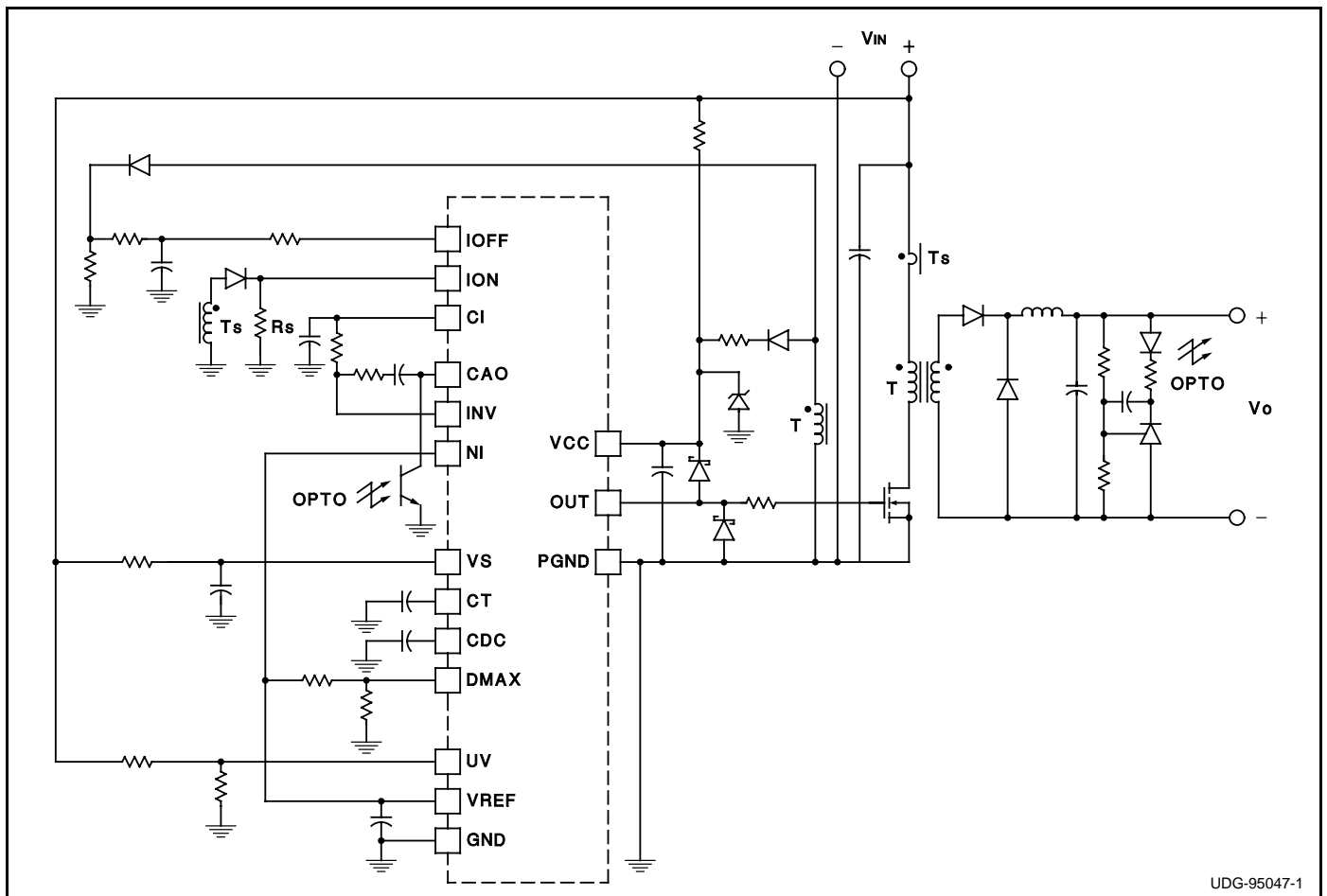


Figure 7: Duty Cycle Control



UDG-95046

Figure 8: Ground Plane Considerations



UDG-95047-1

Figure 9: Typical Application - Voltage Feedforward Control Isolated Forward Converter with Average Current Limiting

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UC3548N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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