Features

- Transient Protection for 2 Differential Line Pairs (4 lines) with Bi-directional.
- Provide Transient Protection for the Protected Differential Line Pair to
  IEC 61000-4-2 (ESD) ±30kV (contact/air)
  IEC 61000-4-4 (EFT) 60A (5/50ns)
  IEC 61000-4-5 (Lightning) 30A (8/20μs)
  Cable Discharge Event (CDE)
- JEDEC SO-8 Package.
- Specific Pin Out For Easy Board Layout.
- Fast Turn-On and Low Clamping Voltage.
- Low Operating Voltage: 2.8V.
- Low Leakage Current
- Solid-State Silicon-Avalanche and Active Circuit Triggering Technology.
- ROHS part is available
- Green part is available

Applications

- WAN/LAN Device
- 10/100/1000 Ethernet
- Power Over Ethernet (POE)
- Switching Systems
- Computers
- Instruments
- Differential Inputs

Description

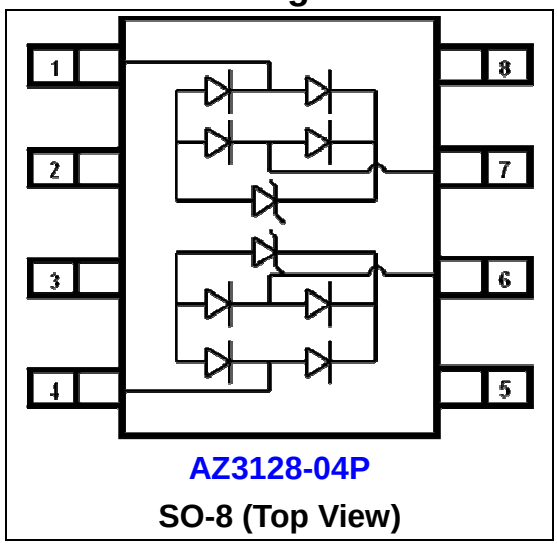
AZ3128-04P is a design which includes bi-directional surge rated clamping cells to protect two differential high speed data-line pairs in an electronic systems. The AZ3128-04P has been specifically designed to protect sensitive components which are connected to the differential line pairs from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ3128-04P is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells provide low clamping voltages to minimize the stress on the protected components.

AZ3128-04P is bi-directional and may be used on lines where the signal swings above and below ground.

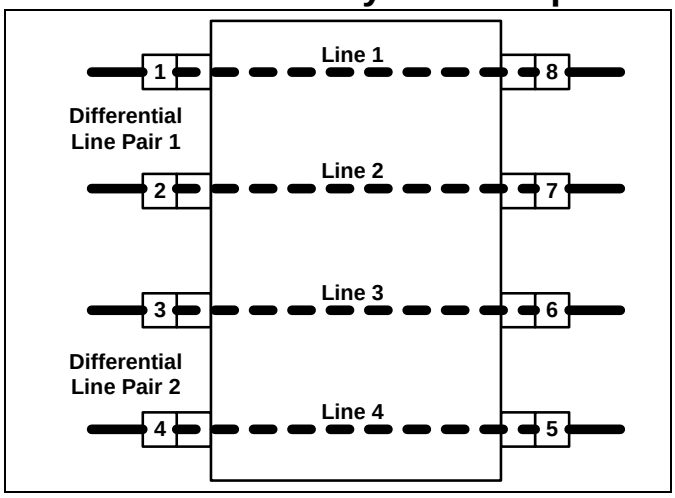
AZ3128-04P may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



AZ3128-04P
SO-8 (Top View)

Circuit Board Layout Example

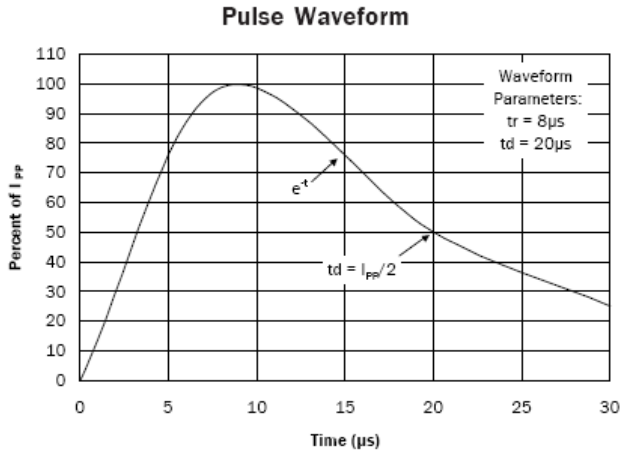


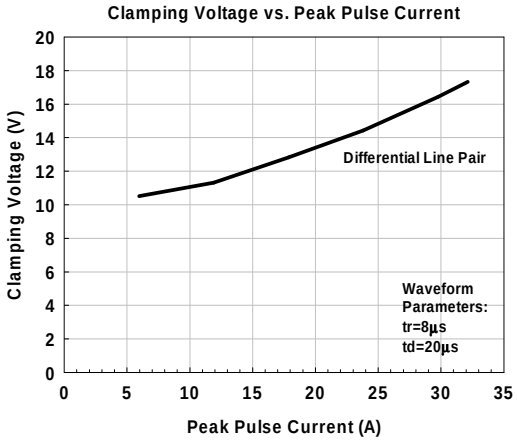
SPECIFICATIONS

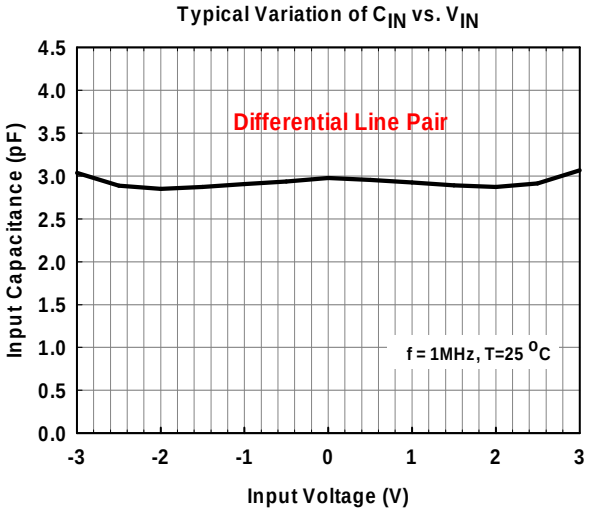
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20us) for each differential line pair	I_{PP}	30	A
ESD per IEC 61000-4-2 (Contact /Air) for each differential line pair	V_{ESD}	±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	^{o}C
Operating Temperature	T_{OP}	-55 to +125	^{o}C
Storage Temperature	T_{STO}	-55 to +150	^{o}C

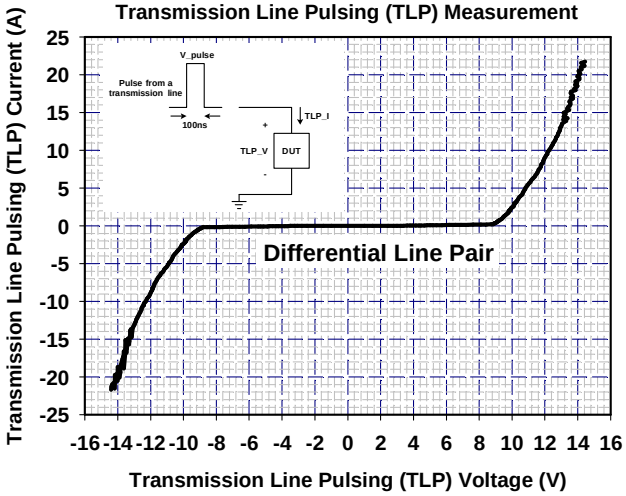
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	T=25 ^{o}C.			2.8	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 2.8V, T=25 ^{o}C (Each Line)			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 ^{o}C. (Each Differential Line Pair)	3			V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA. (Each Differential Line Pair)	2.8			V
Clamping Voltage	V_{CL}	I_{PP}=5A, tp=8/20us, T=25 ^{o}C. (Each Differential Line Pair)			12	V
Clamping Voltage	V_{CL}	I_{PP}=24A, tp=8/20us, T=25 ^{o}C. (Each Differential Line Pair)			16	V
Clamping Voltage	V_{CL}	I_{PP}=30A, tp=8/20us, T=25 ^{o}C. (Each Differential Line Pair)			18	V
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 ^{o}C. (Each Differential Line Pair)		3.0	4.5	pF

Typical Characteristics









Applications Information

The AZ3128-04P is designed to protect four lines against System ESD/EFT/Lightning pulses by clamping them to an acceptable reference. It provides bi-directional protection.

The usage of the AZ3128-04P is shown in Fig. 1. It can be configured to protect two high speed line pairs (four lines). The first line pair is connected to Pin-1, Pin-2, Pin-8, and Pin-7, simultaneously. The second line pair is connected to Pin-3, Pin-4, Pin-6, and Pin-5, simultaneously. The traces must be connected at the bottom of AZ3128-04P.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ3128-04P.
- Place the AZ3128-04P near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transience easily injects to.

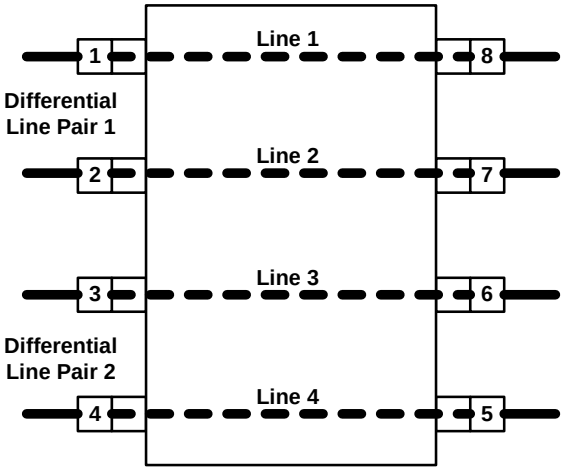
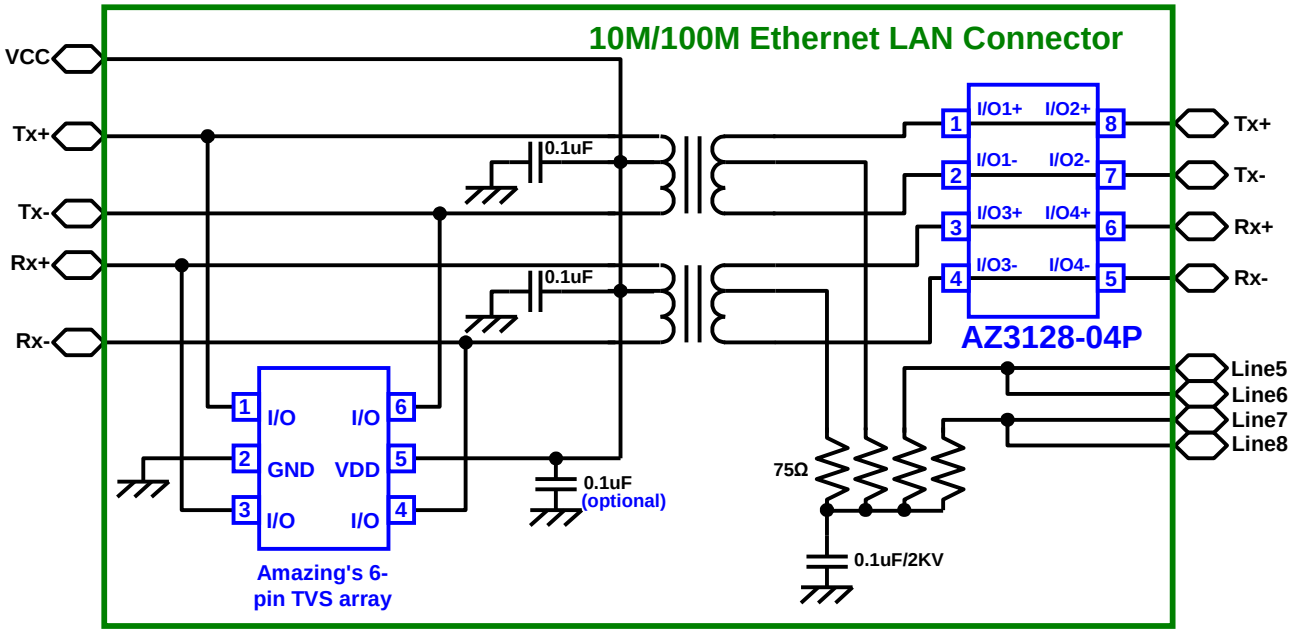
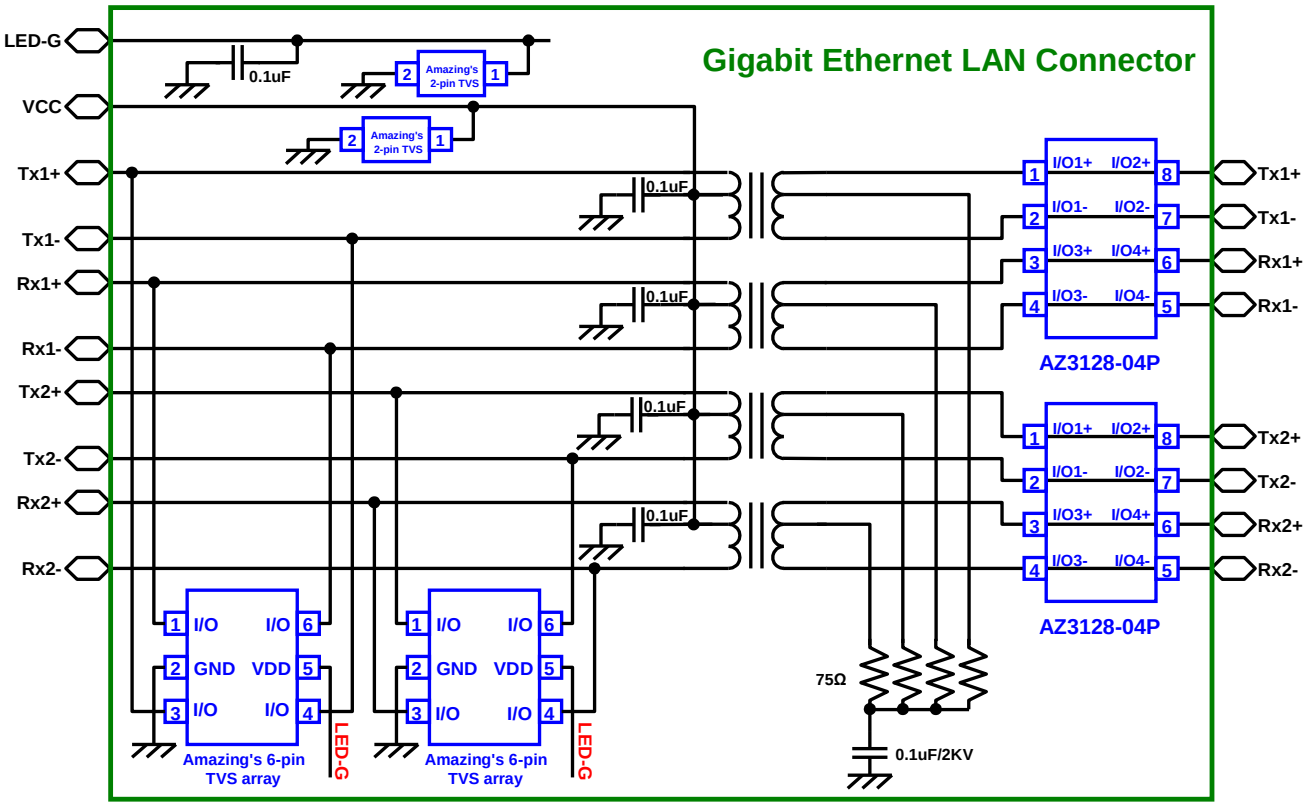


Fig. 1
Configuration for protecting two differential line pairs

Typical Applications



10M/100M Ethernet Protection Circuit



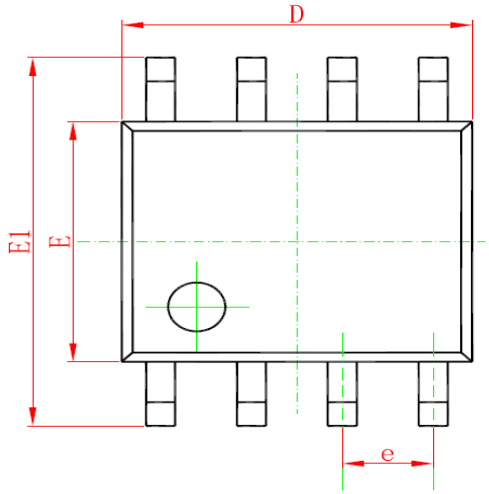
Gigabit Ethernet Protection Circuit

Mechanical Details

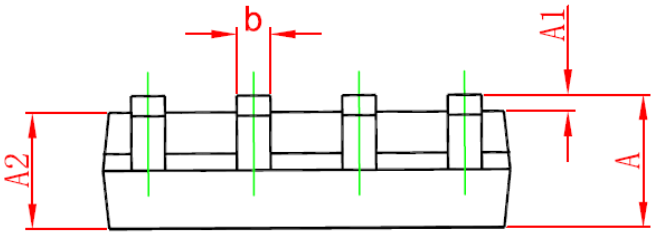
SO-8

PACKAGE DIAGRAMS

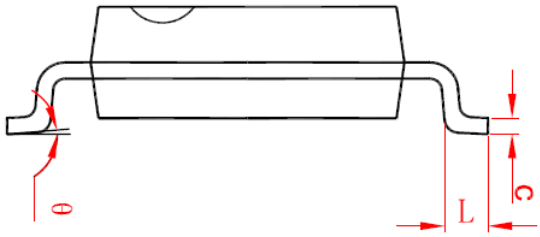
TOP VIEW



SIDE VIEW



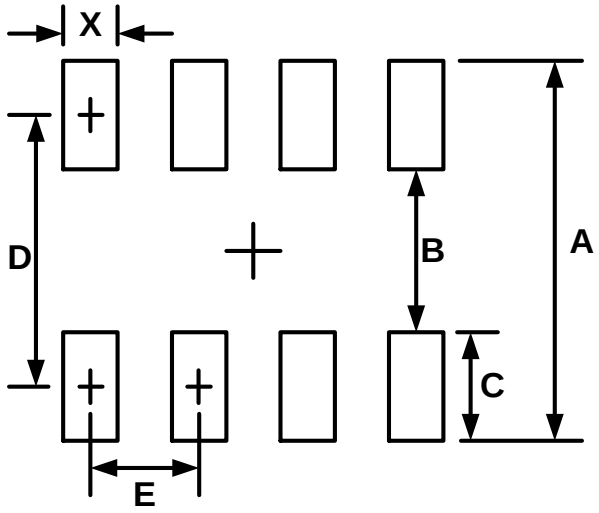
END VIEW



PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	min	max	min	max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.35	1.55	0.053	0.061
b	0.33	0.51	0.013	0.020
C	0.17	0.26	0.007	0.010
D	4.70	5.10	0.185	0.201
E	3.70	4.10	0.146	0.161
E1	5.80	6.20	0.228	0.244
e	1.27 BSC		0.05BSC	
L	0.40	1.27	0.016	0.050
Θ	0	8	0	8

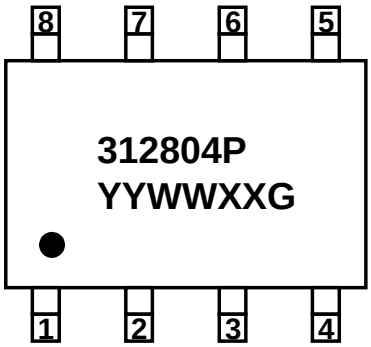
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	7.40	0.291
B	3.00	0.118
C	2.20	0.087
D	5.20	0.205
E	1.27	0.050
X	0.60	0.24

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



312804P = Device Code
YYWWXXG = Date Code

Part Number	Marking Code
AZ3128-04P (Green Part)	**312804P YYWWXXG**

Green means Pb-free, RoHS, and Halogen free compliant

Revision History

Revision	Modification Description
Revision 2011/12/15	Preliminary Release.
Revision 2012/07/31	Formal Release.
Revision 2014/03/25	Add applications “Power Over Ethernet (POE)”