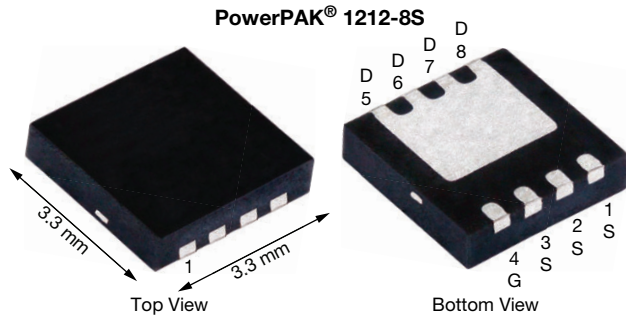


## N-Channel 150 V (D-S) MOSFET



### FEATURES

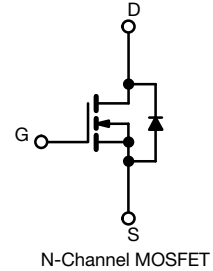
- TrenchFET® with ThunderFET technology optimizes balance of  $R_{DS(on)}$ ,  $Q_g$ ,  $Q_{sw}$ , and  $Q_{oss}$
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Primary side switching
- Synchronous rectification
- DC/DC converter
- Motor drive control
- Load switch



PRODUCT SUMMARY	
$V_{DS}$ (V)	150
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.042
$Q_g$ typ. (nC)	8.5
$I_D$ (A)	25.5 <sup>a</sup>
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiSS72DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	150	V	
Gate-source voltage	$V_{GS}$	$\pm 20$		
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	25.5	A
		$T_C = 70$ °C	20.4	
		$T_A = 25$ °C	7 <sup>b, c</sup>	
		$T_A = 70$ °C	5.6 <sup>b, c</sup>	
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	50		
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	54.8	
		$T_A = 25$ °C	4.2 <sup>b, c</sup>	
Single pulse avalanche current	$I_{AS}$	20		
Single pulse avalanche energy	$E_{AS}$	20	mJ	
Maximum power dissipation	$P_D$	$T_C = 25$ °C	65.8	W
		$T_C = 70$ °C	42.1	
		$T_A = 25$ °C	5.1 <sup>b, c</sup>	
		$T_A = 70$ °C	3.2 <sup>b, c</sup>	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>c</sup>		260		

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$R_{thJA}$	20	25	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	1.5	1.9	

### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 65 °C/W



SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	150	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ mA}$	-	92	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-7.1	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$	-	-	100	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 150\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 150\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 70\text{ }^\circ\text{C}$	-	-	15	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \leq 10\text{ V}$ , $V_{GS} = 10\text{ V}$	20	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 7\text{ A}$	-	0.035	0.042	$\Omega$
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 7\text{ A}$	-	16	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = 75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	-	550	-	pF
Output capacitance	$C_{oss}$		-	120	-	
Reverse transfer capacitance	$C_{rss}$		-	6	-	
Total gate charge	$Q_g$	$V_{DS} = 75\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 7\text{ A}$	-	10.85	22	nC
		$V_{DS} = 75\text{ V}$ , $V_{GS} = 7.5\text{ V}$ , $I_D = 7\text{ A}$	-	8.5	13	
Gate-source charge	$Q_{gs}$		-	3	-	
Gate-drain charge	$Q_{gd}$		-	3	-	
Output charge	$Q_{oss}$	$V_{DS} = 75\text{ V}$ , $V_{GS} = 0\text{ V}$	-	27.7	42	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.24	1.2	2.4	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 75\text{ V}$ , $R_L = 13.4\text{ }\Omega$ , $I_D \cong 5.6\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	-	18	36	ns
Rise time	$t_r$		-	6	12	
Turn-off delay time	$t_{d(off)}$		-	30	60	
Fall time	$t_f$		-	9	18	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 75\text{ V}$ , $R_L = 13.4\text{ }\Omega$ , $I_D \cong 5.6\text{ A}$ , $V_{GEN} = 7.5\text{ V}$ , $R_g = 1\text{ }\Omega$	-	20	40	
Rise time	$t_r$		-	8	16	
Turn-off delay time	$t_{d(off)}$		-	25	50	
Fall time	$t_f$		-	11	22	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	54.8	A
Pulse diode forward current	$I_{SM}$		-	-	50	
Body diode voltage	$V_{SD}$	$I_S = 5.6\text{ A}$ , $V_{GS} = 0\text{ V}$	-	0.8	1.2	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 5.6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	-	60	120	ns
Body diode reverse recovery charge	$Q_{rr}$		-	133	266	nC
Reverse recovery fall time	$t_a$		-	50	-	ns
Reverse recovery rise time	$t_b$		-	10	-	

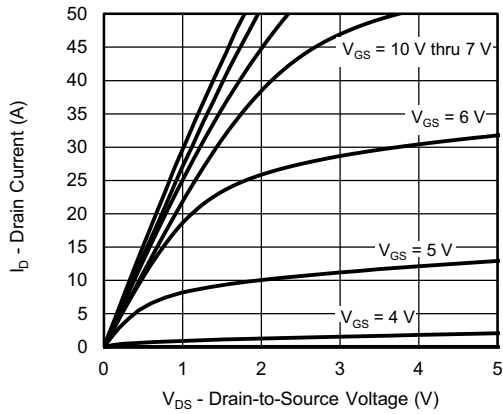
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

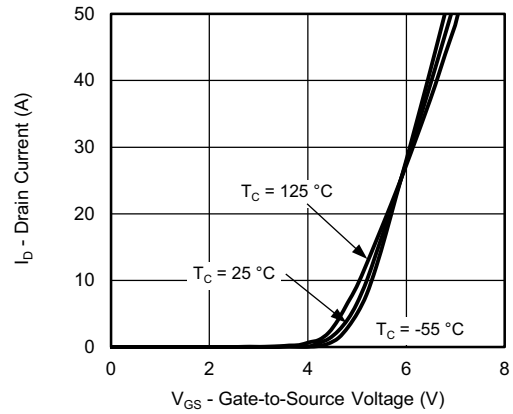
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



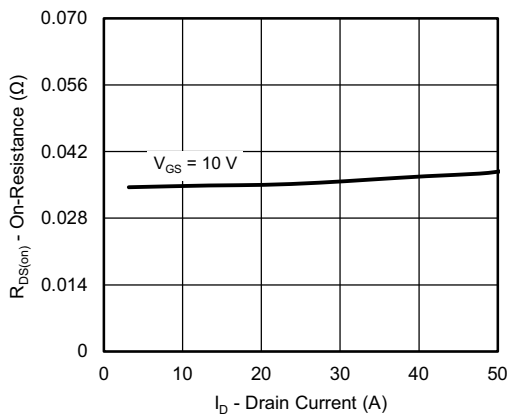
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



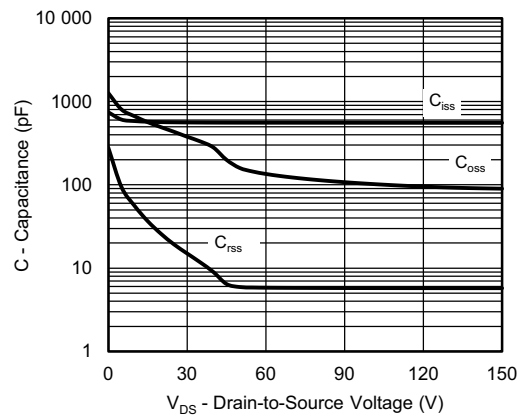
Output Characteristics



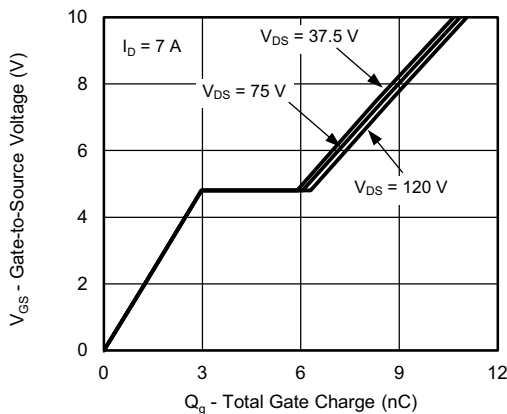
Transfer Characteristics



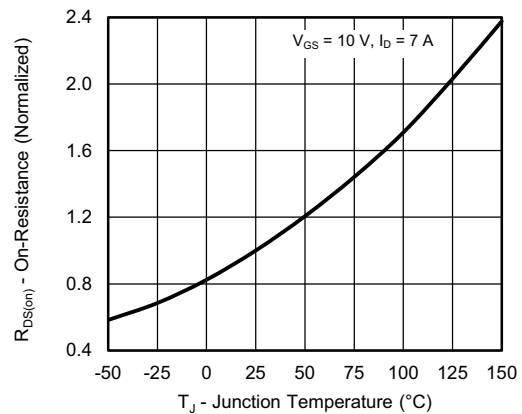
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



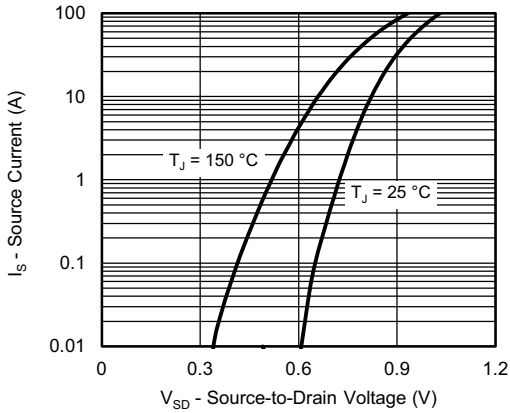
Gate Charge



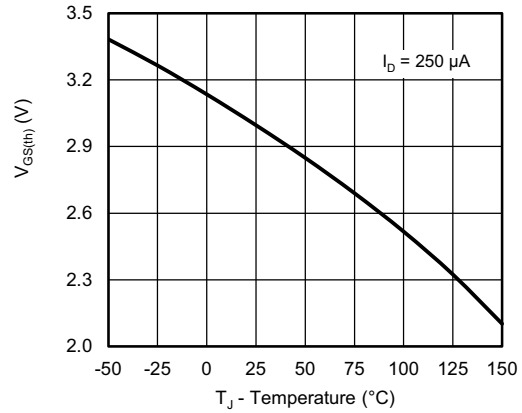
On-Resistance vs. Junction Temperature



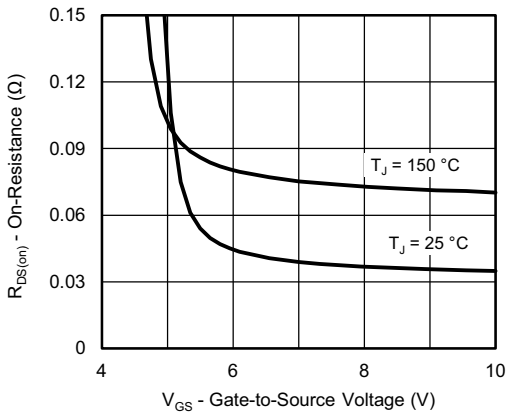
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



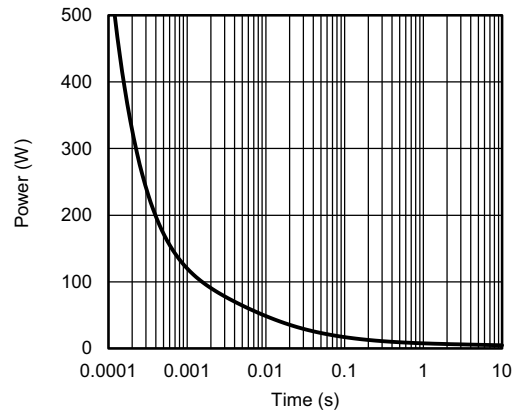
Source-Drain Diode Forward Voltage



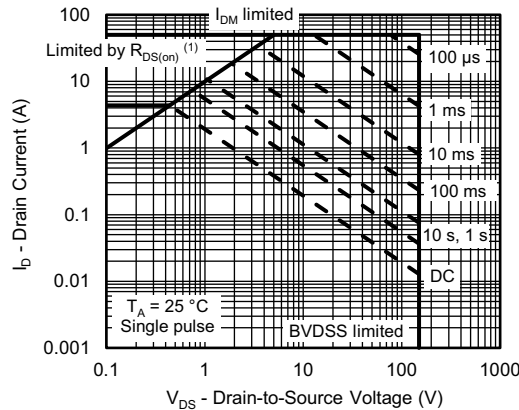
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



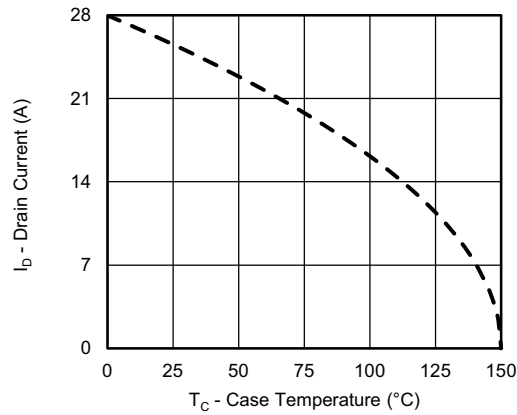
Single Pulse Power, Junction-to-Ambient



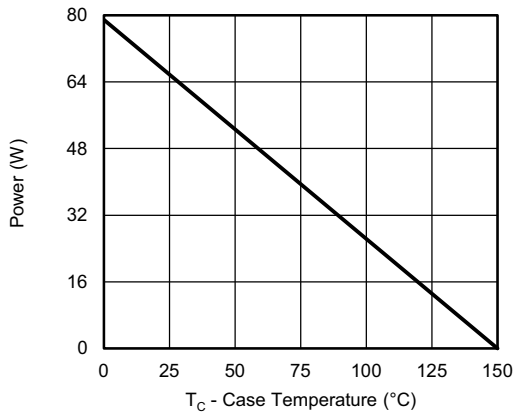
Safe Operating Area, Junction-to-Ambient



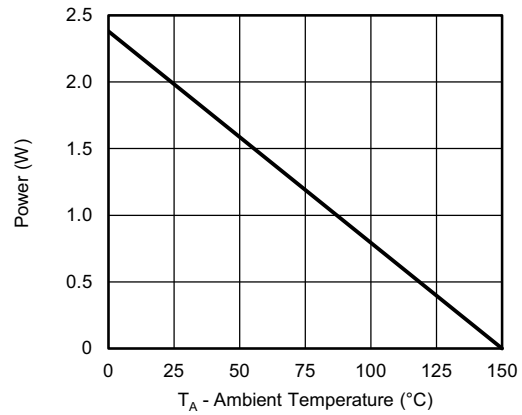
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



**Power, Junction-to-Case**



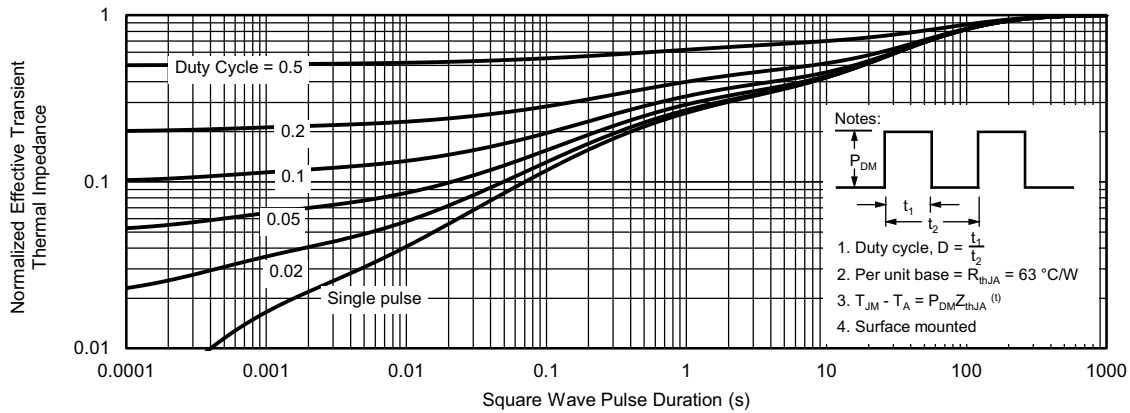
**Power, Junction-to-Ambient**

**Note**

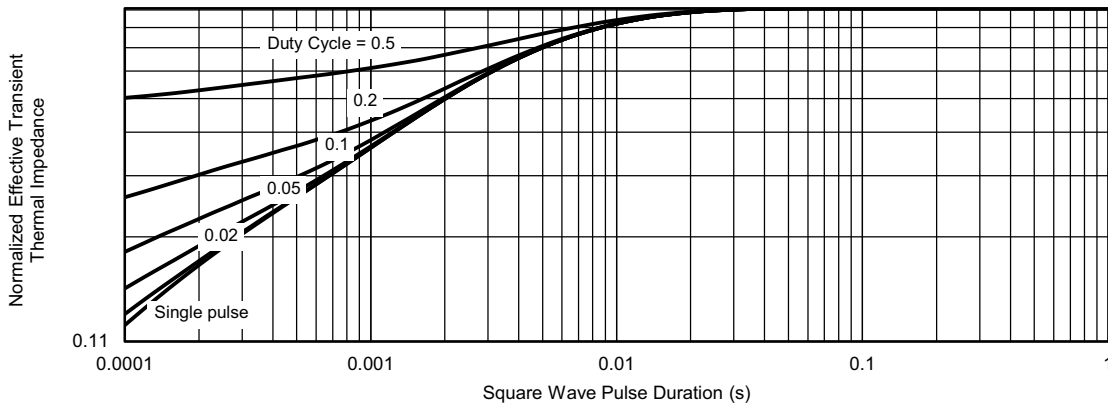
- a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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## Case Outline for PowerPAK® 1212-8S



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.026	0.030	0.033
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		

ECN: C20-0862-Rev. B, 20-Jul-2020  
DWG: 6008

## RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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