



A Product Line of  
Diodes Incorporated



## SPECIFICATION FOR APPROVAL

CUSTOMER \_\_\_\_\_

NOMINAL FREQUENCY \_\_\_\_\_ 12.288000 MHz \_\_\_\_\_

PRODUCT TYPE \_\_\_\_\_ TYPE FJ 2.5x2.0 SEAM SEALED CRYSTAL CLOCK OSCILLATOR \_\_\_\_\_

SPEC. NO. ( P/N ) \_\_\_\_\_ FJ1220010Q \_\_\_\_\_

CUSTOMER P/N \_\_\_\_\_

ISSUE DATE \_\_\_\_\_ August 14, 2018 \_\_\_\_\_

VERSION \_\_\_\_\_ B \_\_\_\_\_

| APPROVED | PREPARED | QA |
|----------|----------|----|
|          |          |    |

### Diodes Incorporated

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- \*Pb-free
- \*RoHS Compliant
- \*HF-Halogen Free
- \*REACH Compliant
- \*AEC-Q200 Compliant

# TYPE FJ 2.5x2.0 SEAM SEALED CRYSTAL CLOCK OSCILLATOR

## ***FJ1220010Q***

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### VERSION HISTORY

| Version No. | Version Date | Description     | Notes |
|-------------|--------------|-----------------|-------|
| A           | Aug.18,2017  | Initial Release |       |
| B           | Aug.14,2018  | Updated Logo    |       |
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### ELECTRICAL SPECIFICATIONS

SRe Part Number : FJ1220010Q

| Item                            | Symbol                         | Specifications      | Units | Notes                              |
|---------------------------------|--------------------------------|---------------------|-------|------------------------------------|
| Nominal Frequency               | F <sub>0</sub>                 | 12.288000           | MHz   |                                    |
| Frequency Stability             | FT                             | ± 50                | ppm   | **See note                         |
| Operating Temperature Range     | TR                             | -40 to +85          | °C    |                                    |
| Supply Voltage                  | V <sub>DD</sub>                | +3.3 ± 10%          | V     |                                    |
| Logic Type                      | LT                             | LVC MOS             |       |                                    |
| Supply Current, Output Enabled  | I <sub>DD</sub> /OE            | 10                  | mA    | Max                                |
| Supply Current, Output Disabled | I <sub>DD</sub> /OD            | 10                  | µA    | Max                                |
| Duty Cycle (Symmetry)           | DC/SY                          | 45 / 55             | %     | Measured 50% of Waveform           |
| Rise / Fall Time                | T <sub>R</sub> /T <sub>F</sub> | 5                   | ns    | Max. measured 10 / 90% of Waveform |
| Output Voltage "0" Level        | V <sub>OL</sub>                | 10% V <sub>DD</sub> | V     | Max                                |
| Output Voltage "1" Level        | V <sub>OH</sub>                | 90% V <sub>DD</sub> | V     | Min                                |
| Output Load                     | CL                             | 15                  | pF    | Max                                |
| Jitter, Phase                   | RMS                            | 1                   | ps    | Max. 12KHz ~ 5MHz Frequency Band   |
| Jitter, Accumulated             | RMS(1-σ)                       | 5                   | ps    | Typ. 20,000 Consecutive Periods    |
| Jitter, Peak to Peak            | Pk-Pk                          | 50                  | ps    | Max. 100,000 Random Periods        |
| Start Up Time                   |                                | 10                  | ms    | Max.                               |
| Storage Temperature Range       |                                | -55 to +125         | °C    |                                    |

※ This product doesn't include harmful substance that stipulated by SONY SS-00259 Level 1 and S-AT2-001 Level 1 standard. RoHS Compliant (Pb - Free).

\*\*Stability includes all combinations of Operating Temperature, Load changes, rated Input (Supply) Voltage changes, Initial Calibration Tolerance (25°C), Aging (1 year at 25°C Average Effective Ambient Temperature), Shock and Vibration.

#### Output Enable / Disable Function

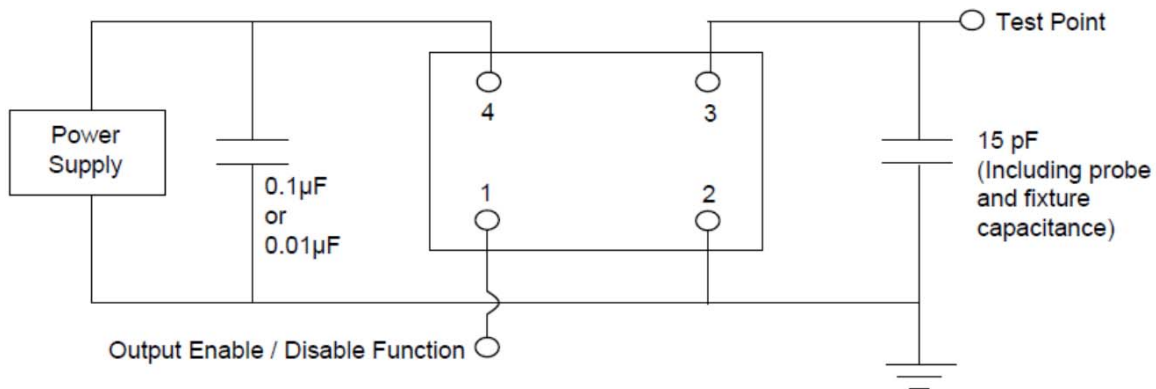
| Parameter  | Min.               | Typ. | Max.               | Units | Notes          |
|--|--------------------|------|--------------------|-------|----------------|
| Input Voltage (Pin1), Output Enable                      | 0.7V <sub>DD</sub> |      |                    | V     | Or Open        |
| Input Voltage (Pin1), Output Disable (low power standby) |                    |      | 0.3V <sub>DD</sub> | V     | Output is Hi-Z |
| Internal Pullup Resistance                               | 30                 |      |                    | KΩ    |                |
| Output Disable Delay                                     |                    |      | 50                 | ns    |                |

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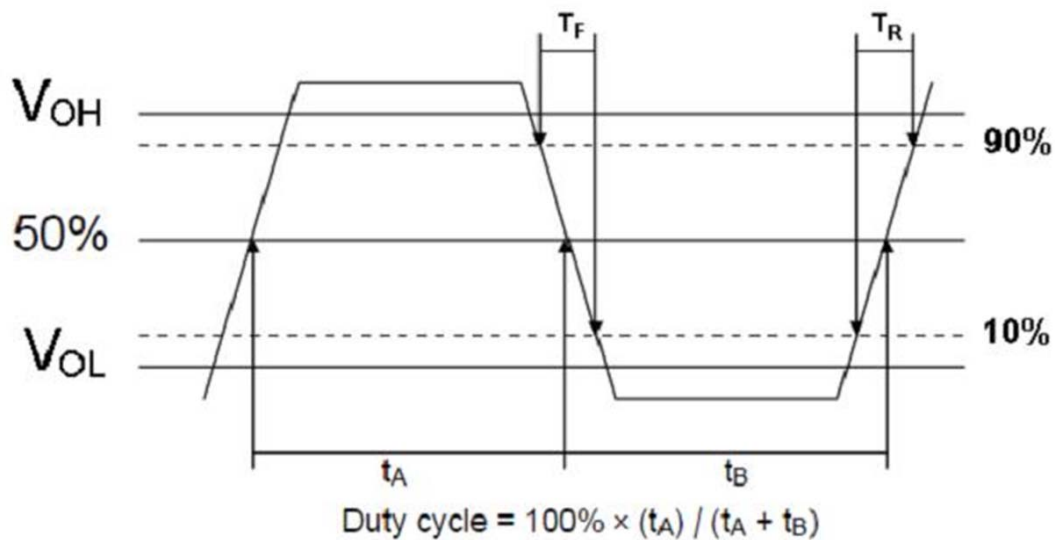
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### TEST CIRCUIT



### OUTPUT WAVEFORM



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## AEC-Q200 RELIABILITY TEST SPECIFICATIONS:

### 1. Initial

- 1.1 Physical Dimensions: JESD22, Method JB1-100
- 1.2 External Visual: MIL-STD-883, Method 2009
- 1.3 Freq. Vs. Temperature: Per Specification/Datasheet

### 2. Mechanical

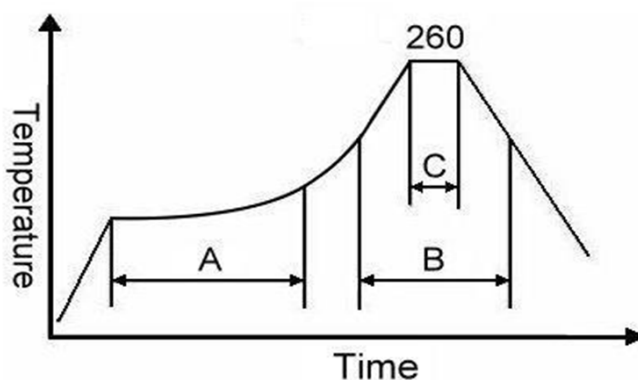
- 2.1 Mechanical Shock: MIL-STD-202 Method 213
- 2.2 Vibration: MIL-STD-202 Method 204
- 2.3 Solderability: J-STD-002
- 2.4 Board Flex: AEC Q200-005
- 2.5 Terminal Strength (SMD): AEC Q200-006

### 3.Environmental

- 3.1 Temp Cycle: JESD22, Method JA-104
- 3.2 Resistance to Solder Heat: MIL-STD-202 Method 210
- 3.3 High Temperature Operating Life: MIL-STD-202, Method 108
- 3.4 High Temp Exposure: MIL-STD-202, Method 108
- 3.5 High Temp & High Humidity: MIL-STD-202, Method 103
- 3.6 Thermal Shock: MIL-STD-202, Method 107

## SUGGESTED IR REFLOW PROFILE

\*As per IPC-JEDEC J-STD-020D



Note:

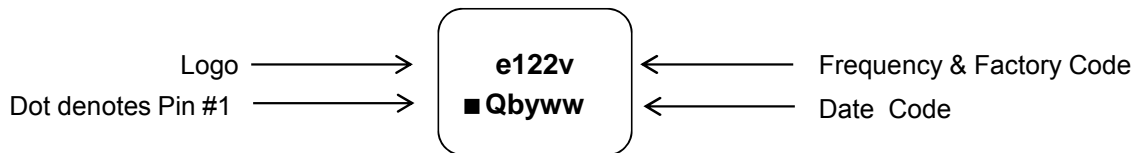
|   | Stage        | Temperature | Time       |
|---|--------------|-------------|------------|
| A | Preheat      | 150~200°C   | 60~120 Sec |
| B | Primary Heat | 217°C       | 60~150 Sec |
| C | Peak         | 260°C       | 10 Sec     |

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### MARKING



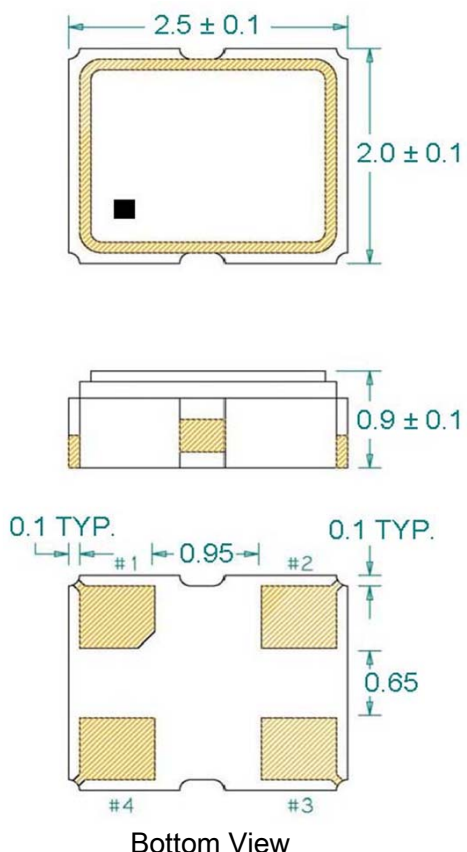
Qb  
Model Series

y  
Year Code (last digit of year)

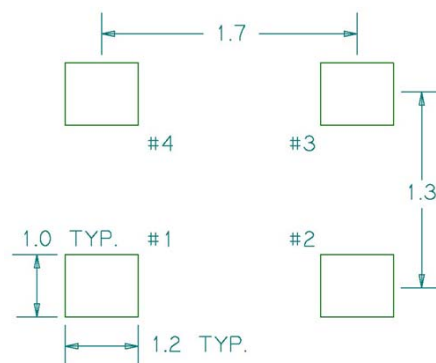
ww  
Week Code

v  
Factory Code

### MECHANICAL DRAWINGS ( Scale:None. Dimensions are in mm.)



#### Recommended Land Pattern\*



\*External high-frequency power decoupling is recommended.(see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

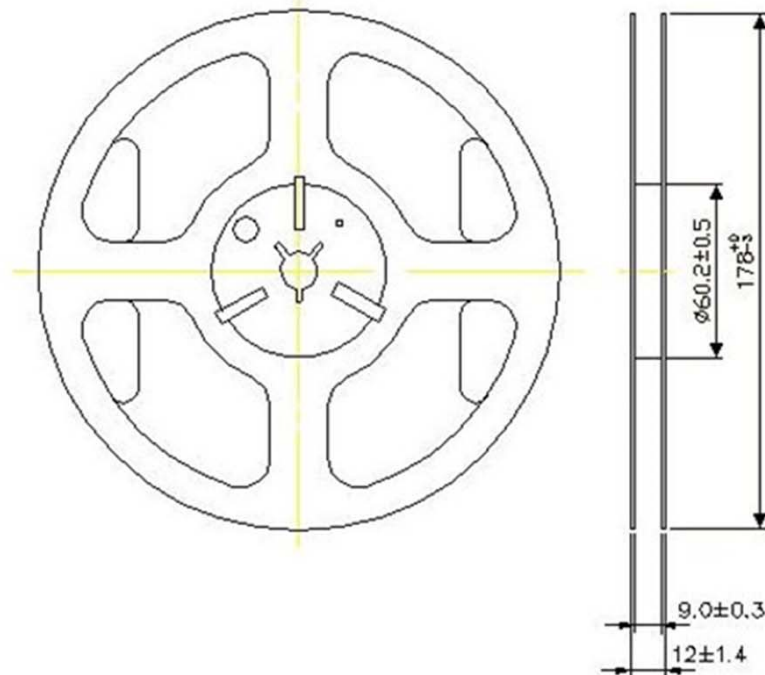
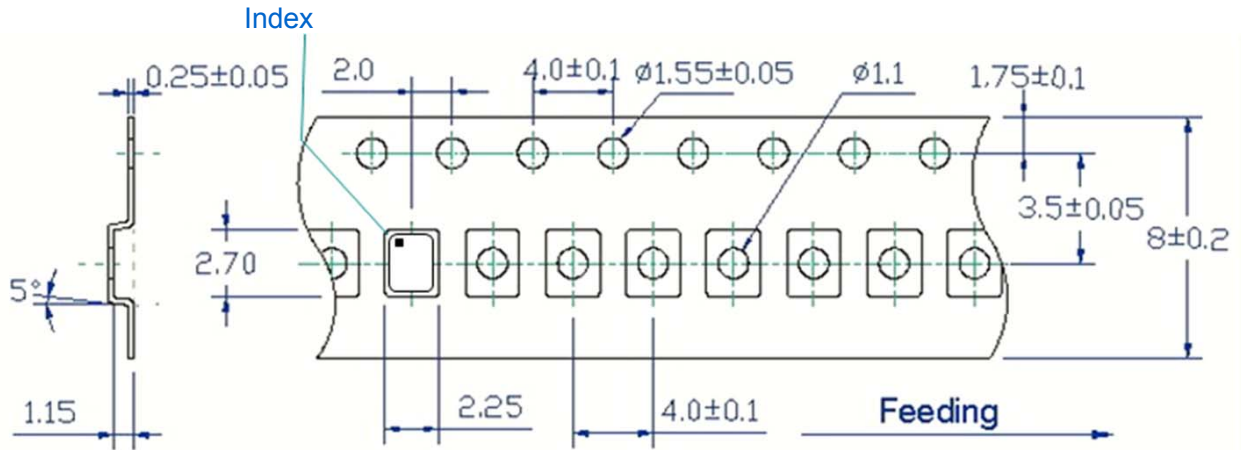
| Pin | Function        |
|-----|-----------------|
| 1   | OE              |
| 2   | Ground          |
| 3   | Clock Output    |
| 4   | V <sub>DD</sub> |

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### TAPE & REEL



1. 230mm minimum leader which consist of carrier and/or tape followed by a minimum of 160mm of empty carrier tape sealed with cover tape.
2. 160mm minimum trailer of empty carrier tape sealed with cover tape.

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### PACKING

